22-nm Gain Cell DRAM for Cryogenic Operation

Tomoki Iwase, Shigeru Yamamoto, Kazutoshi Kobayashi

Kyoto Institute of Technology

***Abstract*—We propose a Gain Cell DRAM（GCDRAM） as an alternative to SRAM, which is advantageous in cryogenic environments. The cell area of the proposed 22-nm GCDRAM is 38% of a 22-nm SRAM. At 22 K, the retention time of the 22-nm GCDRAM becomes 10ms which is 290,000x longer than at room temperature.**

Keywords—Gain Cell DRAM, SRAM, cryogenic

I. Introduction

Current quantum computers lack error correction functionality. However, implementing error correction requires controlling a large number of redundant qubits, which is challenging when controlled from a room-temperature control unit. To address this, control circuits must to be placed inside a dilution refrigerator [1]. Consequently, small-volume and low-power control circuits are essential. GCDRAM emerges as a promising replacement for SRAM, which has a large area and high power consumption, making it a suitable solution for efficient quantum computing control [2].

II. Gain Cell DRAM

The structure of the GCDRAM is shown in Fig. 1. In GCDRAM, the gate capacitance of the read-side transistor (M2) works as the storage node, enabling data retention even after reading. Additionally, lower temperatures increase the threshold voltage and reduce leakage current, significantly extending data retention time. These characteristics make GCDRAM a promising candidate for cryogenic environments. In this study, 22-nm NMOS GCDRAM cells were fabricated with different threshold voltages. The cell area of GCDRAM becomes 38% of SRAM cell, as shown in Table 1.

III. Measurement Results

The data retention time of GCDRAM was evaluated for low-threshold (LVT), standard-threshold (SVT), and high-threshold (HVT) transistors. Since the simulation is only guaranteed down to around 200 K, temperatures below 200 K were evaluated through actual measurements. At room temperature, the data retention time is too short to be evaluated through actual measurements. It assessed through simulations. We conducted actual measurements using the measurement system in Fig. 2, the measurement setup in Fig. 3, the measurement circuit in Fig. 4, and the measurement waveforms in Fig. 5. As shown in Fig. 6, the longer the time between write and read, the lower the current value. The data retention time was defined as the time when the current decrease to 5 μA.

As shown in Figs. 7 - 9, at around 30 K, the data retention time of the LVT GCDRAM cell resulted 30 ms which is 6,700,000x longer than at room temperature. The SVT and HVT cells also have 10 ms and 30 ms retention time at cryogenic temperatures.

Table 2 shows the maximum current for data "1" readout and data "0" readout at the lowest measured temperature. As shown in Table 2, the LVT cell is well-suited for data retention because it maintains a large current difference between data "0" and "1" during readout even at cryogenic temperatures, making it easier to detect 0 or 1.

IV. GCDRAM Array

We designed an 8-bit × 8-word NMOS GCDRAM memory in the 22nm process. The overall memory circuit is shown in Fig. 10 [3]. The sense amplifier is shown in Fig. 11[4]. The control signals to operate the memory array are shown in Fig. 12. The actual simulation results are presented in Fig. 13. The simulation was conducted with the 22nm process at the temperature of 196K. During the simulation, it was confirmed that both write and read operations were successfully performed.

V. Conclusion

In this paper, the design and evaluation of GCDRAM were conducted, and its effectiveness in cryogenic environments was demonstrated. The data retention time of GCDRAM was in nano seconds at room temperature. But by lowering the temperature to around 30K, it was confirmed that the retention time was extended to several tens of milliseconds. Future work will focus on evaluating the speed and power consumption of the memory array.

Acknowledgment

This work was (is) supported by Japan Science Technology (JST) Moonshot R&D Grant Number JPMJMS226A.

This work was also supported through the activities of d-lab VDEC, The University of Tokyo, in collaboration with NIHON SYNOPSYS G.K., Cadence Design Systems and Siemens Electronic Design Automation Japan K.K.

References

[1] Kazutoshi Kobayashi, “Scalable Highly Integrated Quantum Bit Error Correction System by Classical Electronics”, ASICON, IEEE, 2023.

[2] Ki Chul Chun, Pulkit Jain, Tae-Ho Kim, and Chris H. Kim, “A 667 MHz Logic-Compatible Embedded DRAM Featuring an Asymmetric 2T Gain Cell for High Speed On-Die Caches”, IEEE, 2012.

[3] Tai-Feng Chen, Yutaka Masuda, and Tohru Ishihara, “A Standard Cell Memory Based on 2T Gain Cell DRAM for Memory-Centric Accelerator Design”, SOCC, IEEE, 2023.

[4] Rakshith Saligram, Suman Datta, and Arijit Raychowdhury, “CryoMem: A 4–300-K 1.3-GHz Hybrid 2T-Gain-Cell-Based eDRAM Macro in 28-nm Logic Process for Cryogenic Applications”, IEEE, 2021.

Ⅱ. Gain Cell DRAM

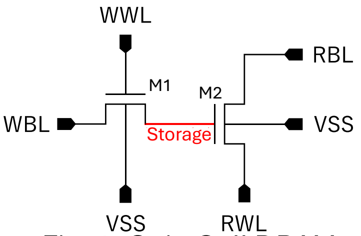

Fig. 1. Gain Cell DRAM

Table1 Cell area

	6T-SRAM	GCDRAM
Cell area	$0.465\mu m^2$	$0.177\mu m^2$

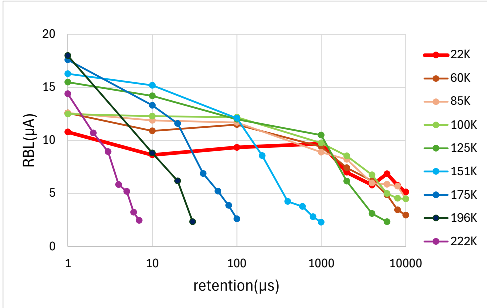

Fig. 6. Current measurement results (SVT)

Ⅲ. Measurement results

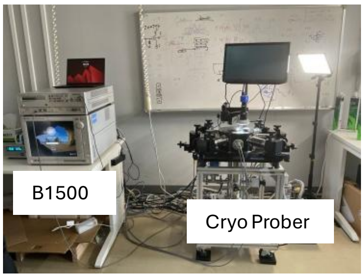

Fig. 2. Measurement system

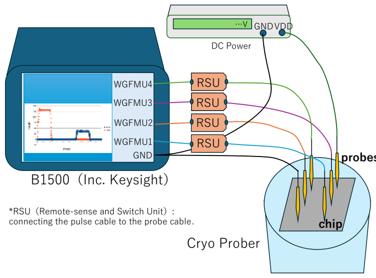

Fig. 3. Measurement setup

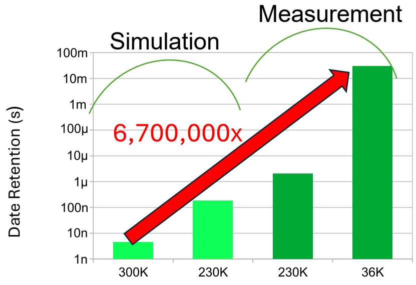

Fig. 7. LVT-retention time

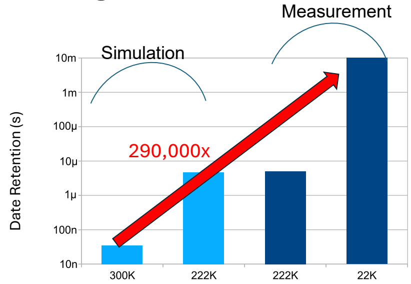

Fig. 8. SVT-retention time

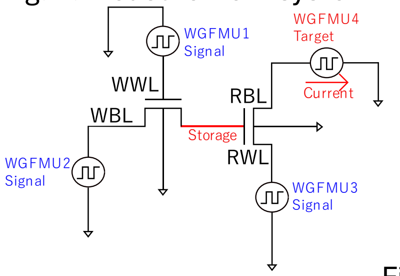

Fig. 4. Measurement circuit

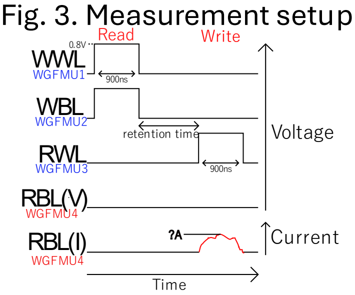

Fig. 5. Measurement waveforms

Table2 Read current at low-temperature

	LVT	SVT	HVT
1read（μA）	26.9	10.8	7.81
0read（μA）	2.05	1.91	2.47
1read-0read（μA）	24.9	8.89	5.34

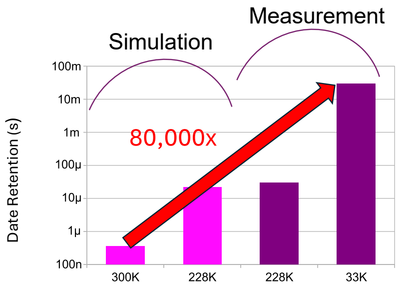

Fig. 9. LVT-retention time

Ⅳ. GCDRAM array

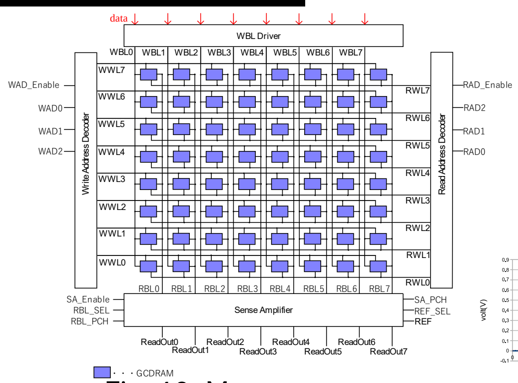

Fig. 10. Memory array

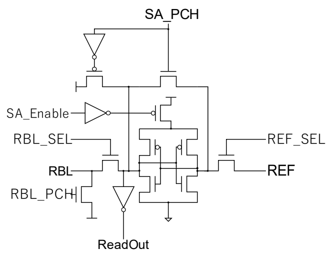

Fig. 11. Sense amplifier

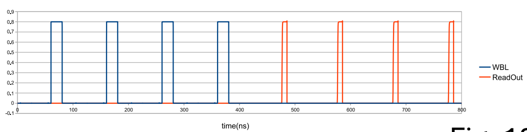

Fig. 13. Readout

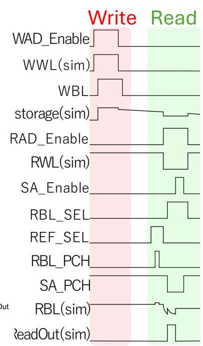

Fig. 12. Control signals