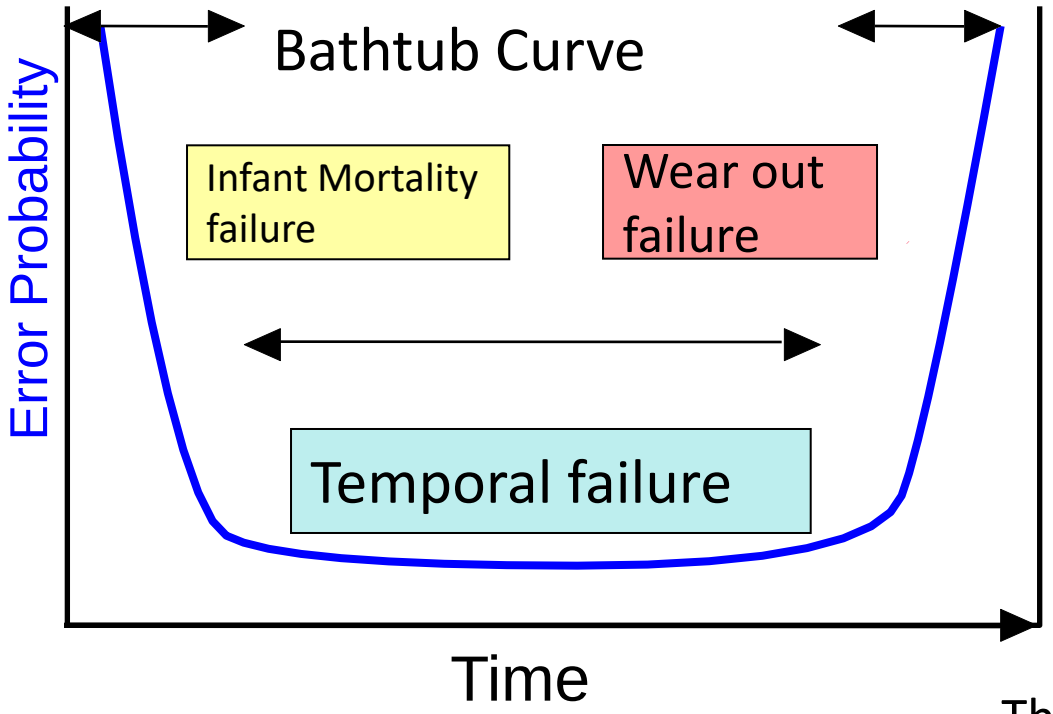
Neutron, Carbon and Heavy-ion Beam Irradiation to Measure Soft Errors on Radiation-hard Circuits for Automotive and Aerospace Applications

Kazutoshi Kobayashi
Kyoto Institute of Technology
Japan
kazutoshi.kobayashi@kit.ac.jp

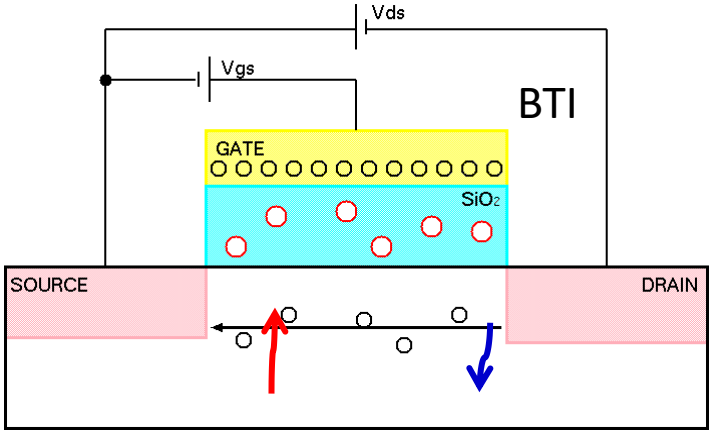
Outline

- Reliability issues in Si-based semiconductor chips
- Soft errors
  - What is soft error?
  - Mitigation techniques
- How to evaluate soft errors
  - Acceleration tests by using beam facilities
    - White neutron
    - Clinical carbon beam
    - Heavy ions
- Radiation-hard flip-flop
- Conclusion

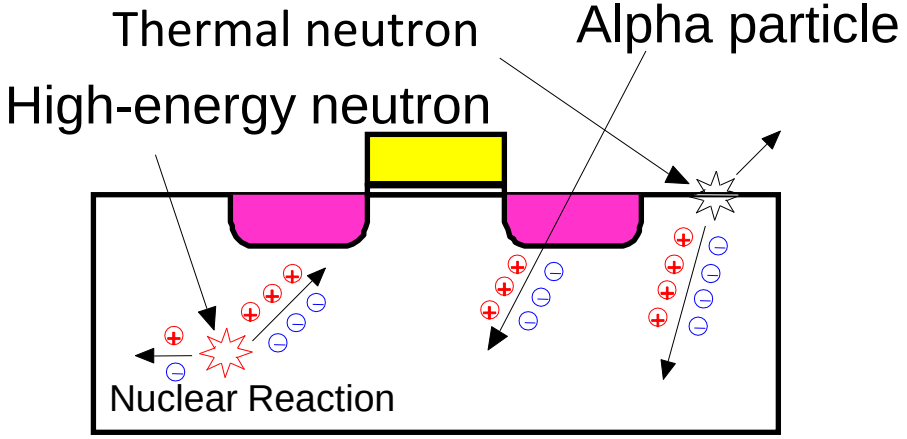
Reliability Issues in Si-based Semiconductor Chips



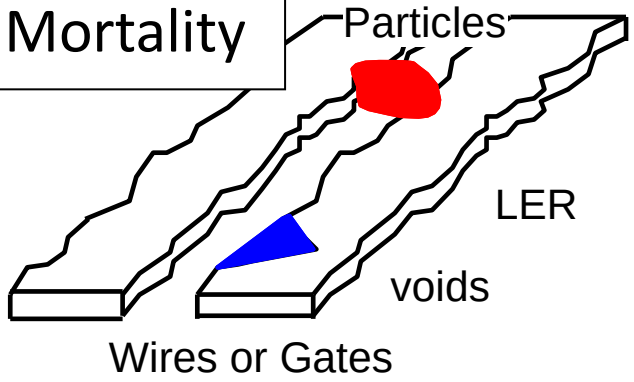
Wear Out (Aging)



Temporal (Soft error)



Infant Mortality



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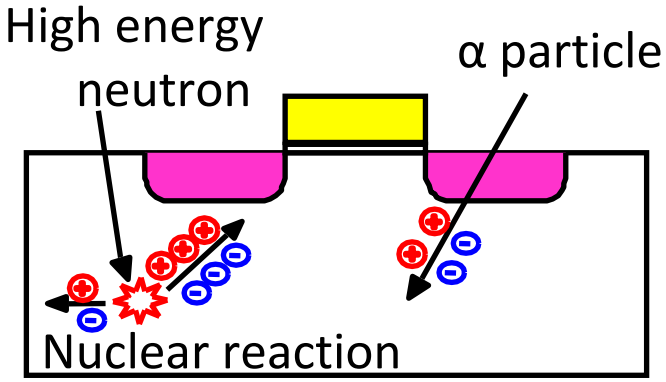
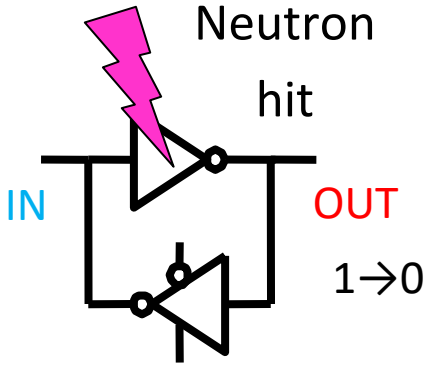
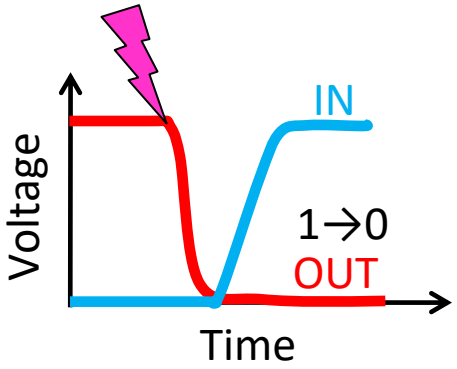
What is Soft Error?

From sky

From radio isotope



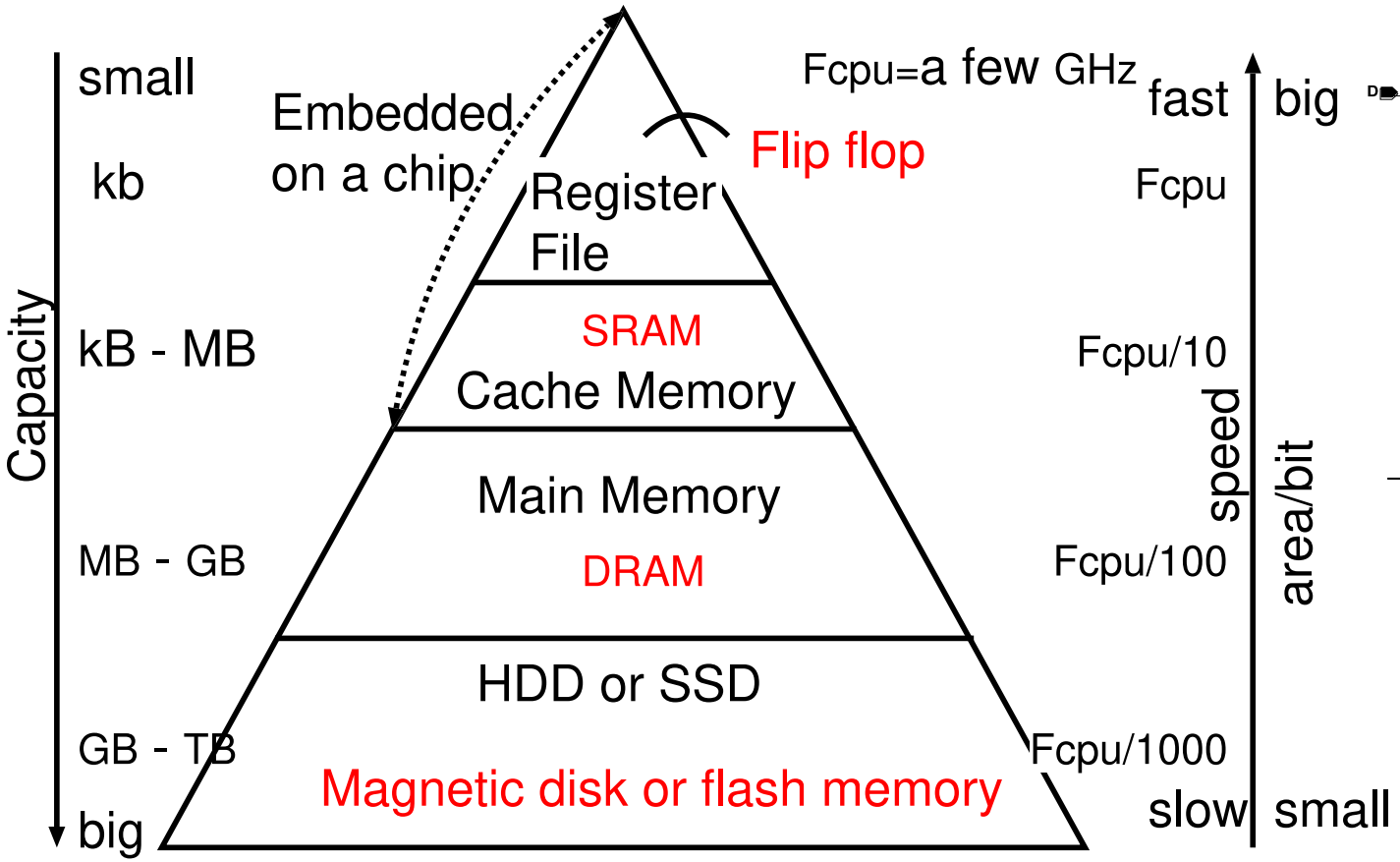


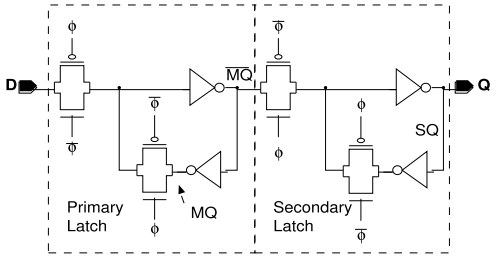


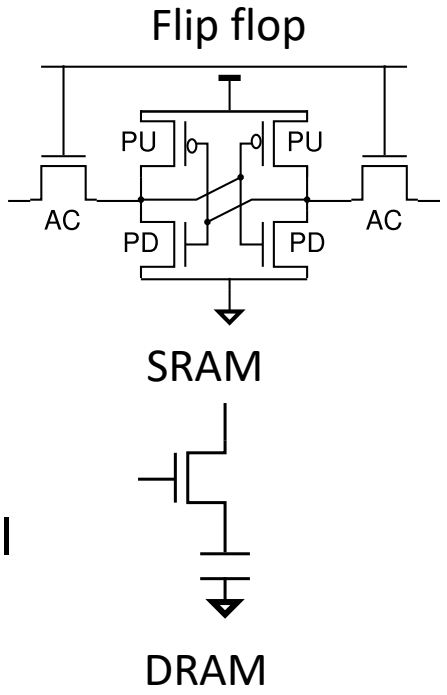
- Caused when a radiation particle penetrates in Si and generates e–h pairs
  - When neutron hits a Si atom (not always). Whenever α particles go through chip
- Upset storage cells such as SRAMs/FFs on a chip
  - Called Single Event Upset (SEU) = Soft Error
- A pressing issue of semiconductor chips for automotive, aerospace and HPC
- Not so many companies / researchers know well about soft errors. Unknown errors → Soft error?

Memory Hierarchy of Computers

- Flip of storage (memory) cells = soft errors
- Flip-flops (FF) and SRAM are weak, while DRAM is strong







Soft Errors on SRAM for Workstation

[EETimes 2001]

Sun CEO
Scott McNealy
[Forbes 2000]

We never buy IBM's SRAMs

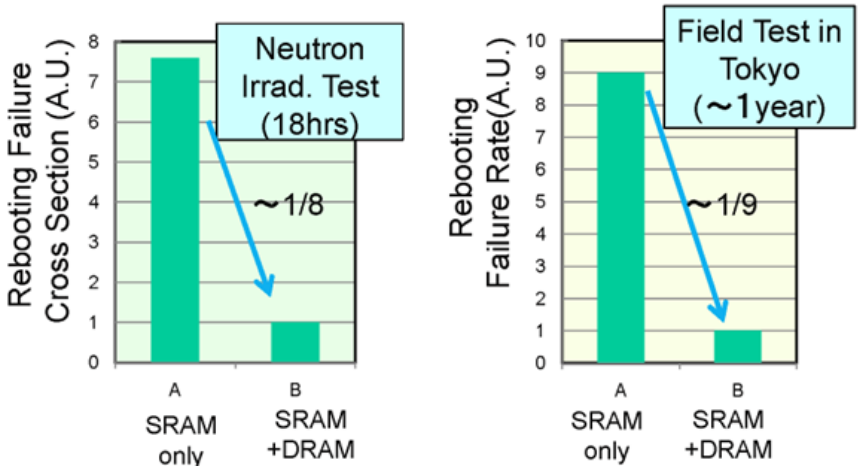
- SRAM from IBM happened to be weak against soft errors.
- Some of Sun's mission critical servers faltered due to soft errors in cache memory

3B JPY (20M USD) Loss by Soft Errors

- In 2019, Yokogawa Electric announced that they lost 3B JPY caused by soft errors.
- I heard that some electronic equipment happened to be weak against soft errors

YOKOGAWA

- Usually, it is very hard to recognize errors are caused by soft errors.
- Hitachi revealed that error rates are reduced by 1/8–1/9 after replacing SRAM with DRAM with error correction.

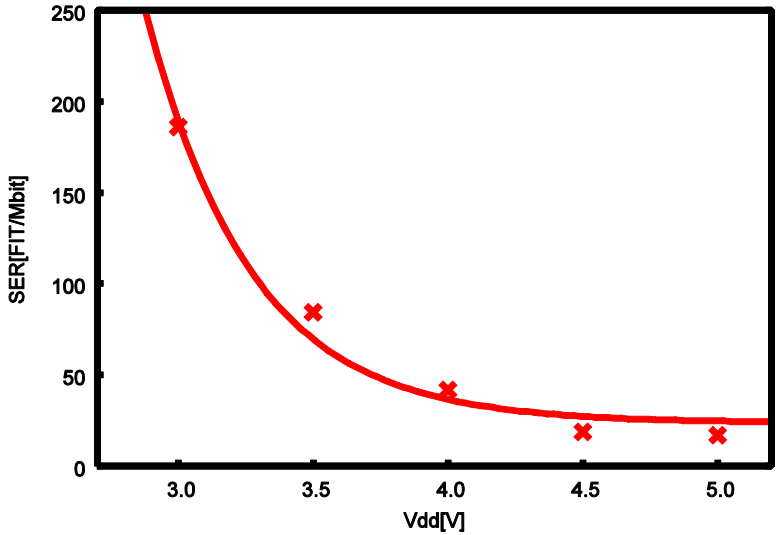


Shimbo, *SELSE7* (2011)

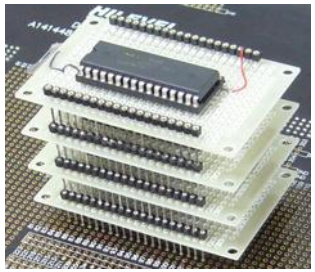
Almost all unknown errors are caused by soft errors

Reliability Metrics: FIT

- FIT
  - Failure in Time
  - # of errors / 10^9 hours (114k years)
  - # of errors / 1 M (10^6) products /1000 (10^3) hours (40 days)
- Example
  - FIT rate of 1 μm 1Mbit SRAM: 200 FIT/Mbit at 3 V
    - 1 error / 570 years / Mbit
  - FIT rate of DDR4 DRAM: a few FIT/Gbit



Measurement Data of 1 Mbit SRAM at RCNP



Soft Error Threaten Safety

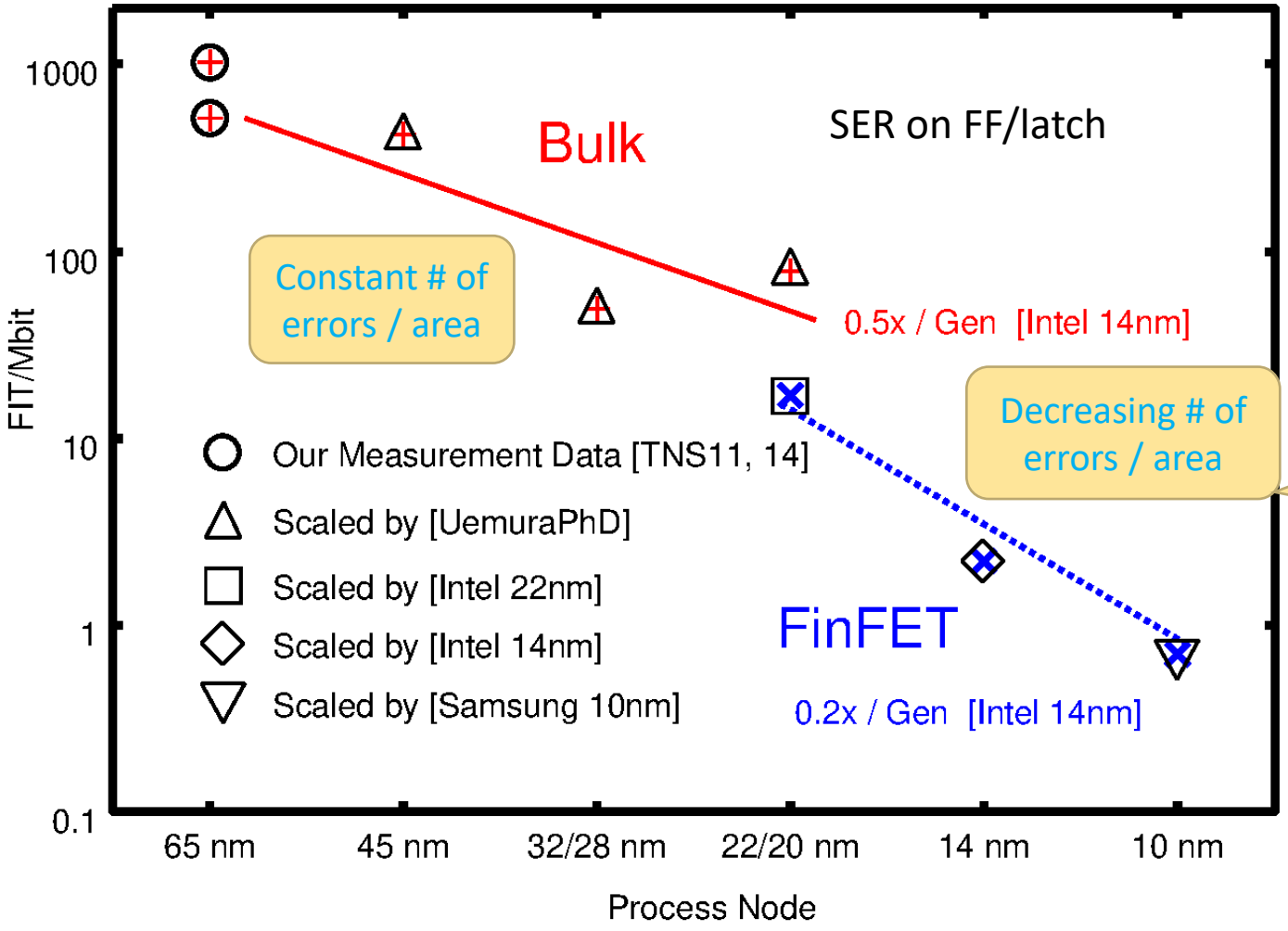
- Error rates
  - Standard SRAM/FF: ～1000 FIT/Mbit
  - Standard ASIC : 100,000 FIT/chip ≒ 1 error/year
- Automotive and Aviation
  - An error leads to an accident

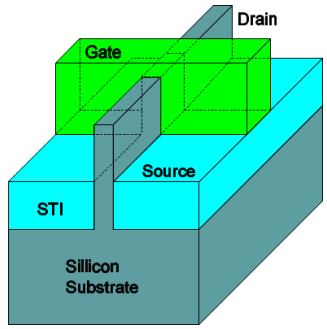
ISO26262 definition of automotive safety

Level	FIT rate	Objective
ASIL-A	< 1000	Convenience (Rear-camera)
ASIL-B, C	<100	Safety (Break assistance, Dashboard display)
ASIL-D	**<10**	Full automatic driving (Tesla, Cruise…)

https://www.motor1.com/news/590053/gm-cruise-driverless-taxi-california/

Scaling Trend of Soft Error Rate (SER)





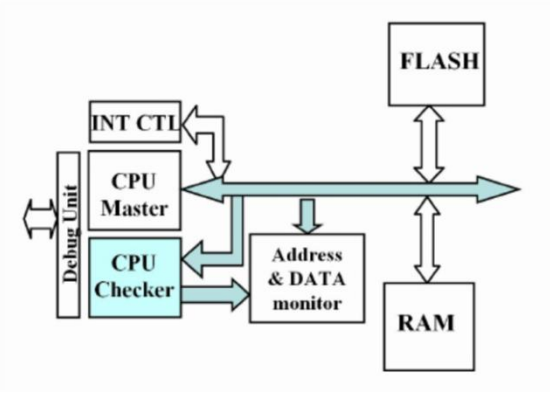
FinFET

# of chips / system is increasing!

[TNS11] R. Yamamoto et. al, TNS, pp. 3053-3059 (2011), [TNS14] K. Kobayashi et. al, TNS, pp. 1881-1888 (2014)
[UemuraPhD] T. Uemura, "A Study on Soft Error Mitigation for Microprocessor in Bulk CMOS Technology", PhD thesis (2011)
[Intel 22nm] N. Seifert et. al, TNS, pp. 2666-2673 (2012)
[Intel 14nm] N. Seifert et. al, TNS, pp. 2570-2577 (2015)
[Samsung 10nm] M. Jin et. al., IEDM 15.1.1-15.1.4 (2016)

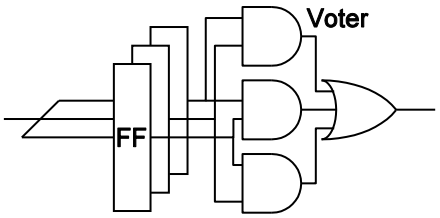
Soft Error Mitigation Techniques

- Architecture level
  - Dual lock-step for automotive and aerospac
- Circuit level
  - Parity and ECC (Error check code) for SRAM and DRAM
  - Majority voting for latches and flip flops
- Process/device level
  - FinFET/FDSOI To reduce # of carriers collected to drain
  - Epitaxial wafer to reduce resistance
  - As many well-taps as possible

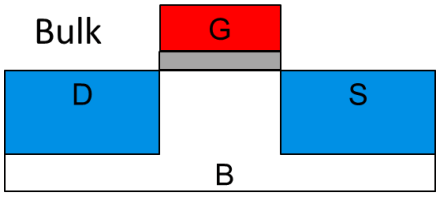


Dual lock-step

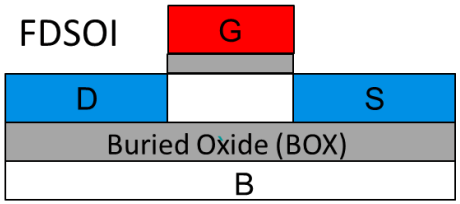
[M. Baleani, et al., CASES, 2013]



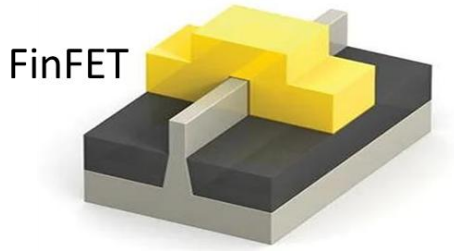
TMR FF



Cheap but leaky



Low power but expensive



High speed but very expensive

SBU/MBU Mitigation on SRAM

- Parity
  - Single Error Detect (SED) only for SBU (Single Bit Upset)

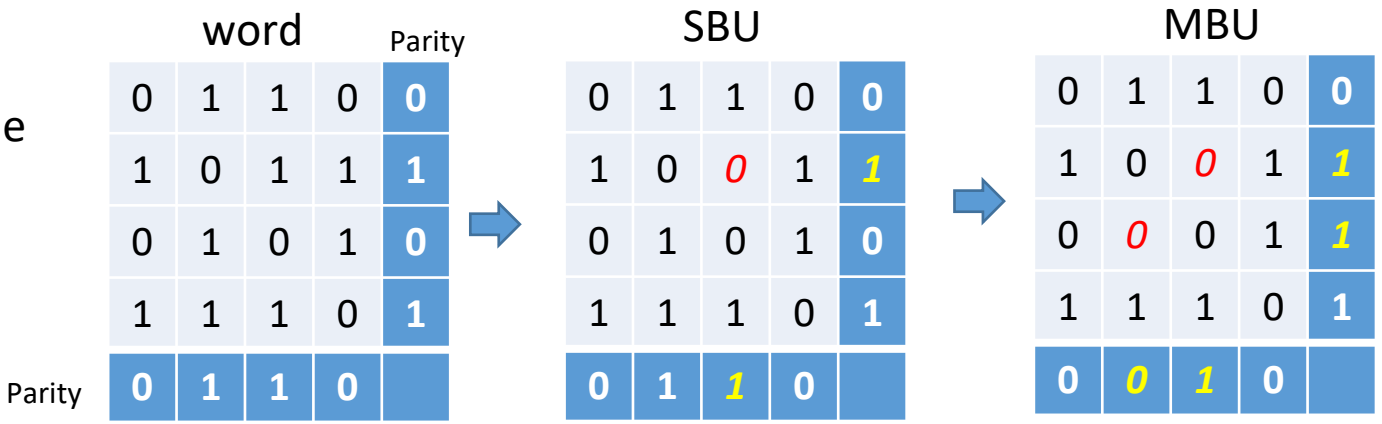
Exclusive OR

Parity = ^ word; 1= ^01011101 → 1≠ ^01001101

(Parity: 1, word: ^01011101 / ^01001101)

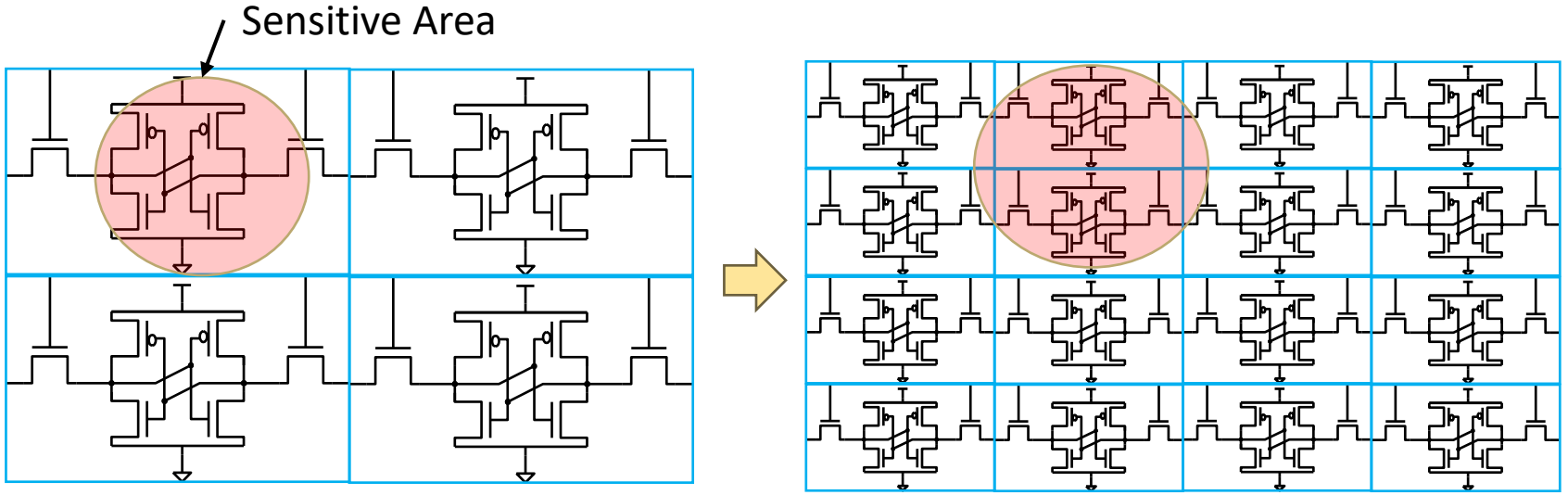
- ECC (Error Correction Code) for SBU and MBU (Multiple Bit Upset)
  - Single Error Correct and Double Error Detect (SEC-DED) for MBU

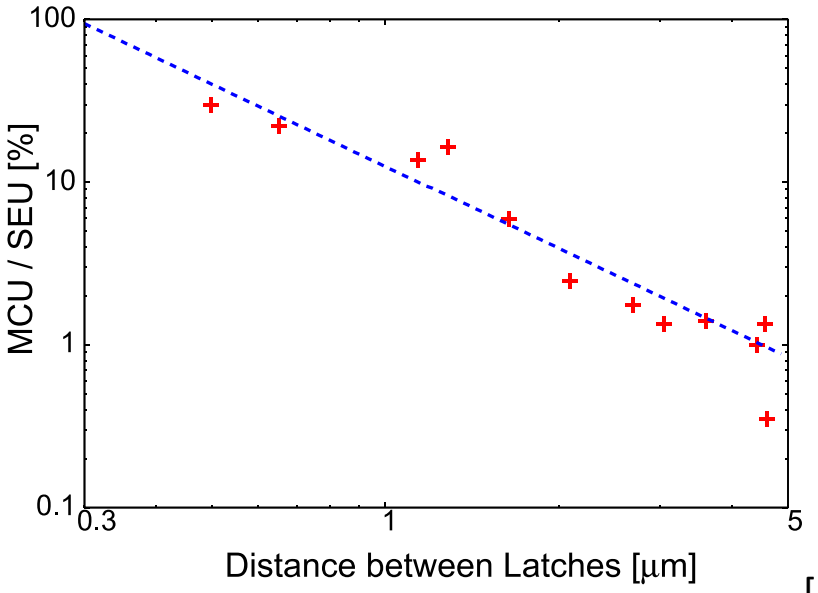
2D-Parity Code (16+8-bit)



MBU can be detected but not corrected by SEC-DED

MCU Rate Elevation by Scaling





- Sensitive area does not scale
  - Possibility to cause MCU is increased by scaling
- Redundancy is not effective on scaled process nodes
- Interleaving must be adopted to eliminate MBU on SRAM

[J. Furuta et al., IRPS, 6C.3.1-6C.3.4, 2013]

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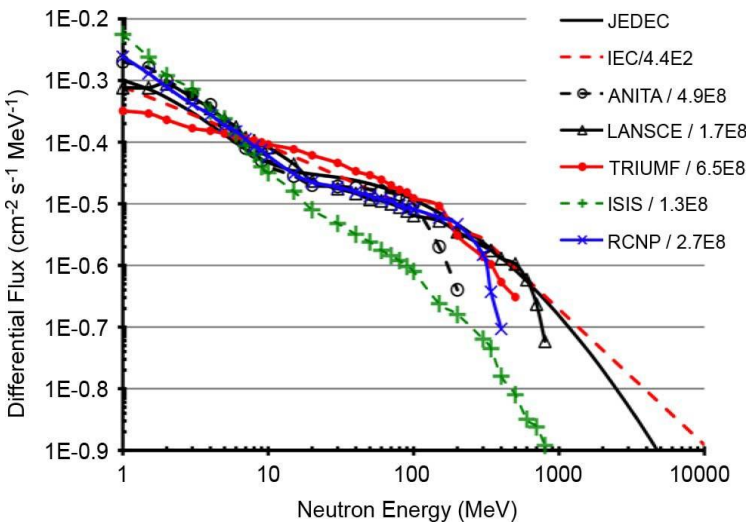
How to Evaluate Soft Errors

- Simulation
  - Circuit Simulation
    - Logic gate, SRAM, latch, flip-flops
  - Device Simulation
    - Discrete MOSFET, logic gate, SRAM or latch
  - Logic Simulation
    - Transient or static simulation by fault injection
- Measurement
  - Accelerated test
    - α Particle, Neutron, Heavy ion and Muon
  - Field test
    - High altitude for higher neutron flux
    - Underground for lower neutron flux

White Neutron Irradiation Test

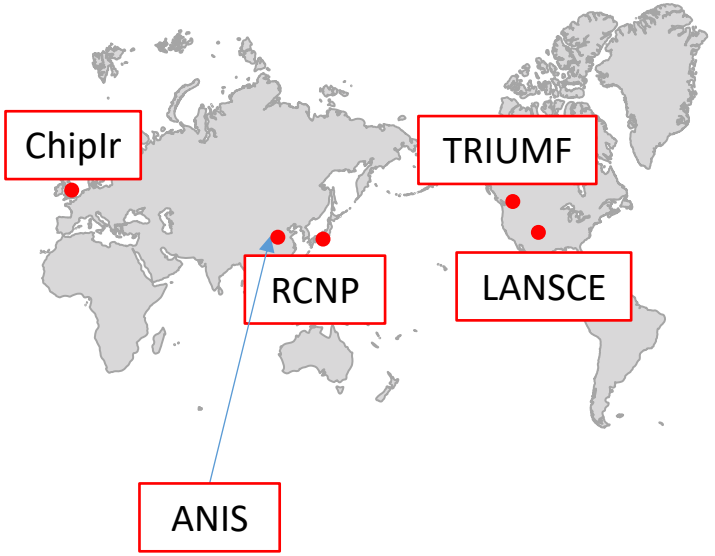
- Accelerator must be used
  - White (spallation) neutron: similar energy spectrum at sea level
    - Acceleration factor is ~4x10^8 RCNP (1s. irrad. 10y. at sea level)
  - Lots of DUTs must be prepared
    - 1000 FIT/Mbit == 2500 errors/Mbit in 1 day irradiation
    - A few errors on radiation-hard (rad-hard) storage cells

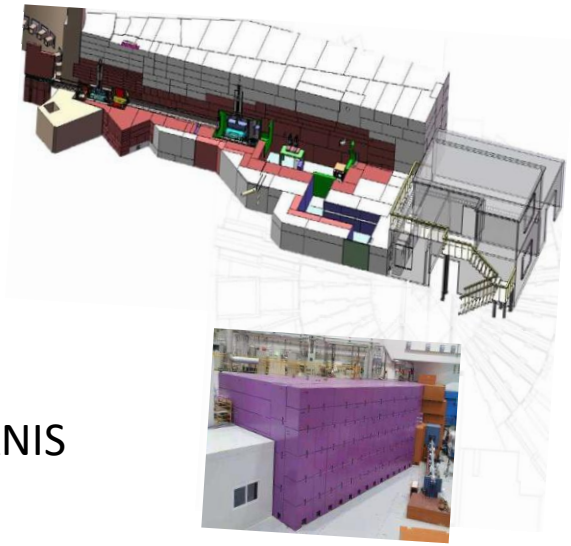


[C. Slayman, TNS 2010]

White Neutron Facility around the World

- High-energy neutrons are a major factor in soft-errors in terrestrial environments.
- Only four + one facilities offer white neutron beams for acceleration tests around the world.
- In 2022, ANIS in China started to be operated.





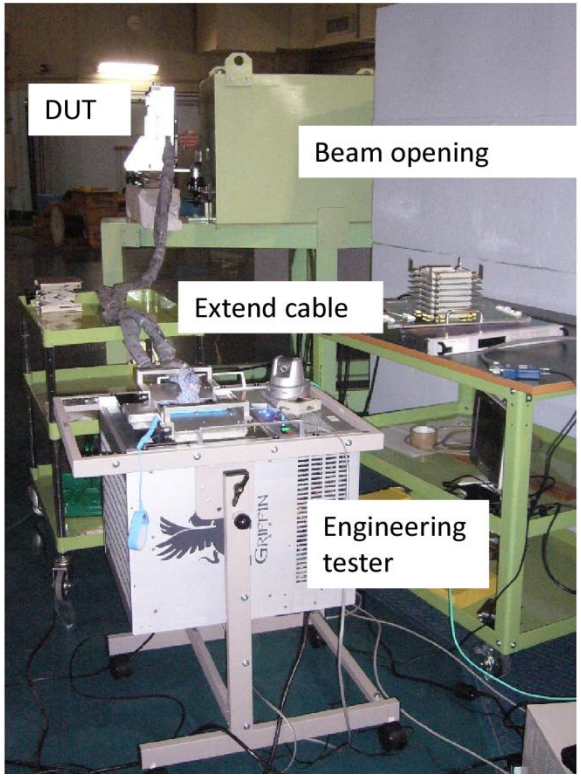
ANIS

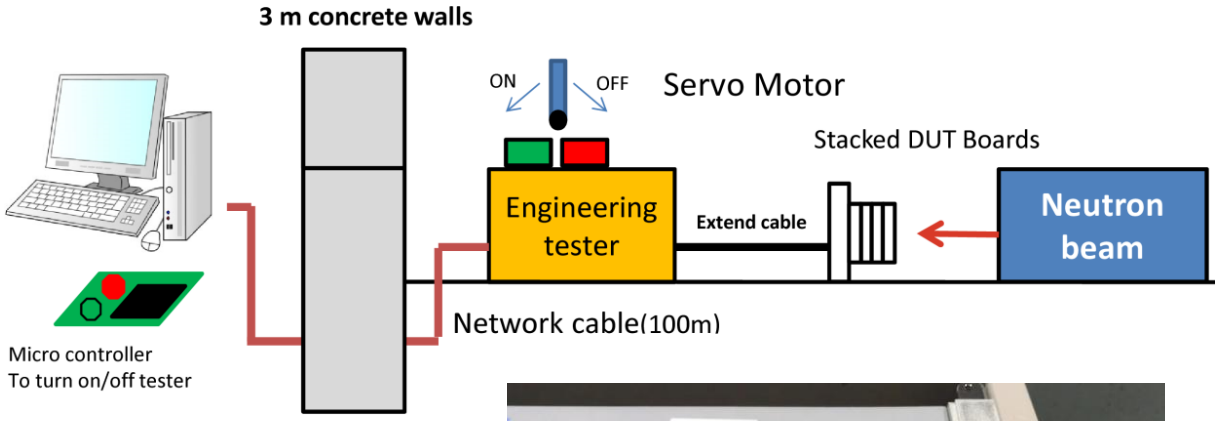
Large area beam (70x70m^2)

	Flux (cm^{-2} s^{-1}) >10MeV	Energy (MeV)
LANSCE	1-2x10^6	800
TRIUMF	2-3x10^6	400
RCNP	7x10^5	480
~~TSL-ANITA~~	~~9x10^5~~	~~180~~
ChipIr	5.4x10^6	**800**
ANIS	10^7	**1600**

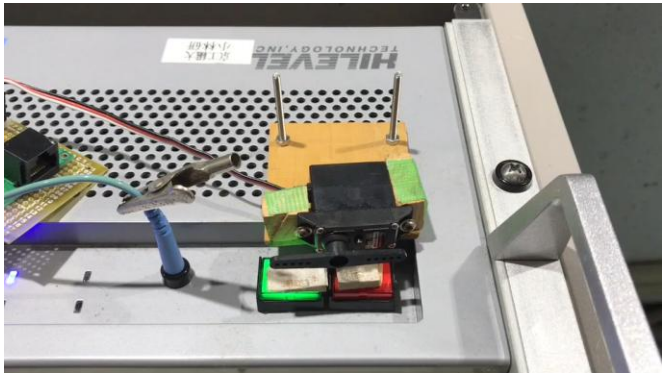
From RADECS 2024 Thermal Workshop

Neutron Test Setups





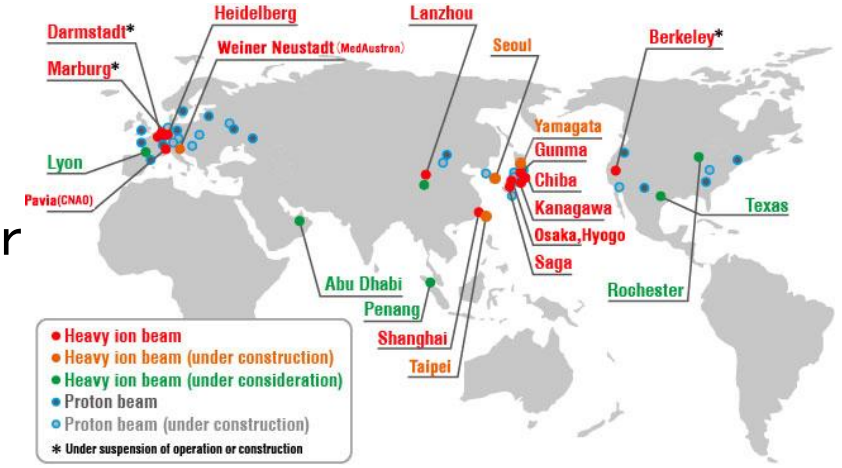
Remote – controlled servo motor (movie)



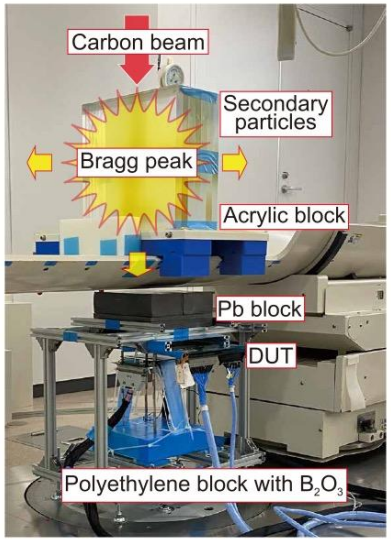
- Accelerated neutron is harmful to human body and test instruments
  - Humans must be outside beam room
  - Better to place PCs outside or protect them by Pb blocks.
  - Test instruments must be aside beam opening

Alternative White Neutron Source: Clinical Carbon Beam

- Clinical carbon beams are used for cancer therapy
- HIMAC (Heavy Ion Medical Accelerator in Chiba) is the world-first carbon beam facility
  - 7 carbon beam facilities are now available in Japan
  - Accelerator facilities are planned to be constructed around the world.
- When a carbon beam is irradiated onto an acrylic block, a large number of secondary particles are generated around the Bragg peak.
  - Secondary particles are Neutrons, protons, alpha particles
  - Generated neutrons are used for soft error evaluation tests.



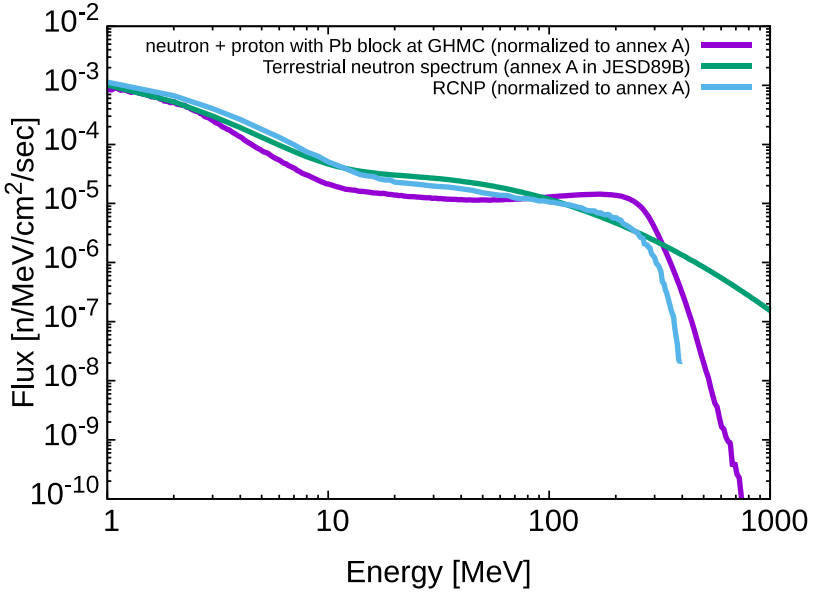
https://www.particle.or.jp/hirtjapan/en/medical/current/world.html



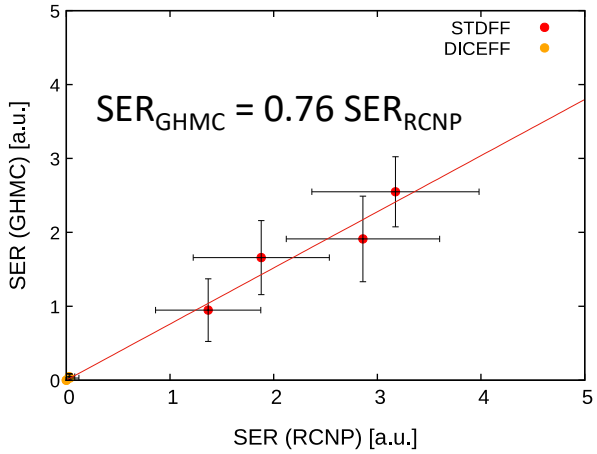
Neutron irradiation setup in a therapy room

Neutron Spectrum and Measurement Results

- Carbon beam at GHMC (Gunma Univ. Heavy Ion Medical Center)
  - Energy spectra are calculated by PHITS.
  - According to JESD89B, protons (> 50 MeV) can be used in place of equivalent energy neutrons.
  - Neutrons (> 10 MeV): 6.1x10^9 /cm^2/hour
  - Protons (> 50 MeV): 1.6x10^8 /cm^2/hour → Acceleration factor: 4.9x10^8
  - RCNP (white neutron beam):
    - Acceleration factor: 1.6x10^8
- Correlation coefficient between the SERs from RCNP and GHMC is 0.99
  - Error rates of GHMC are 24% less than RCNP



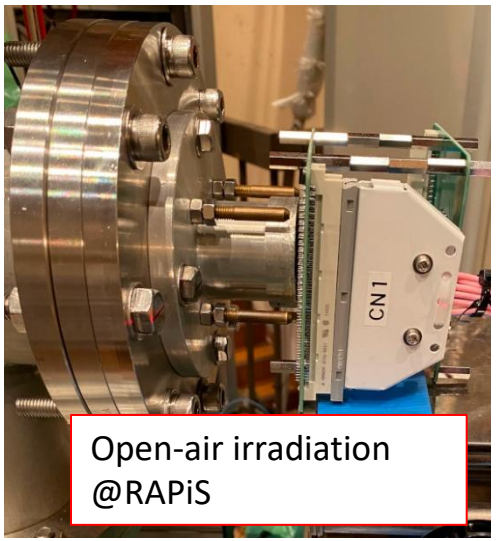
The terrestrial neutron spectrum in JESD89B (12.96 n/cm^2 · hour).



Heavy-Ion Irradiation

- For outer space application
- Accelerator must be used
  - TIARA/HIMAC @ QST, RARiS (CYRIC) @ Tohoku U. , RIBF@RIKEN
  - TIARA, RAPiS provide “Cocktail beam”
- Better to put DUT in vacuum chamber to keep heavy ion energy

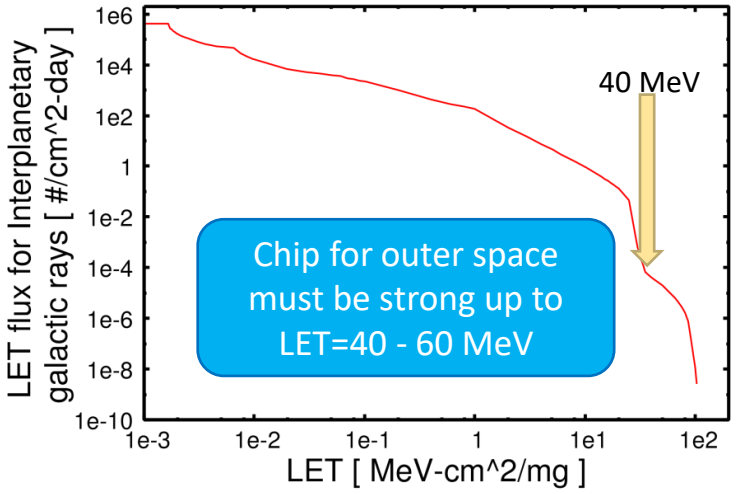
Vacuum chamber irradiation @TIARA



Open-air irradiation @RAPiS

Ions	LET [MeV/ (mg/cm²)]	Energy [MeV]
N	3.4	56
Ne	6.6	75
Ar	16	150
Kr	40	322
Xe	64	454

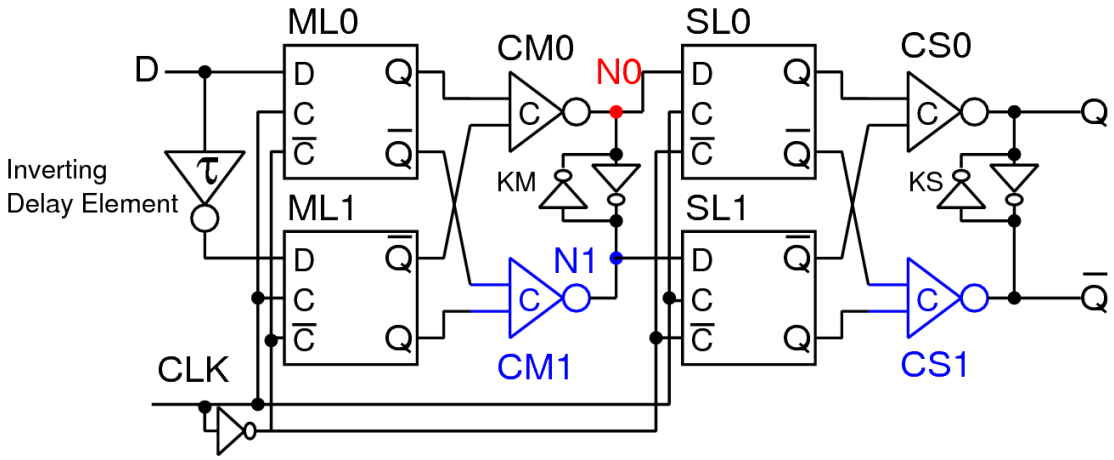
Heavy ions at TIARA



Outline

- Reliability issues in Si-based semiconductor chips
- Soft errors
  - What is soft error?
  - Mitigation techniques
- How to evaluate soft errors
  - Acceleration tests by using beam facilities
    - White neutron
    - Clinical carbon beam
    - Heavy ions
- Radiation-hard flip-flop
- Conclusion

BCDMR FF [Furuta et.al, VLSI Cir. 2010]

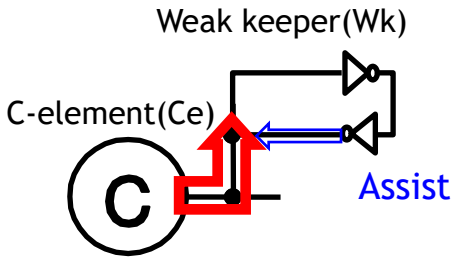


	Area	Delay	Power
BISER	3.00	1.47	2.15
BCDMR	3.00	1.45	2.20

Normalized by Standard FF

BISER: Radiation-hard FF developed by Intel/Stanford

- Bistable Cross-coupled Dual Modular Redundancy FF
  - Strong against an SET pulse from C-element
  - Duplicated C-elements strongly assists to keep correct data. No area-overhead because of smaller transistors on C-elements



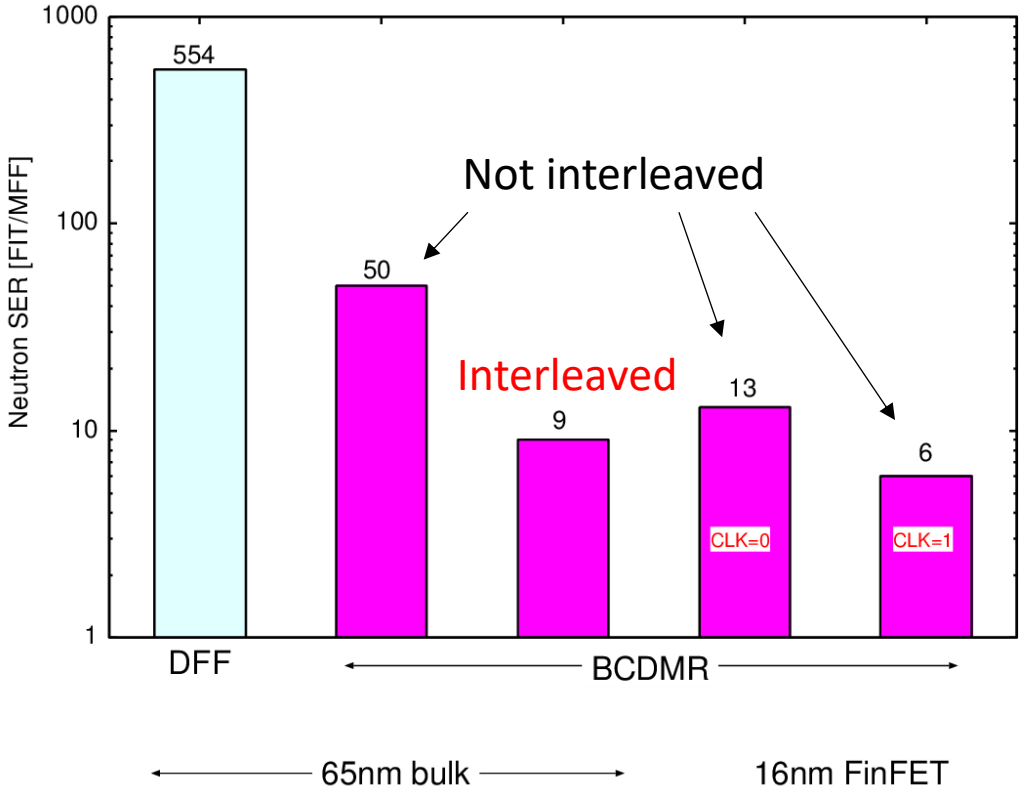
Drive strength Ce : Wk = 10 : 1

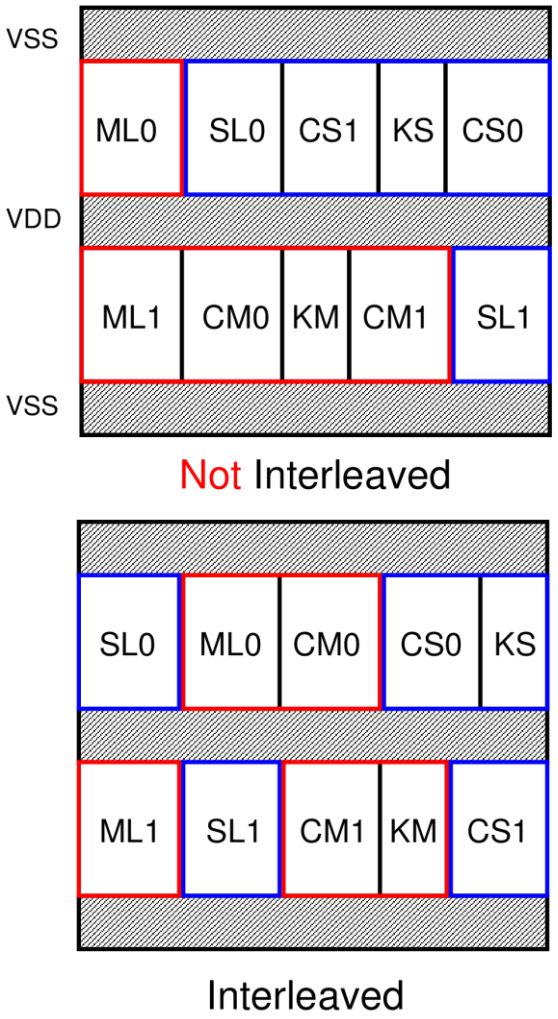
BISER

BCDMR

Ce : Sk = 5 : 2

Interleaved Layout for Scaled Tech. Node





- Similar SERs b/w 65nm interleaved and 16nm not-interleaved BCDMR
  - Interleaved layout decreases SER

[K. Kobayashi, et. al. IRPS 2017]

Place redundant storage cells as far apart as possible

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Conclusion

- Semiconductor chips for automotive, aerospace, HPC etc. must be reliable.
- Soft error is a temporal failure caused by a radiation particle
  - Alpha particles, Neutrons are main sources at the ground level
  - Heavy ions are main sources in the outer space
  - Only five neutron facilities around the world
  - Clinical carbon beams can be used for an alternative neutron source
- Redundancy is used to protect storage cells against soft errors
  - ECC is for DRAM and SRAM, while majority voting for flip flops.
  - We have designed many types of radiation-hard flip-flops.

Acknowledgement

- All members of our VLSI-system Lab. in KIT.

2009

2023

- d.lab VDEC in Univ. of Tokyo for chip fabrication and EDA support
- All corporate collaborators

Quantum Computer

QUBECS
Quantum Bit Error Correction System
Moonshot Target 6

Moonshot Goal 6

"Development of Scalable Highly Integrated Quantum Bit Error Correction System"

Moonshot Goal 6 QUBECS: Quantum Bit Error Correction System

* Moonshot International Symposium for Goal 6 held at April 23, 2021 (Public video site)
*

Project Manager: Kazutoshi Kobayashi

Professor, Dept. of Electronics, Graduate School of Science and Technology, Kyoto Institute of Technology
Director, Kyoto Lab for a Greener Future, Kyoto Institute of Technology

京都工芸繊維大学
KYOTO INSTITUTE OF TECHNOLOGY