Implementation and Evaluation of a Cryogenic DSP in 22-nm with Floating-Point Arithmetic for Estimating Qubit States

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***Abstract*—Recent advancements in quantum computing have emphasized the need for scalable quantum–classical interfaces (QC-IFs) capable of controlling a huge number of qubits efficiently. Conventional QC-IFs, implemented at room temperature, face wiring and thermal challenges that limit system scalability as the number of qubits increases. To address these issues, we propose a cryogenic digital signal processor (DSP) architecture capable of performing qubit readout and control operations inside the dilution refrigerator. We implemented the DSP which replaced wide fixed-point operations by floating-point ones in a previous study. An ASIC was fabricated using a 22-nm CMOS bulk process. Compared with the previous study, power consumption and area increased at room temperature due to additional circuits. We conducted a leakage power analysis on this design based on transistor leakage characteristics at 25 °C and −73 °C. The results demonstrated a reduction of 96.6 % compared to leakage power at 25 °C. These results demonstrate the feasibility of low-power, compact control electronics for future Cryo-CMOS control SoCs and fault-tolerant quantum computing systems.**

***Index Terms*—CMOS, cryogenic, DSP, low-power, quantum computing**

I. INTRODUCTION

Quantum computers are implemented using quantum mechanics, a computational theory that differs from conventional classical computers [1], and are expected to accelerate a variety of fields, including quantum simulations and model optimizations [2]. Quantum computing is being actively researched by many organizations, including major technology companies, as a next-generation large-scale computing platform [3] [4]. To realize practical systems, many qubits must be controlled and measured with high precision, which requires an efficient quantum–classical interface (QC-IF). According to IBM's published roadmap, quantum computer systems with over 2,000 logical qubits are expected to be implemented by 2030s [5]. Achieving this goal requires increasing the number of physical qubits by more than three orders of magnitude compared with the current level. However, in existing quantum computers, the QC-IF is located at room temperature, and each qubit inside the dilution refrigerator is connected through dedicated wiring. The number of these connections scales linearly with the number of qubits, resulting in a larger control system and a dilution refrigerator with more powerful cooling capacity. Therefore, miniaturization and low-power implementation of control electronics is a key to scaling up quantum computers. We aim to develop a digital signal processor (DSP) for quantum control that can operate under cryogenic environments. By executing a part of the signal processing inside the dilution refrigerator, the number of control wires between room and cryogenic temperatures can be reduced, improving the scalability of the entire system [6]. In designing such cryogenic DSPs, one of the major challenges is the power budget per qubit imposed by the refrigerator. Thus, the signal processing for quantum control must achieve low power consumption while maintaining high data rates and low latency. We focus on a DSP module to determine the logical state of qubits for the fault-tolerant quantum computing (FTQC)–oriented QC-IF proposed in our researches [7] and [8], which are our previous works focusing on FPGA implementation and architectural proposals. While previous studies were limited to FPGA implementations or simulation-based verifications, this work clarifies the feasibility of ASIC implementation and power characteristics in low-temperature environments through the fabrication of a test chip. In this work, we evaluate the effect of replacing the arithmetic representation of data signals in key computational blocks with more efficient numerical forms and their behavior in cryogenic environments.

II. BACKGROUND

Fig. 1 shows the block diagram of the signal-processing circuit targeted in this study. It is used for read-out of

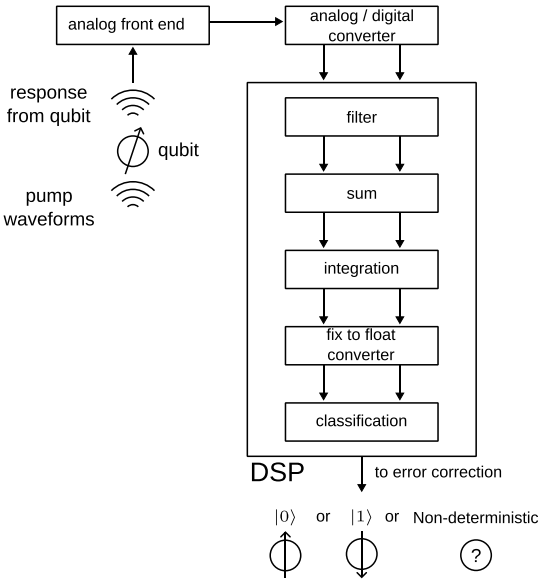


Fig. 1. Digital control architecture

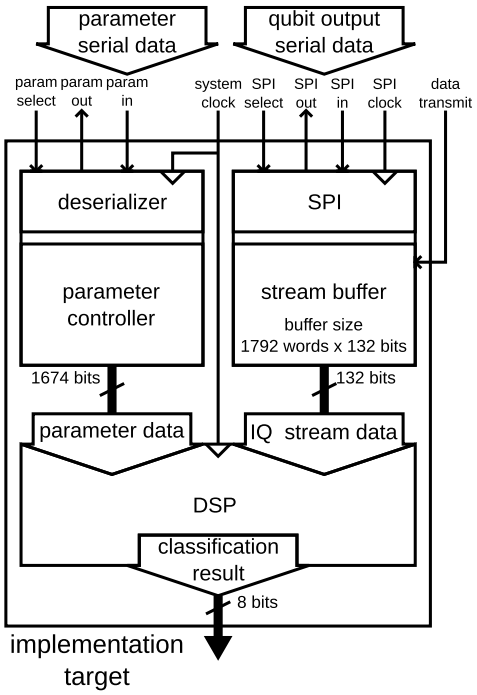


Fig. 2. Chip implementation architecture of the proposed DSP

qubits proposed in [7], [8]. The reflected microwave from a qubit is down-converted by the analog front-end, digitized by the analog to digital converter (ADC), and input to the DSP as a stream of complex IQ data. Inside the DSP, the signal passes through a sequence of processing blocks—low-pass filtering, summation, integration, and classification to estimate the quantum state ($|0\rangle$, $|1\rangle$, or indeterminate). In existing FPGA implementations, all data are represented in a fixed-point format to ensure high computational accuracy and to avoid rounding errors. Consequently, bit widths expand with each stage: the inputs have 16 bit real and imaginary components, the filter and sum output are 89 and 101 bit respectively, and the internal and output data of the integration reach 121 bit. The integration block also requires storing more than 1,000 words of intermediate data, leading to the use of large static random access memories (SRAMs) that dominate the overall power and area of the DSP. To address this issue, [8] proposed converting fixed-point data to the single-precision floating-point format before integration and implementing the integration unit using floating-point arithmetic operations. This conversion compresses 121 bit signals to 32 bit, reducing memory bit widths while maintaining output accuracy. Although the area reduction has been confirmed in the previous research, the impact of the cryogenic environment in actual implementation has not been verified. In this study, we implement the single-precision floating-point version of the DSP on a chip and quantitatively evaluate the power and area of the digital circuit in a 22-nm CMOS bulk process at cryogenic temperatures.

III. RELATED WORK

This work builds upon the DSP architecture proposed in [8] and focuses on experimentally validating the previously introduced arithmetic-format conversion through an actual chip implementation. Ref. [8] extensively evaluated the power reduction at the preliminary place and route (PnR) stage, logical equivalence, and demonstrated that the floating-point implementation maintains comparable estimation fidelity to the fixed-point baseline despite the significant data compression. However, the operating characteristics in low-temperature environments were not addressed. This paper fills this gap by validating the effectiveness of the circuit improvements and evaluating the performance in a real environment using fabricated chips, which cannot be fully captured by simulations alone. Furthermore, to improve the accuracy of the power analysis, we estimate leak current derived from low-temperature transistor characteristics to evaluate power consumption within the target temperature range. The results obtained in this study provide effective guidelines for achieving low power consumption and ensuring reliability in the design of future Cryo-CMOS control SoCs and quantum-control DSPs.

IV. TARGET SIGNAL PROCESSING

The actual implementation was performed on the circuit block shown in Fig. 2. In addition to the DSP circuit, data input interface was integrated for verification. The qubit waveform data are supplied by an on-chip emulator composed of a Serial Peripheral Interface (SPI) and a stream buffer memory, which is designed to emulate the signal stream from an ADC. Emulated data is written to stream buffer via SPI, and the data stored in the stream buffer are transferred to the DSP at 33 Gb/s by triggering data transmit. In addition, the parameters are loaded into each module in the DSP through the deserializer and the parameter controller. The newly added features are introduced to overcome the constraints arising from the limitations of the number of measurement terminals

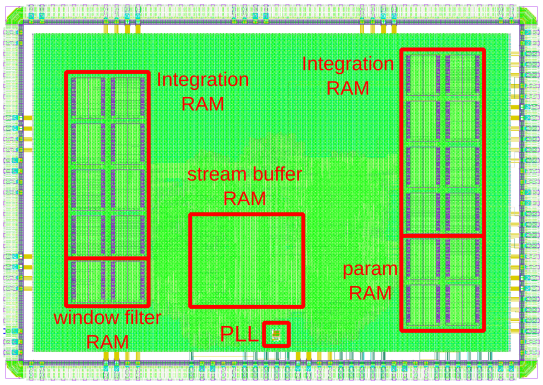
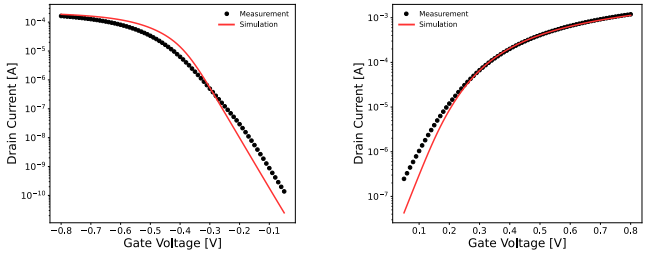


Fig. 3. Chip layout



(a) PMOS (b) NMOS

Fig. 4. Transistor characteristics at $|V_{\mathrm{DS}}| = 0.8\,\mathrm{V}$

and signal speed, thereby enabling both practical measurement and operation at the nominal speed.

V. IMPLEMENTATION RESULTS

Logic synthesis was carried out using Synopsys Design Compiler with the DesignWare library and a custom-designed SRAM for cryogenic operation. IC Compiler II was employed for PnR and power estimation. Fig. 3 is the fabricated layout after PnR, targeting 25 °C. The red box indicates the implemented SRAM and the PLL for clock supply. I/O terminals are located at the periphery, while the core logic is implemented in the remaining area. Table I shows area and power consumption of both implementations in [8] and this work. Power analysis was performed using IC Compiler II on the post-PnR layout, utilizing a 22-nm standard cell library and wire load models. Compared to [8], this work shows an area increase of 0.33 µm^2 and a total power increase of 25 mW. The area and power increase at 25 °C are due to the additional SPI, stream buffers and the clocking phase locked loop. Although power estimation at low temperatures falls outside the standard model's scope, we estimated power consumption by calculating the deviation between the model and actual measurements using the transistor test element group (TEG) characteristics shown in Fig. 4. In the figure, the red solid lines represent the measured values, while the black dashed lines represent the post-layout simulation values with parasitic components extracted. Since this study estimates OFF-leakage characteristics based solely on the OFF-region properties, the ON-region characteristics are not discussed here. Regarding the characteristics in the transistor's OFF region (high $V_{\mathrm{DS}} = 0.8\,\mathrm{V}$, low $V_{\mathrm{GS}} = 0.05\,\mathrm{V}$), for PMOS, the measured value was −21.6 nA and the simulated value was −5.55 nA, while for NMOS, the measured value was 247 nA and the simulated value was 42.8 nA. Based on these measurements, averaging the NMOS and PMOS results revealed that the current flow is 5.36 times higher than that predicted by the transistor model. Table I presents the leakage power corrected using this relationship. Based on these results, the leakage power at −73 °C decreased by 96.6 % compared to room temperature. At 4 K, the leakage power is expected to be even lower than the result obtained at −73 °C.

TABLE I
AREA AND POWER CONSUMPTION

	Temp [°C]	Area [µm^2]	Dynamic [mW]	Leakage [µW]	Total [mW]
Reference (Exclude IF*)	25	1.62	-	-	160
This work (Include IF*)	25	1.95	133	52,400	185
	−73	1.95	129	331	129
	−73**	1.95	129	1,760	131

* IF means Interface.
**Corrected based on leakage characteristics.

VI. CONCLUSION

Toward the realization of large-scale quantum computers, we aim to develop a chip to estimate qubit states that can operate in cryogenic environments. To achieve this, it is necessary to implement a chip with low power consumption and small area. In this paper, we implemented a DSP that uses single-precision floating-point numbers as the internal representation to construct control integrated circuits. The prototype was fabricated using a 22-nm bulk process. Logic synthesis was performed with Synopsys Design Compiler, followed by place and route using Synopsys IC Compiler II. Through this implementation, we designed a chip in 1.95 mm^2 area and consumes 185 mW of power at 25 °C and 131 mW at −73 °C. The power analysis at −73 °C is estimated based on measured values from the transistor TEG. The leakage power strongly depends on temperature, decreasing by 96.6 % from 52.4 mW at 25 °C to 1.76 mW at −73 °C. The proportion of total power accounted for by leakage decreased from 28.3 % at 25 °C to 1.34 % at −73 °C. In the target 4 K environment, leakage power is expected to be further reduced. However, a limitation of this study is that it relies on measurements from a single transistor TEG, without accounting for process variations in transistor characteristics. In future work, we plan to verify simulation predictions against actual measurements using the fabricated chip. By clarifying the degree of leakage power reduction, we aim to provide deeper insights into guidelines for power estimation in cryogenic environments.

ACKNOWLEDGMENT

This work is supported by JST Moonshot R&D Grant Number JPMJMS226A. This work was also supported through the activities of VDEC, d.lab, The University of Tokyo, in

collaboration with Cadence Design Systems, NIHON SYNOPSYS G.K, and Siemens Electronic Design Automation Japan K.K.

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