# IRPSFF: Improved Recovery-Path Structured Flip-Flop for Enhanced Soft-error Tolerance with Low Performance Overhead in a 65-nm FD-SOI process

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***Abstract*—We propose a radiation-hardened flip-flop (FF) suitable for FD-SOI processes. It integrates a reduce-sensitive-range (RSR)-based secondary latch and a pass-transistor delay in the feedback-recovery path to improve soft-error tolerance without increasing performance overheads. The target delay for the recovery path was determined based on a sigmoid approximation of prior experimental data to ensure robustness against long Single-Event Transient pulses. Post-layout simulation and Xe-ion irradiation results show that the proposed FF achieves approximately 2x higher soft-error tolerance than the conventional stacked FF, while maintaining low area, delay, and power overheads comparable to those of the Dual Feedback Recovery FF.**

***Index Terms*—soft-error, heavy ion, flip-flop, FD-SOI**

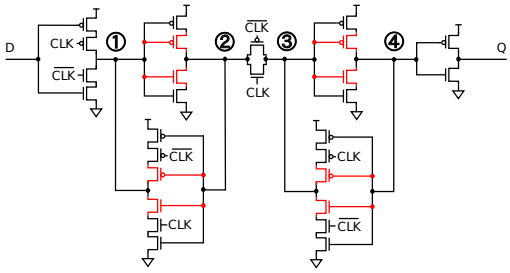



Fig. 1. Stacked FF. The red colored transistors and wires are added to the standard FF. The transistors that consist inverters in each latch are stacked.

## I. Introduction

Fully-depleted silicon-on-insulator (FD-SOI) process effectively mitigates Single-Event Effects, as the buried oxide layer suppresses charge collection caused by radiation strikes. According to Ref. [1], [2], [3], FD-SOI process has around 10-100x higher soft-error tolerance than the bulk process. However, Single-Event Upsets (SEUs) still occur in storage elements such as flip-flops (FFs) and SRAMs due to parasitic bipolar effects (PBEs) [3]. Therefore, circuit-level hardening is essential for mission-critical applications [4].

Several radiation-hardened FFs suitable for FD-SOI have been proposed. Stacked FF in Fig. 1 adopts a stacked transistor structure [5] to suppress PBEs, providing high robustness but large delay overhead. Dual Feedback Recovery FF (DFRFF) [6] in Fig. 2 uses a guard-gate (GG) structure [7] to filter out short Single-Event Transient (SET) pulses, achieving small propagation delay from input to output. However, under high-LET (Linear Energy Transfer) conditions, long SET pulses are frequently generated, and the GG delay in DFRFF is insufficient to suppress such long pulses [8]. To address this issue, DFRFF with long delay (DFRFFLD) in Fig. 3 has been proposed [9]. DFRFFLD increases the GG delay by adding two inverters as delay elements. However, in the Secondary Latch (SL), the GG delay remains insufficient, resulting in the soft-error tolerance of only several times smaller than that of Standard FF. Further increasing the GG delay using an approach similar to that of DFRFFLD leads to increased area and power overheads.

We propose the Improved Recovery-Path Structured FF (IRPSFF), achieving high soft-error tolerance with low delay, area, and power overheads. To ensure robustness against long SET pulses, we establish a target recovery-path delay using a sigmoid approximation of prior experimental data. Based on this target, the IRPSFF enhances the guard-gate delay in the primary latch using a pass-transistor-based structure, while the secondary latch employs a reduce-sensitive-range (RSR) inverter and a stacked inverter instead of the GG structure. The design was validated through Xe-ion irradiation at an LET

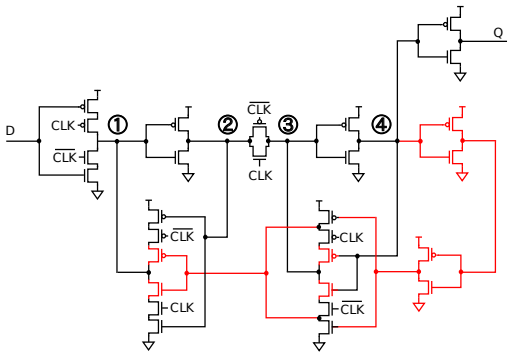



Fig. 2. DFRFF. The red-colored transistors and wires are added to the standard FF. GG structures are used in each latch.

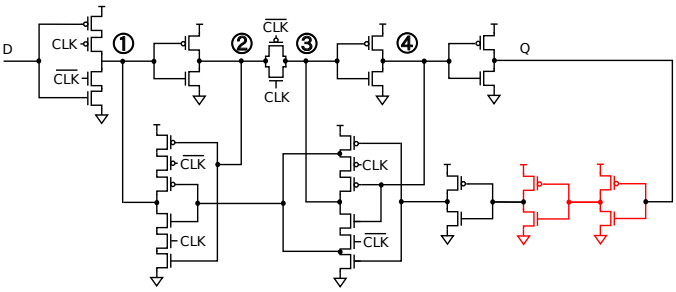



Fig. 3. DFRFFLD. The red-colored transistors and wires are added to the DFRFF. GG structures are used in each latch.

of $69.3\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$, demonstrating superior tolerance with minimal performance overhead.

In this study, SET pulse generation is assumed to occur only in nMOS transistors. In FD-SOI, more than 89% of soft errors are reported to occur in nMOS transistors [10].

Section II explains the design target for GG delay, Section III explains the proposed FF, Section IV presents results, and Section V concludes this paper.

## II. Analysis and Design Target for Guard-Gate Delay

In FD-SOI processes, the GG structure effectively suppresses SET pulses. Fig. 4 shows the schematic of the GG structure to clarify the operating principle. The GG structure has a delay element to filter out SET pulses with widths shorter than the delay duration. However, conventional GG designs

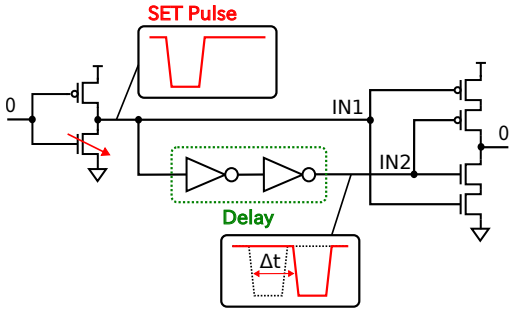



Fig. 4. Schematic of the GG structure. The delay element filters out SET pulses that are narrower than the delay duration.

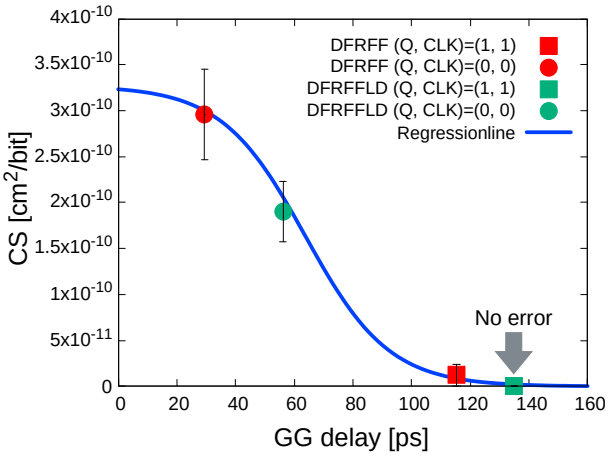



Fig. 5. Comparison between the GG delay and CS under Kr-ion irradiation in a 65 nm FD-SOI process. Note that the simulated GG delay values are approximately 10 ps different from those reported in Ref. [9] due to an update of the SPICE model.

in Ref. [8] and [9] cannot sufficiently suppress long SET pulses induced by high-LET heavy ions. Therefore, this study reanalyzes the relationship between GG delay and soft-error tolerance. The objective is to establish a design guideline for the GG delay in the proposed FF.

In our previous study [9], we evaluated the SEU cross-section (CS) of DFRFF and a DFRFFLD under Kr-ion irradiation. Ref. [9] described the relationship between CS and GG delay using a linear approximation. However, SET pulses have a distribution in pulse width, and soft errors occur only when the SET pulse width exceeds the GG delay. Therefore, the CS for a given GG delay is given by the cumulative rate of SET pulses with pulse widths longer than GG delay. In Ref. [11], such cumulative SET rates were fitted using a sigmoid function. Accordingly, the CS-GG delay relationship corresponds to the cumulative distribution of SET pulse widths, rather than a linear dependence on the GG delay.

Fig. 5 shows the sigmoid approximation of the CS-GG delay relationship, and the approximation function is given in Eq. (1).

$$\mathrm{CS}\,[\mathrm{cm}^2/\mathrm{bit}] = \frac{3.27\times10^{-10}}{1+\exp\{0.07\times(\mathrm{GGdelay}\,[\mathrm{ps}]-63.8)\}}. \quad (1)$$

As shown in Fig. 5, this relationship yields a GG delay of 137 ps to achieve $2\times10^{-12}\,\mathrm{cm}^2/\mathrm{bit}$ under Kr-ion irradiation. This target CS value was selected based on a previously reported Stacked FF implemented in the same 65 nm FD-SOI process [12]. Although no errors were observed in Ref. [12], the upper bound of the confidence interval corresponded to $2\times10^{-12}\,\mathrm{cm}^2/\mathrm{bit}$, which was therefore adopted as the design target in this work.

The GG delay derived under Kr-ion irradiation should be evaluated for applicability to high-LET space environments. For space applications, tolerance against heavy ions with LET exceeding $60\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$ is required [13]. In FD-SOI, SET pulse width increases with LET. Under Xe-ion irradiation (LET $=$ $68\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$), SET pulses are

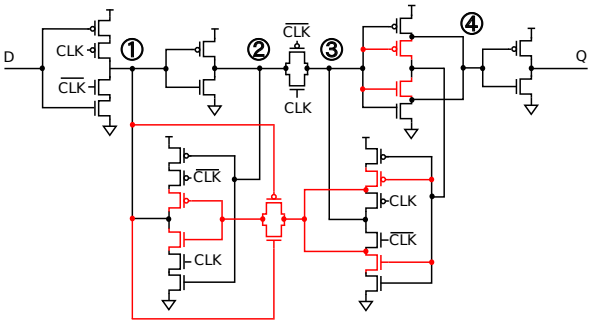



Fig. 6. Proposed FF: IRPSFF. The red-colored transistors and wires are added to the standard FF. GG structure is used in primary latch and RSR structure is used in the secondary latch.

approximately 1.2 times longer than under Kr-ion irradiation (LET $= 40\,\mathrm{MeV}\cdot\mathrm{cm}^2/\mathrm{mg}$) [14]. Ideally, Eq. (1) should be generalized to include LET as a variable. However, since measurements were not conducted at other LETs, the LET dependence of the equation cannot be determined. Therefore, we estimated the target for Xe-ions simply by scaling the required delay for Kr-ions (137 ps) by 1.2. By this calculation, a target GG delay of 165 ps was derived. However, implementing the GG delay in the same manner as a conventional DFRFFLD incurs significant area and power overhead. Therefore, a new circuit architecture, termed IRPSFF, is proposed in the next section.

## III. Proposed FF

This section explains the design concept of the IRPSFF in Fig. 6 and evaluates its circuit performance against other hardened FFs.

### A. Circuit Features and Design Updates

The IRPSFF is based on the conventional DFRFF structure. Two major updates are introduced to improve soft-error tolerance while maintaining low delay overhead.

*1) Secondary Latch Modification (RSR Structure):* In the DFRFF, the secondary latch adopts a GG structure to filter out short SET pulses. However, under high-LET conditions, long SET pulses cannot be fully suppressed by the conventional GG structure. Adding delay elements to the GG path can mitigate them, but it increases area and power overhead. The IRPSFF replaces the GG-based secondary latch with a combination of a reduce-sensitive-range (RSR) inverter [15][16] and a stacked inverter. The schematic of the RSR structure is shown in Fig. 7. This structure promotes charge recombination through the shared diffusion, suppressing an output flip and improving soft-error tolerance [16]. The inverter on the D-Q signal path adopts the RSR structure. As shown in Fig. 8, the internal node of the RSR inverter is connected to the output inverter, which reduces delay overhead.

*2) Primary Latch Modification (Guard-Gate Delay Enhancement):* To improve tolerance against long SET pulses, the GG path in the primary latch is revised. As shown in Fig. 9, pass-transistors are inserted as delay elements to increase the GG delay. In conventional FFs, the GG delay element typically

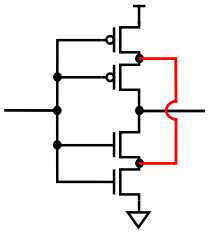
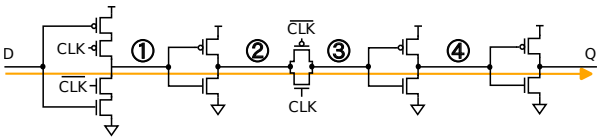
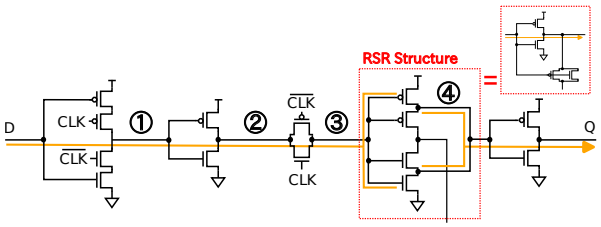


Fig. 7. Schematic of the Reduce-Sensitive-Range (RSR) structure. The shared diffusion area between the stacked transistors promotes charge recombination, thereby suppressing an output flip and improving soft-error tolerance.




(a) Standard FF.



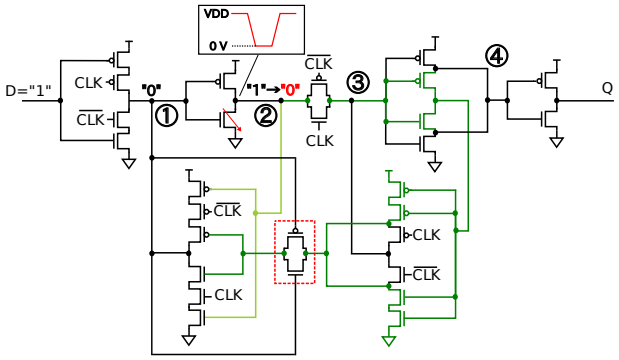

(b) IRPSFF.

Fig. 8. Signal paths from D to Q. The IRPSFF shown in (b) utilizes the RSR structure in the secondary latch. The internal node of RSR inverter is connected to output inverter, which enables to have the signal path configured with the same number of inverters as the standard FF.

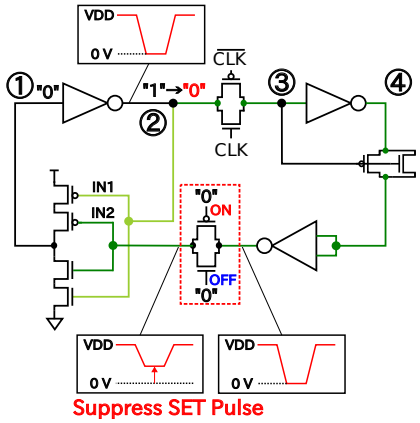
consists of an inverter or buffer. In contrast, the pass-transistors used in this design not only increase the GG delay but also attenuate the amplitude of SET pulses propagating through the GG path [17][18]. Each pass-transistor receives its input from node ①, which is the output of C-element. Because the C-element has a stacked structure, SET pulses are less likely to be generated in the C-element. As a result, node ① is relatively robust against SETs and serves as a reliable control signal for the pass-transistor. Circuit simulations yielded a 162 ps GG delay for the IRPSFF, which is over 40% longer than the DFRFF and close to the 165 ps target.

### B. Performance Evaluation

Post-layout simulations were performed and compared with other radiation-hardened FFs. Four types of FFs were designed and implemented on the same test chips fabricated in a 65 nm FD-SOI process. The number of FF stages per chip is summarized in Table I. Simulations were conducted at the standard supply voltage of 1.2 V, and the normalized results are summarized in Table II. Here, the CLK-Q delay represents the propagation time from the triggering clock edge to the output transition, and the D-Q delay is defined as the minimum time interval from the data input transition to the output transition. As shown in Table II, the setup time of the IRPSFF is approximately 2.5x that of the Standard FF. The increased




(a) Transistor-level schematic.




(b) Simplified logic gate representation.

Fig. 9. Mechanism of error mitigation by GG structure and pass-transistor in the IRPSFF. The green and lightgreen lines are the signal paths. The path with the green line makes GG delay that attenuates SET pulses. An on-state pass-transistor suppresses SET pulses.

TABLE I
THE NUMBER OF FF STAGES PER CHIP UTILIZED FOR THE MEASUREMENT.

| | # of FFs |
|---|---|
| Standard FF | 16560 |
| DFRFF | 25480 |
| Stacked FF | 25500 |
| IRPSFF | 25480 |

setup time is mainly caused by the added pass-transistor driven by node ①. This addition increases the load capacitance at node ①, resulting in a longer setup time. Fig. 10 shows the setup time and GG delay variations with different pass-transistor gate widths. Reducing the gate width decreases the load capacitance at node ①, leading to a shorter setup time. In contrast, the GG delay remains almost unchanged. Although a gate width of 200 nm was adopted in this design, reducing the gate width allows the setup time to be improved without increasing the GG delay.

Regarding delay characteristics, the CLK-Q delay of the IRPSFF is 9% smaller than that of the DFRFF. In contrast, the D-Q delay is 6% larger than that of the DFRFF. Compared with the Stacked FF, the IRPSFF achieves 35% smaller CLK-Q delay and 31% smaller D-Q delay. Thus, the delay overhead due to node reinforcement is locally suppressed. The area of the IRPSFF is equal to that of the DFRFF. Both static and dynamic power consumptions are lower than those of the DFRFF. Therefore, the proposed GG delay structure combining RSR and pass-transistors improves soft-error tolerance with low overhead.

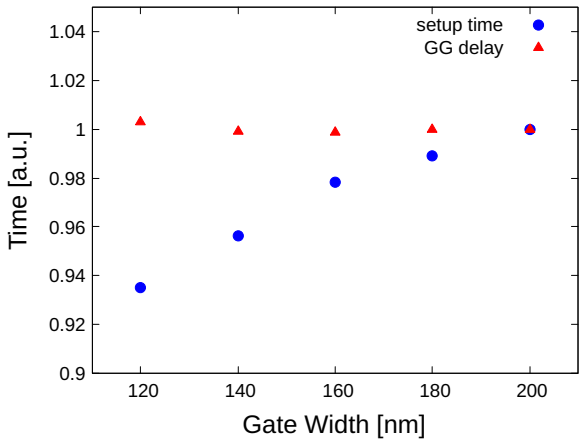



Fig. 10. Dependence of setup time and GG delay on pass-transistor gate width. The gate width used in this design is 200 nm.

## IV. Measurement Setup and Results

Heavy-ion irradiation tests were performed at RIKEN RI Beam Factory (RIBF) [19], using a Xe beam with an LET of 69.3 $\mathrm{MeV \cdot cm^2/mg}$. Irradiation was conducted under both normal incidence and a 45° tilt angle to investigate angular dependence of SEU sensitivity. Fig. 11 shows the experimental setups at RIBF. The total fluence was approximately $3.36 \times 10^8\,\mathrm{ions/cm^2}$. During irradiation, all FFs were initialized to the same logic state (All-0 or All-1). The supply voltage of the test chip was set to 1.2 V. The CS was calculated using Eq. (2).

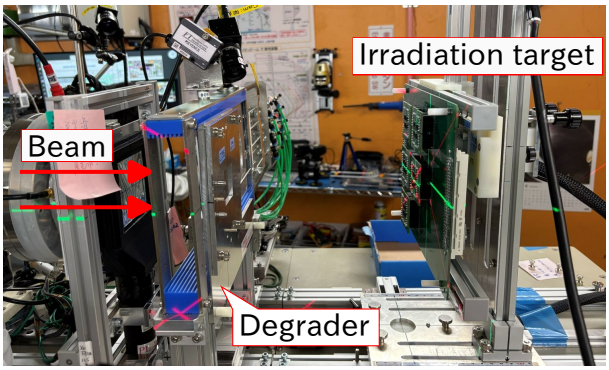
$$\mathrm{CS\,[cm^2/bit]} = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}} \times N_{\mathrm{ion}} \cos\theta}, \tag{2}$$

where $N_{\mathrm{error}}$ is the number of observed upset counts, $N_{\mathrm{FF}}$ is the number of FF stages, $N_{\mathrm{ion}}$ is the particle fluence, and $\theta$ is the irradiation angle [20].

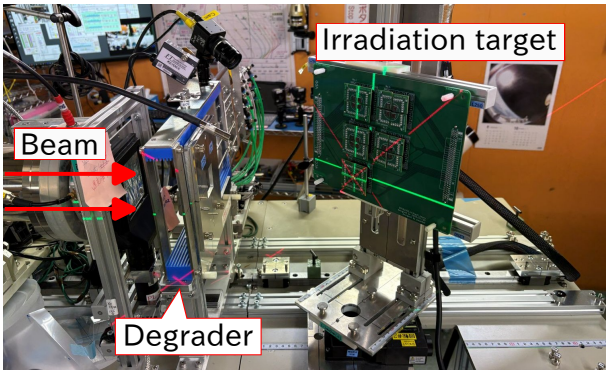
Fig. 12 shows the CSs of all FFs under four (Q, CLK) conditions at 0° and 45°. Under 0° condition, the IRPSFF achieved the smallest average CS, approximately 1/56 of the DFRFF and approximately one-third of the Stacked FF. When the angle was changed to 45°, the average CS increased by 1.03x for the DFRFF, 2.78x for the Stacked FF, and 4.17x for the IRPSFF. Nevertheless, SEUs occurred only at (Q, CLK) = (0, 1) for the Stacked FF and the IRPSFF. The errors observed at (Q, CLK) = (0, 1) originate from the input tristate inverter. If the C-element in the feedback path were the root cause, errors would also be expected in the secondary latch, where the C-element output is node ③. Because node ③ becomes vulnerable under the (Q, CLK) = (1, 0) condition, errors should appear at (Q, CLK) = (1, 0). However, no errors were observed

TABLE II
PERFORMANCE AND THE NUMBER OF TRANSISTORS OF IMPLEMENTED FFS. EACH PERFORMANCE VALUE IS NORMALIZED TO THOSE OF THE STANDARD FF.

| FF | # of Tr. | Area | Setup time | Hold time | CLK-Q delay | D-Q delay | Static power | Dynamic power |
|---|---|---|---|---|---|---|---|---|
| Standard FF | 20 | 1.00 | 1.00 | -1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| DFRFF | 28 | 1.29 | 1.26 | -1.49 | 1.21 | 1.20 | 1.16 | 1.12 |
| Stacked FF | 28 | 1.24 | 2.57 | -2.61 | 1.69 | 1.85 | 0.87 | 1.08 |
| IRPSFF | 28 | 1.29 | 2.59 | -2.63 | 1.10 | 1.28 | 1.00 | 1.10 |

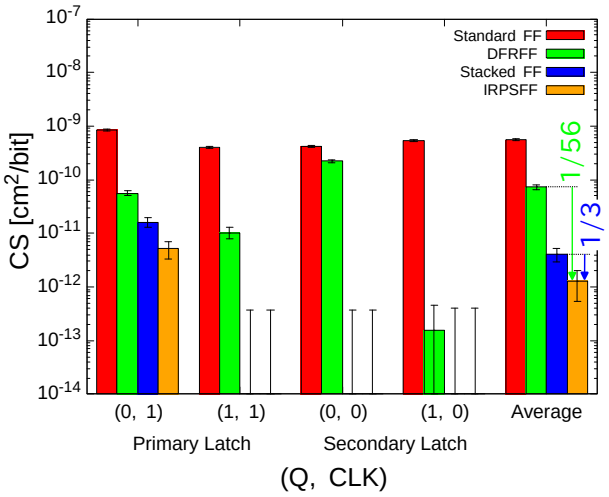



(a) Normal incidence.

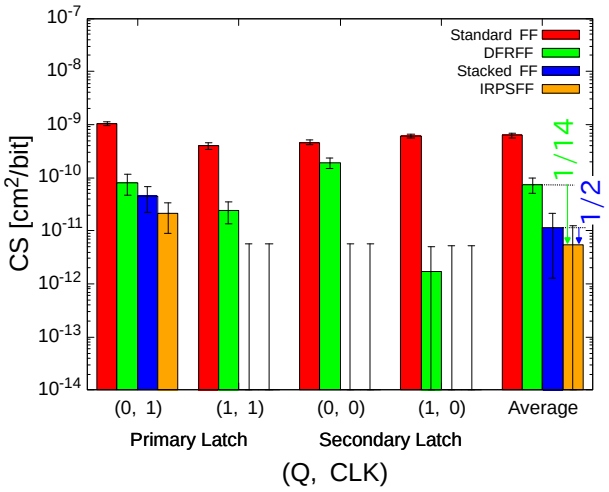



(b) Tilted incidence (45°).

Fig. 11. Measurement setups at RIBF. Degrader was used to control LET and shut off the beam. The irradiation was performed for all four conditions: (Q, CLK) = (0, 0), (0, 1), (1, 0), (1, 1).




(a) Normal incidence.




(b) Tilted incidence (45°).

Fig. 12. Results of the CS by Xe-ion irradiation test. Error bars are within 95% confidence. The results show that the IRPSFF achieved the smallest average CS.

at (1, 0), indicating that the C-element is not the dominant source of the errors. Fig. 13 shows the CSs of the stacked FF and IRPSFF at 0° and 45°. The CS increased by 2.77x for the Stacked FF and 4.17x for the IRPSFF. Although the CS of the IRPSFF increased more, CS value remained almost the same as that of the Stacked FF, indicating high robustness under the 45° angled irradiation. The IRPSFF achieved soft-error tolerance comparable to the Stacked FF while suppressing performance overhead through minimal modifications to the DFRFF structure.

## V. CONCLUSION

In this paper, we proposed a radiation hardened FF, named the IRPSFF, and evaluated its soft-error tolerance by Xe-ion irradiation. The IRPSFF combines an RSR-based secondary latch and pass-transistors to improve soft-error tolerance with minimal design changes. To ensure effectiveness against long SET pulses, the target delay for the guard-gate was set to 165 ps based on a sigmoid approximation of prior experimental data, which is consistent with the 162 ps implementation in our design.

Post-layout simulations and heavy-ion irradiation results demonstrated that the IRPSFF achieved comparable radiation hardness to the Stacked FF while maintaining the low power and delay overheads of the DFRFF. At normal incidence, the IRPSFF achieved a 56x lower average CS than the DFRFF

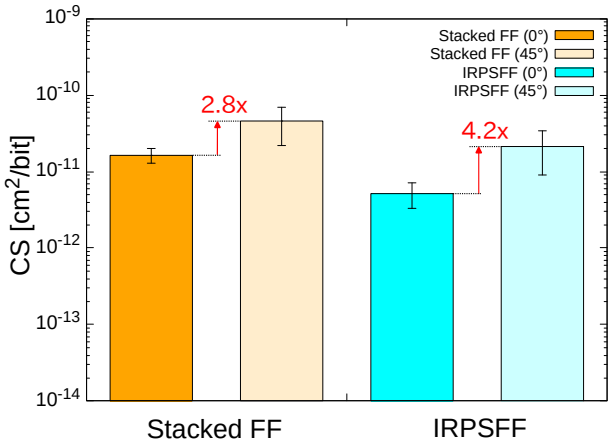



Fig. 13. Comparison of CSs of the Stacked FF and the IRPSFF between irradiation angle of 0° and 45° under the condition of (Q, CLK) = (0, 1). Error bars are within 95% confidence.

and a 3x lower cross-section than the Stacked FF. These results were obtained while reducing CLK-Q and D-Q delays by 35% and 31%, respectively, compared to the Stacked FF.

As a future work, we will evaluate the proposed IRPSFF in advanced FD-SOI nodes such as 22 nm FD-SOI process. In advanced FD-SOI technologies, circuit performance can be tuned by well architecture and substrate potential control [21]. Such tuning may change the SET pulse width and the GG delay. In particular, the pass-transistors forming the GG delay in the IRPSFF are sensitive to substrate potential. Their threshold voltage variations modify the attenuation of SET pulse amplitude. Future work will clarify the substrate potential range where the IRPSFF maintains high soft-error tolerance.

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