Impact of Locations of Circuit Components on Multiple Cell Upset Mitigation in a 22 nm Bulk Process

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***Abstract*—Single-event upsets (SEUs) in redundant storage elements are caused by multiple-cell upsets (MCUs) primarily driven by charge sharing and the parasitic bipolar effect. A precise evaluation of these phenomena is crucial for effective radiation-hardened design. To investigate their relative dominance, we evaluated three types of Triple Modular Redundancy Flip-Flops (TMR-FFs) with different layout structures, fabricated in a 22 nm bulk process. In alpha-particle irradiation tests, the parasitic bipolar effect had no observable impact. Furthermore, the effectiveness of additional interleaving was limited, suggesting that the baseline spacing in the non-hardened design was already sufficient to suppress most charge-sharing-induced MCUs. In contrast, heavy-ion irradiation tests revealed that charge sharing is the predominant cause of MCUs. However, the proportion of MCUs attributed to the parasitic bipolar effect increases with the linear energy transfer (LET). These findings underscore the necessity of combining interleaving with adjacent tap-cell placement to effectively mitigate MCUs in high-LET environments.**

***Index Terms*—soft-error, multiple cell upset, flip-flop, alpha particle, heavy ion**

I. Introduction

Redundancy is an effective countermeasure against soft-errors. However, redundant circuits still fail due to multiple-cell upsets (MCUs) caused by charge sharing and the parasitic bipolar effect [1]. The probability of MCUs increases in advanced technology nodes. This increase is caused by reduced critical charge (Q_{crit}) resulting from lower voltage levels and decreased node capacitance, as well as reduced spacing between cells [2] [3].

Two layout-level countermeasures are commonly used to mitigate MCUs. One is interleaving, which increases the physical distance between vulnerable nodes and reduces MCUs [4]. The other increases the density of well-taps. Well-taps stabilize the well and substrate potentials and reduce MCUs from the parasitic bipolar effect [5]. However, tap-less standard cells require additional tap-cells [6], and a higher tap-cell density for MCU mitigation increases the layout area. The effectiveness of these methods depends on the strength of charge sharing and the parasitic bipolar effect. In low-LET (linear energy transfer) environments, the charge generation region is localized. Therefore, the benefit of interleaving may be limited. In high-LET environments, the charge generation region becomes wider. Thus, charge sharing and the parasitic bipolar effect become significant [7] [8]. This study evaluates how the dominance of charge sharing and the parasitic bipolar effect changes across LET conditions.

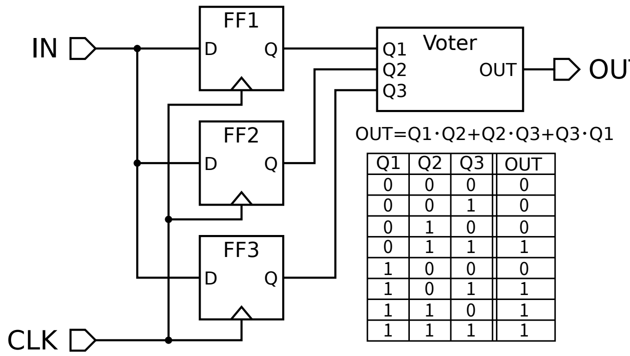
In this paper, three Triple Modular Redundancy Flip-Flops (TMR-FFs) [9] with different interleaving distances and tap-cell placements were designed in a 22 nm bulk process. Charged particle irradiation was used to evaluate the effect of LET on MCU mechanisms. This paper clarifies how the dominant MCU mechanism changes between charge sharing and the parasitic bipolar effect under different LET conditions. This insight helps identify suitable countermeasures for each radiation environment.

II. Target Circuits and MCU Mitigation

Fig. 1 shows the schematic of the TMR-FF. In this paper, the designed TMR-FFs consist of the standard FFs shown in Fig. 2. The description of the designed TMR-FFs is provided below.

t-Non (Fig. 3a)
: No MCU countermeasure is implemented in this layout.

t-Voter (Fig. 3b)
: Interleaving was implemented as a countermeasure against MCUs. The voter was placed in the center to separate the left and right FFs. In FF1, primary



Q1	Q2	Q3	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Fig. 1. TMR-FF.

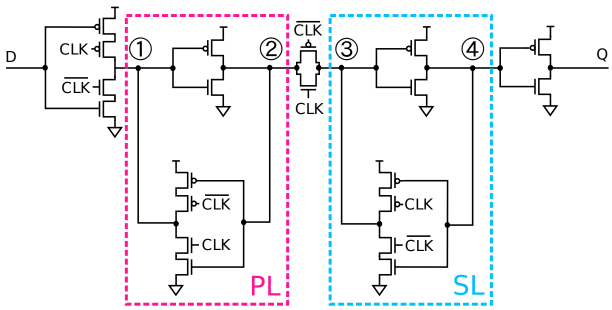
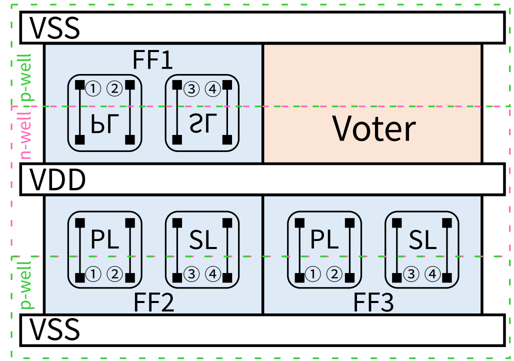
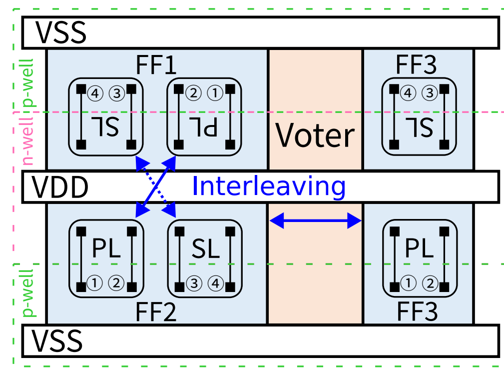


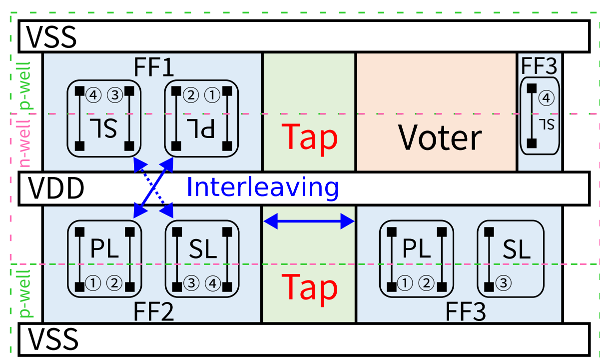
Fig. 2. Standard FF.



(a) t-Non.



(b) t-Voter.



(c) t-Tap.

Fig. 3. Simplified layout diagrams of designed TMR-FFs. Node numbers correspond to those in Fig. 2. PMOS transistors share the same well, whereas NMOS transistors located above and below do not share a common well.

latch (PL) and secondary latch (SL) were swapped to isolate the vulnerable latch nodes in the adjacent FFs. Compared to t-Non, the increased latch spacing is expected to suppress MCUs induced by charge sharing.

t-Tap (Fig. 3c)
: The tap-cells are placed between the left and right FFs to stabilize the well potential. This placement mitigates MCUs induced by both charge sharing and the parasitic bipolar effect.

The MCU countermeasure comparison and inter-node distances of the TMR-FFs are summarized in Tables I and II, respectively. PMOS transistors share the same well, resulting in shorter distances between critical transistors compared to NMOS transistors. By comparing t-Voter with t-Non, the impact of charge sharing can be evaluated based on the difference of interleaving distance. By comparing t-Tap with t-Voter, the impact of parasitic bipolar effect can be evaluated based on the tap-cell density.

TABLE I
Comparison of MCU mitigation between three types of TMR-FFs.

	MCU mitigation	
	charge sharing	parasitic bipolar effect
t-Non	No	No
t-Voter	Yes	No
t-Tap	Yes	Yes

III. Experimental Setups and Results

Neutrons are a major radiation source that causes soft-errors on the ground. However, neutron irradiation generates many secondary particles [10]. Thus, it is difficult to evaluate each particle mechanism separately. This study used charged particles: alpha-particles and heavy-ions. Using both alpha-particles and heavy-ions allows the separation of low-LET and high-LET MCU mechanisms.

A. Setup of irradiation tests

The test chips were fabricated in a 22 nm bulk process. All FFs were implemented as a shift register. For all types

TABLE II
DISTANCES BETWEEN THE VULNERABLE NODE PAIR IN THE TMR-FFS. NODE NUMBERS CORRESPOND TO THOSE IN FIGS. 2 AND 3.

(A) NMOS.

	(Q, CLK), node			
	(0, 1),①	(1, 1),②	(0, 0),④	(1, 0),③
t-Non	1.34 μm	1.34 μm	1.36 μm	1.34 μm
t-Voter	1.92 μm	1.82 μm	1.96 μm	1.94 μm
t-Tap	1.70 μm	1.70 μm	2.80 μm	1.70 μm

(B) PMOS.

	(Q, CLK), node			
	(0, 1),②	(1, 1),①	(0, 0),③	(1, 0),④
t-Non	0.19 μm	0.19 μm	0.19 μm	0.21 μm
t-Voter	0.23 μm	0.87 μm	0.64 μm	1.35 μm
t-Tap	0.27 μm	0.29 μm	0.41 μm	1.23 μm

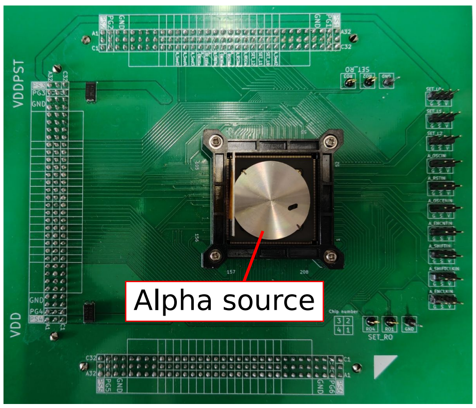


Fig. 4. Measurement setup in the alpha-particle irradiation. An alpha source was placed on the target.

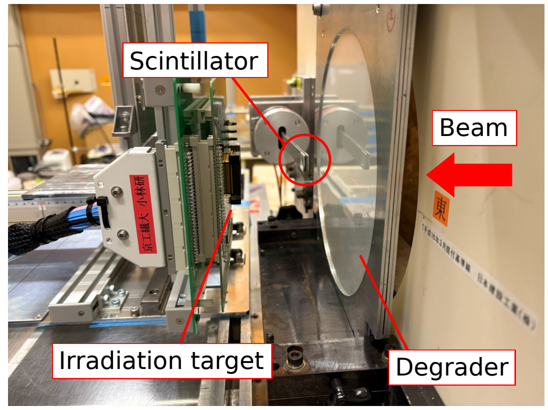


Fig. 5. Measurement setup in the heavy-ion irradiation. Degrader was used for LET adjustment and scintillator was used for beam monitoring.

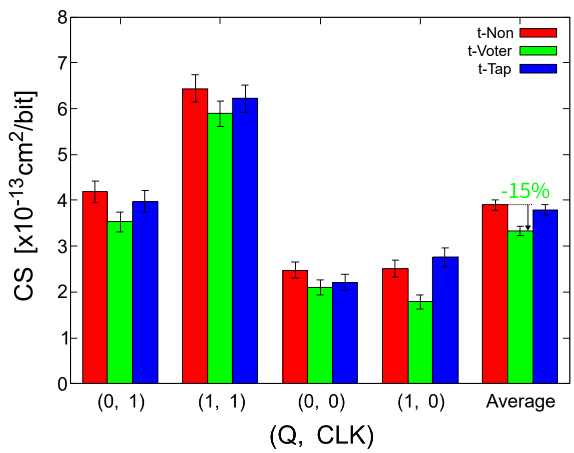


Fig. 6. Experimental results in the alpha-particle irradiation. Error bars are within 95% confidence.

of TMR-FFs, tap-cells are inserted after every four TMR-FFs in the horizontal direction. The irradiation tests were conducted using alpha-particles from a 3 MBq $^{241}\mathrm{Am}$ source. Heavy-ion irradiation using $^{132}\mathrm{Xe}$ was performed at Heavy Ion Medical Accelerator in Chiba (HIMAC) of National Institutes for Quantum Science and Technology (QST) [11]. The LET of the alpha-particle was approximated as 0.645 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$ [12]. In the Xe-ion tests, we evaluated MCU tolerance with two LETs: 33.1 and 42.5 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$. Figs. 4 and 5 show the experimental setups in the alpha-particle and heavy-ion irradiation tests, respectively. The irradiation tests were conducted at the static conditions of (Q, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1). The supply voltage was set to the standard voltage of 0.8 V.

In the irradiation tests, we calculated cross section (CS). CS was calculated by the following equation.

$$\mathrm{CS} = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}} \times N_{\mathrm{ion}} \cos\theta}, \tag{1}$$

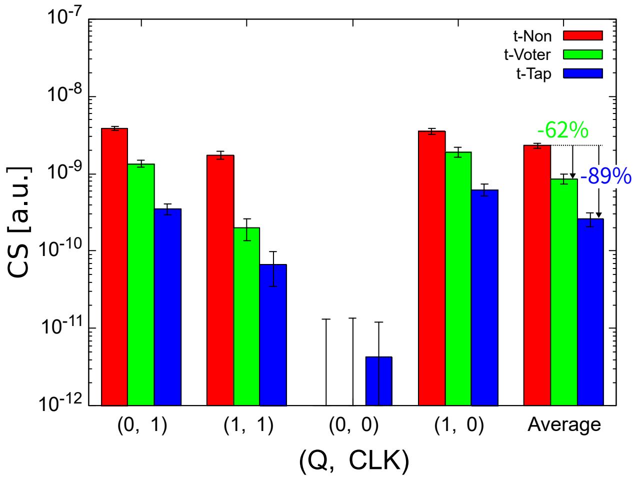
where N_{error} is the number of observed errors, N_{FF} is the number of FFs, N_{ion} is the effective heavy-ion fluence per cm^2, and θ is the irradiation angle [13]. In all the measurements, θ is 0°.

B. Alpha-particle irradiation test

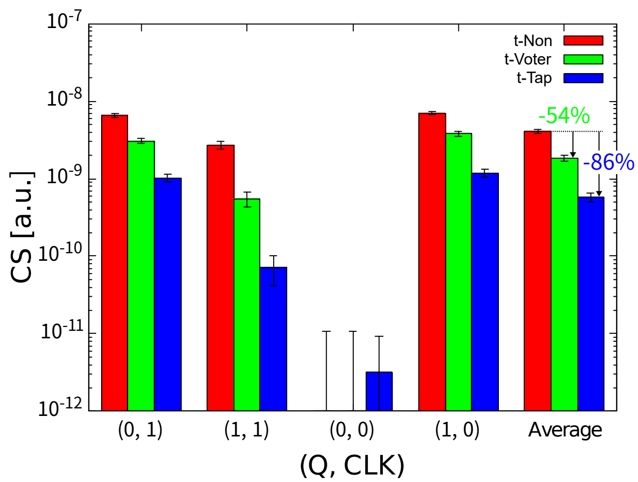
Fig. 6 shows CS in the alpha-particle irradiation. In the alpha-particle test, irradiation was applied from one side of the $^{241}\mathrm{Am}$ source. The active area of the source was 0.95 mm square. The distance between the chips and the source was about 1 mm. Therefore, the attenuation factor was set to 0.68 [14]. The total fluence in the alpha-particle test was approximately 4.5×10^{11} $\mathrm{ions/cm^2}$. t-Voter showed the smallest average CS among the TMR-FFs, and it was 15% lower than that of t-Non.

C. Heavy-ion irradiation tests

Fig. 7 shows the CSs in the heavy-ion irradiation. In the HIMAC measurements, secondary particles generated by the polymethyl-methacrylate (PMMA) degrader affected the fluence measured by the scintillator. Therefore, CS values are compared using an arbitrary constant. These particles are primarily high-energy protons and alpha-particles. Their impact on MCU generation is negligible relative to Xe-ions due to their low LET and low probability of direct ionization. Therefore, a relative comparison of the MCU tolerance remains valid.



(a) LET = 33.1 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$.



(b) LET = 42.5 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$.

Fig. 7. Experimental results in the heavy-ion irradiation. Error bars are within 95% confidence. The CS values for the two different LET levels are on the same scale.

For both LET conditions, the MCU tolerance followed the order: t-Tap $>$ t-Voter $>$ t-Non. As the LET increased from 33.1 to 42.5 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$, the average CS increased by factors of 1.8, 2.2, and 2.2 for t-Non, t-Voter, and t-Tap, respectively.

IV. Discussion

A. Low-LET condition (alpha-particle)

In the alpha-particle test, t-Voter showed the lowest CS among the TMR-FFs. However, the difference was smaller than in the heavy-ion results. The reduction of the cross-section from t-Non to t-Voter was only 15%. This result suggests that the latch spacing of t-Non was enough to suppress charge sharing for alpha-particles. The remaining 85% of MCUs could not be prevented by any TMR-FF types. Oblique particle incidences may expand the effective charge generation region [15]. Thus, charge may be collected beyond the layout spacing. However, the number of MCUs was very small in all circuits as shown in Table III. Thus, the standard spacing already provided sufficient tolerance against charge sharing-induced MCUs.

TABLE III
The Number of Errors per Chip per Test under Alpha-Particle Irradiation. The Results are Averaged over 10,000 Trials of 10-second Tests per (Q, CLK) Condition using Four Chips.

	# of TMR-FFs per chip	# of errors for each (Q, CLK) conditions			
		(0, 1)	(1, 1)	(0, 0)	(1, 0)
t-Non	6272	0.030	0.046	0.018	0.018
t-Voter	6160	0.025	0.041	0.015	0.012
t-Tap	6016	0.027	0.042	0.015	0.019

TABLE IV
Average Q_{crit} [fC] of Corresponding Nodes Across the Three FFs in the TMR-FFs. Node Numbers Correspond to Those in Figs. 2 and 3.

(a) NMOS.

	(Q, CLK), node			
	(0, 1),①	(1, 1),②	(0, 0),④	(1, 0),③
t-Non	1.3	2.5	3.3	1.2
t-Voter	1.4	2.7	3.8	1.3
t-Tap	1.3	2.5	3.7	1.3

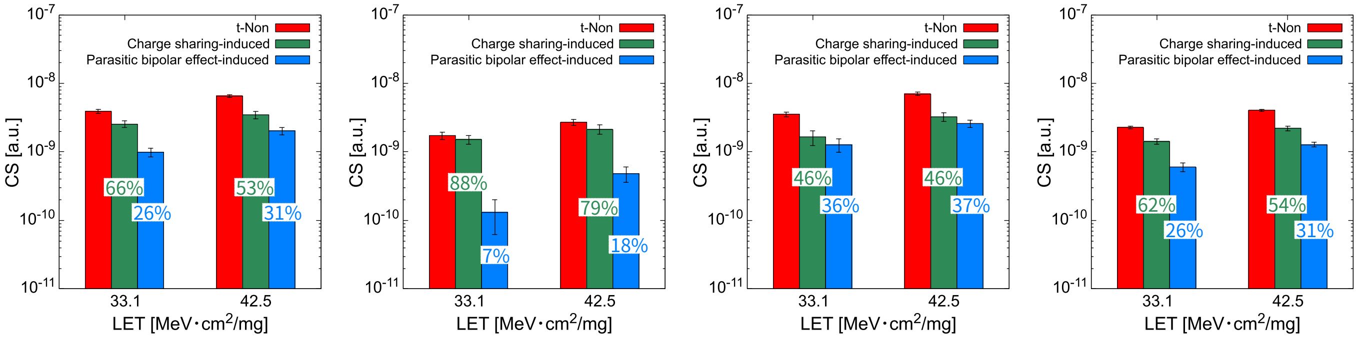
(b) PMOS.

	(Q, CLK), node			
	(0, 1),②	(1, 1),①	(0, 0),③	(1, 0),④
t-Non	2.4	1.3	1.3	2.9
t-Voter	2.6	1.4	1.5	3.3
t-Tap	2.4	1.3	1.4	3.2

In contrast, the CS of t-Tap was slightly higher than that of t-Voter. This result is likely caused by the smaller Q_{crit} of t-Tap and its relatively smaller node-to-node distances compared to t-Voter. While both structures employ interleaving, t-Voter tends to have larger spacing between sensitive nodes than t-Tap, which further mitigates the probability of charge sharing. Table IV shows Q_{crit} of each node in the TMR-FFs. Q_{crit} was calculated by circuit simulations with the single exponential model [16]. The differences in Q_{crit} were mainly caused by parasitic capacitance resulting from variations in layout features such as wiring density. The higher Q_{crit} generally provides higher soft-error tolerance. Alpha-particle error rates strongly depend on Q_{crit}, as reported in [17] [18]. The predicted tolerance trend from Q_{crit} is t-Voter, t-Tap, then t-Non. This trend generally agrees with the measured results. The clear advantage of t-Tap observed in heavy-ion tests did not appear in the alpha-particle tests. Therefore, the parasitic bipolar effect is negligible for alpha-induced MCUs.

B. High-LET conditions (heavy-ion)

Fig. 8 shows contribution of charge sharing and the parasitic bipolar effect to MCUs across two LET conditions. The CS values from charge sharing and the parasitic bipolar effect are



(a) (Q, CLK) = (0, 1). (b) (Q, CLK) = (1, 1). (c) (Q, CLK) = (1, 0). (d) Average.

Fig. 8. Contribution of charge sharing and the parasitic bipolar effect to MCUs across two LET conditions in the heavy-ion tests. Results for the (Q, CLK) = (0, 0) condition were omitted as the low error rate made it difficult to identify meaningful trends.

defined by the following equations.

Charge sharing-induced:

$$\mathrm{CS} = \mathrm{CS(t\text{-}Non)} - \mathrm{CS(t\text{-}Voter)}, \tag{2}$$

Parasitic bipolar effect-induced:

$$\mathrm{CS} = \mathrm{CS(t\text{-}Voter)} - \mathrm{CS(t\text{-}Tap)}. \tag{3}$$

CS(t-Non), CS(t-Voter), and CS(t-Tap) represent the CS values shown in Fig. 7.

In the heavy-ion tests, clear differences appeared among the three TMR-FFs. For both LET conditions, charge sharing-induced CS accounted for more than 45% of the CS(t-Non). On average, charge sharing-induced CS accounted for approximately 60% of CS(t-Non), and parasitic bipolar effect-induced CS represented approximately 30% of CS(t-Non). The remaining portion of the CS(t-Non) (approximately 10%), which corresponds to the CS of t-Tap, represents the residual MCUs that could not be suppressed even with the combination of both interleaving and dense tap-cell placement in the t-Tap structure. Among the four (Q, CLK) conditions, the larger charge sharing contribution appeared at the (1, 1) condition. Charge sharing accounted for approximately 80-90% of the CS in t-Non. In this condition, the PMOS vulnerable node (node 1) had the largest sensitive area. A larger sensitive area increases the probability of charge collection from incident particles. It increases the MCU probability from charge sharing. This induced the larger MCU reduction as shown in Fig. 7. Therefore, interleaving placement provided stronger improvement in this condition. On the other hand, while the proportion of the parasitic bipolar effect-induced CS was smaller than the other (Q, CLK) conditions, a significant difference was observed between t-Voter and t-Tap as shown in Fig. 7. This indicates that the placement of tap-cells also contributed to suppressing the parasitic bipolar effect.

When LET increased from 33.1 to 42.5 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$, the number of MCUs increased in all types of TMR-FFs. However, the contribution of charge sharing decreased from 62% to 54% on average. In contrast, the contribution of parasitic bipolar effect increased from 26% to 31%. These results indicate that the dominant MCU mechanism gradually shifts from charge sharing to the parasitic bipolar effect as LET increases. Therefore, layout techniques that only increase node spacing may become insufficient in high-LET environments.

V. Conclusion

This study evaluated TMR-FF tolerance in a 22 nm bulk process under multiple LET conditions. Experimental results show that the dominance of charge sharing and the parasitic bipolar effect depends on LET. Under low-LET condition (0.645 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$), the minimum spacing of t-Non sufficiently suppressed charge sharing. The parasitic bipolar effect was not observed. Under high-LET conditions (33.1 and 42.5 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$), more than 45% of MCUs are caused by charge sharing. Thus, interleaving becomes essential. Moreover, the parasitic bipolar contribution increases to about 30% as LET rises from 33.1 to 42.5 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$. Thus, interleaving alone cannot provide sufficient tolerance. Therefore, high-LET designs should combine interleaving with dense tap-cell placement.

While this study provides comprehensive insights into MCU mechanisms in a planar bulk process, continuous technology scaling introduces new structural challenges. Current mainstream technology nodes employ FinFETs, whose three-dimensional structures differ significantly from those of conventional bulk planar MOSFETs. These structural differences alter the underlying mechanisms of soft-errors [19] [20]. Therefore, it is essential to investigate the relative contributions of charge sharing and the parasitic bipolar effect in such advanced nodes.

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