Gate-Voltage-Dependent Input Capacitance Partitioning for Accurate Modeling of Trench-Gate SiC MOSFETs

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***Abstract*—This paper presents a dynamic input-capacitance model for trench-gate silicon carbide (SiC) MOSFETs that accounts for voltage-dependent partitioning between gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances. In contrast to conventional planar-based models with static partition boundaries, the proposed model introduces a dynamically varying boundary governed by instantaneous changes of gate-source voltage V_{gs} and gate-drain voltage V_{gd}. The model is developed based on transient electric field behavior extracted from technology computer-aided design (TCAD) simulations, which reveal time-dependent shifts in the internal gate oxide field boundary during switching transitions. Experimental validation is conducted using gate charge measurements obtained from a double-pulse tester (DPT) with model fitting performed across a two-dimensional voltage space. Compared to the conventional static-boundary model, the proposed model improves accuracy, reducing the relative error against the measurements. Furthermore, it successfully captures the voltage dependence of C_{gs}, thereby offering enhanced physical fidelity for circuit simulations and circuit design involving trench-gate SiC MOSFETs.**

***Index Terms*—SiC MOSFET, trench structure, input capacitance, simulation model**

I. Introduction

Wide-bandgap (WBG) semiconductors, particularly silicon carbide (SiC), offer superior material properties over conventional silicon (Si), including high breakdown voltage, excellent thermal conductivity, and fast switching [1], [2]. SiC-based power devices have been widely adopted in various applications, such as electric vehicles, renewable energy systems, and industrial converters [3]–[5].

SiC MOSFETs typically adopt either planar or trench-type gate structures. In recent years, trench structures have gained prominence due to their improved performance in power applications. The trench structure reduces internal resistance by eliminating the junction field-effect transistor (JFET) region inherent in the planar structure and facilitates higher channel density through cell pitch reduction [2]. Deeper trench depths enable longer vertical channels, which effectively increase the channel cross-sectional area. This results in a reduction of channel resistance and thus allows higher current capability with lower conduction losses. Unlike conventional planar MOSFETs, where a longer channel length typically increases resistance due to an extended carrier transport path, the unique vertical channel architecture in trench devices inverts this trend. Previous studies have confirmed that optimizing trench depth is critical for minimizing conduction losses and improving device performance [6], [7].

However, a major drawback of the trench structure is the increased gate-drain capacitance (C_{gd}), arising from the enlarged overlap between gate and drain regions compared to planar devices [8]. As the trench depth increases, this overlap becomes more pronounced, leading to significantly larger C_{gd} values [9]. Consequently, the input capacitance ($C_{\mathrm{iss}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$) is also affected, directly influencing the switching dynamics and gate drive requirements.

As power electronics systems demand higher efficiency, faster switching speed, and more compact design, accurate power MOSFET models have become increasingly crucial for the efficient design of SiC-based power converters. This is because circuit simulators play a central role in the design and optimization of such converters, making the fidelity of device models essential [10]–[13]. Despite the significant structural differences between trench and planar MOSFETs, most of the existing compact models for trench-type SiC MOSFETs still rely on the device models for planar devices. For instance, some models define a fixed partition boundary between C_{gs} and C_{gd} at the channel edge, following the

structural manner used for planar devices [8]. These models typically treat C_{gs} as a constant and dominate the input capacitance prior to the gate voltage plateau, after which C_{gd} is abruptly introduced [9].

In practice, however, the transition between C_{gs} and C_{gd} is continuous and highly dependent on the instantaneous terminal voltages. The planar-based assumption of a static boundary oversimplifies the physical behavior in the trench-type structure, where increased gate–drain overlap and vertical electric field distribution create a voltage-sensitive and dynamically shifting boundary. This effect becomes more pronounced with deeper trench structures, further limiting the accuracy of conventional models in reproducing the transient behavior of input capacitance during switching.

To overcome this limitation, we propose a dynamic gate capacitance model that incorporates both structural and voltage-dependent characteristics of trench-gate SiC MOSFETs. The model is constructed based on the observation from technology computer-aided design (TCAD) simulations and introduces a dynamically varying boundary between C_{gs} and C_{gd}, determined by the oxide geometry and instantaneous bias conditions. Specifically, the partitioning is governed by the ratio of V_{gs} to V_{gd}, which serves as a simplified indicator of the electric field orientation.

This paper is organized as follows: Section II describes the TCAD simulation setup and presents key observations of the dynamic electric field behavior during switching events. Based on the TCAD simulation results, Section III introduces the proposed voltage-dependent capacitance partitioning model, highlighting its physical basis and formulation. Section IV describes the model validation using a commercial trench-gate SiC MOSFET. This section also discusses the parameter fitting process for our model using double-pulse test (DPT) measurements, a commonly used method for evaluating the switching performance of power devices. The accuracy of the proposed model is then compared with that of conventional models, through both parameter fitting results and time-domain waveform analysis to further assess its performance. Section V concludes this paper.

II. TCAD Simulation

To observe the switching behavior of C_{iss} in the trench-type SiC MOSFET, we analyzed the electrical properties using a commercial TCAD simulator [14].

A. Device Modeling and Setup

Figure 1 illustrates the cross-sectional structure of the simulated trench-gate 4H-SiC MOSFET used in the TCAD simulation. The key device parameters are summarized in TABLE I, based on typical commercial design values and relevant literature [3]. We performed TCAD simulations of the trench-gate SiC MOSFET to quantify the transient evolution of the gate-oxide capacitance during switching.

The turn-on switching behavior was simulated while ramping V_{gs} from 0 V to 20 V and holding V_{ds} down from 30 V to 0 V. Although the drain voltage used here is lower than the typical rating for high-power applications, it is sufficient to trigger a shift in the internal electric field boundary. This enables the evaluation of the voltage-dependent partitioning of the input capacitance C_{iss}, with particular focus on C_{gd} under switching transient conditions.

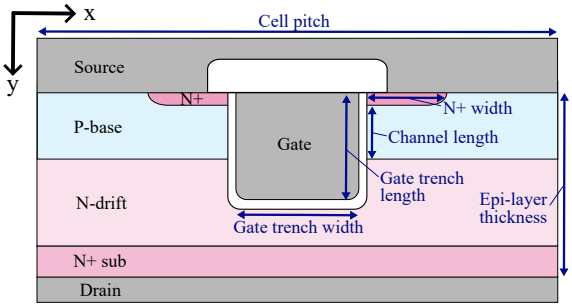


Fig. 1. Cross-sectional structure of the simulated trench-gate SiC MOSFET structure used in the TCAD simulation.

TABLE I
Device Parameters for TCAD Simulations

Parameter (unit)	Values
Cell pitch (μm)	12.0
Gate trench width (μm)	2.0
Gate trench depth (μm)	2.2
Gate oxide thickness - Side (μm)	0.050
Gate oxide thickness - Bottom (μm)	0.10
N+ width (μm)	3.0
N+ thickness (μm)	0.30
P-base width (μm)	5.0
P-base thickness (μm)	1.5
Epi-layer thickness (μm)	12.0
N+ sub thickness (μm)	3.0
N-drift doping concentration (cm^{-3})	2.0×10^{15}
N+ sub doping concentration (cm^{-3})	1.0×10^{19}
P-base doping concentration (cm^{-3})	9.0×10^{16}
N+ doping concentration (cm^{-3})	2.0×10^{19}

1) Electric Field Behavior: To investigate the dynamic capacitance behavior of trench-gate SiC MOSFETs, transient TCAD simulations were performed using the structure shown in Fig. 1.

Figure 2 illustrates the simulated turn-on switching waveforms of V_{gs} and V_{ds} in the TCAD simulation.

The six representative time points, denoted as t_0 through t_5, were selected for detailed analysis. Specifically, t_0 corresponds to the initial off-state, while t_1 marks the moment when the gate voltage reaches the threshold voltage V_{th}. The time points t_2 to t_4 span the Miller plateau region, during which the conductive channel develops and the internal electric field distribution shifts, altering the effective partition between C_{gs} and C_{gd}. The point t_5 represents the post-plateau steady state. To further resolve the dynamic behavior within the plateau, the intermediate points t_{3a} and t_{3b} were additionally extracted. These points elucidate the gradual migration of the electric field within the gate oxide.

Figure 3 displays the TCAD cross-sectional views of the space charge distribution at the time points t_0 through t_5. The brown contours indicate the boundaries of the depletion regions. At t_0 and t_1, the trench sidewalls remain fully depleted, inhibiting current conduction. Between t_1 and t_2, the depletion region near the trench collapses,

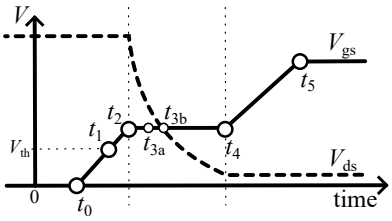


Fig. 2. TCAD-simulated switching waveform with labeled time points t_0 to t_5, corresponding to key stages in the turn-on transition of the trench-gate SiC MOSFET.

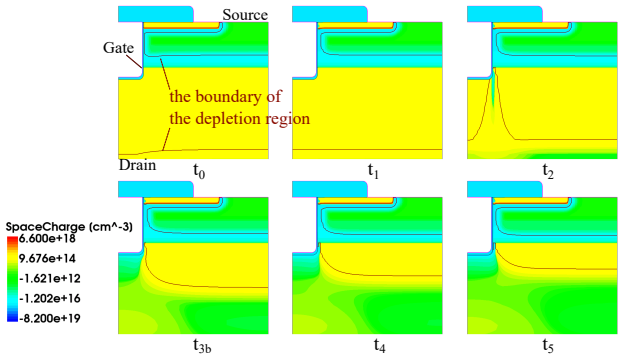


Fig. 3. TCAD cross-sectional views of space charge distribution at time points t_0 to t_5. The brown lines represent the boundary of the depletion regions. Note that this figure depicts only half of the cross-sectional structure shown in Fig. 1. This is because the TCAD simulation was performed on a symmetrical half-structure to reduce computational cost, taking advantage of the device's geometric symmetry.

initiating channel formation. During the interval from t_2 to t_4, the depletion regions beneath the gate and across the PN junction gradually contract, corresponding to the Miller plateau in the switching waveform. After t_4, minimal changes are observed, indicating that the switching event is essentially complete and the device has reached a quasi-static state. Notably, the most significant variations in the depletion region occur beneath the gate during t_2 to t_4, which strongly affects the input capacitance C_{iss}. To elucidate this effect, the next subsection presents electric field vector plots corresponding to the key transitions observed in this interval.

2) Electric Field Vector: To further elucidate the behavior of the internal electric field during switching, electric field vector diagrams were extracted from the TCAD simulations at selected time points: t_0, t_2, t_{3a}, t_{3b}, and t_4, as shown in Fig. 4. Each subfigure depicts the direction of the electric field at the corresponding time point, overlaid on a color map of electron density. The arrows of uniform length indicate direction only; field magnitude is not represented.

The red line labeled "Boundary" denotes the transition between E_{gs} (the electric field from gate to source) and E_{gd} (the electric field from gate to drain). This boundary is determined by the direction of the electric field within the gate oxide. When the absolute values of V_{gs} and V_{gd} induce opposing orientations, as observed from t_0 through t_{3a}, the field vectors cancel out at a distinct point where the net electric field becomes negligible, making the boundary easily identifiable. Beyond t_{3b}, although the field magnitudes differ, the boundary can still be estimated from the overall vector distribution and is indicated by a red line in each subfigure.

The boundary location shifts dynamically with variations in V_{gs} and V_{ds}, reflecting the evolving internal field profile. Notably, the portion of the gate oxide influenced by E_{gs} expands progressively from t_0 to t_{3b}, reaching its maximum extent as $|V_{\text{gs}}|$ becomes dominant. After t_{3a}, the polarity of V_{gs} and V_{gd} aligns, and the boundary gradually shifts back toward the source side by t_4, thereby reducing the effective contribution to C_{gs}.

This dynamic boundary behavior provides the physical foundation for the voltage-dependent partitioning of C_{gs} and C_{gd} introduced in the next section.

III. Dynamic C_{iss} Model

A. C_{iss} Distribution

Figure 5(a) shows a standard equivalent circuit of parasitic capacitances, and Fig. 5(b) depicts the corresponding cross-sectional structure of a trench-gate SiC MOSFET. The input capacitance, C_{iss}, comprises C_{gs} and C_{gd}, each influenced by V_{gs} and V_{gd}, respectively. As illustrated in Fig. 5(b), these capacitances originate from the gate oxide and depletion regions. C_{gs} is primarily determined by the oxide capacitance beneath the gate, and can be composed into three components: C_{OV}, $C_{\text{N+}}$, and C_{P}. These are combined into an effective oxide capacitance $C_{\text{ox,gs}}$ as follows:

$$C_{\text{gs}} = C_{\text{ox,gs}} (= C_{\text{OV}} + C_{\text{N+}} + C_{\text{P}}). \tag{1}$$

In contrast, C_{gd} consists of a series combination of the gate-to-drain oxide capacitance $C_{\text{ox,gd}}$ and the depletion layer capacitance C_{Dep} as shown in (2) [2]. Note that model parameters are hereafter denoted in bold.

$$C_{\text{gd}} = C_{\text{ox,gd}} \parallel C_{\text{Dep}} = C_{\text{ox,gd}} \left(1 - \frac{C_{\text{ox,gd}}^2}{\mathbf{ZETA}} \cdot V_{\text{d}}\right)^{-\frac{1}{2}}, \tag{2}$$

where $V_{\text{d}} = \max(V_{\text{gd}}(t) - \mathbf{VJ}, 0)$, and $\mathbf{ZETA}$ characterizes the voltage response of the depletion region and depends on the doping concentration in the N-drift region. $\mathbf{VJ}$ is an effective built-in voltage associated with the drain–drift junction and determines the endpoint of the Miller plateau during switching.

In conventional models, the oxide capacitances $C_{\text{ox,gs}}$ and $C_{\text{ox,gd}}$ have served as fundamental parameters that define the behavior of C_{gs} and C_{gd}. These oxide components form the physical basis of the input capacitance model, and their treatment significantly influences the model's accuracy.

However, conventional models assume both $C_{\text{ox,gs}}$ and $C_{\text{ox,gd}}$ to be constant values, independent of the applied voltages [8], [9]. This simplification implies that the internal electric field distribution in the gate oxide remains fixed throughout switching. As demonstrated in the previous section, the boundary between C_{gs} and C_{gd} shifts dynamically in response to variations in V_{gs} and V_{gd}, making such assumptions inadequate for trench-type structures.

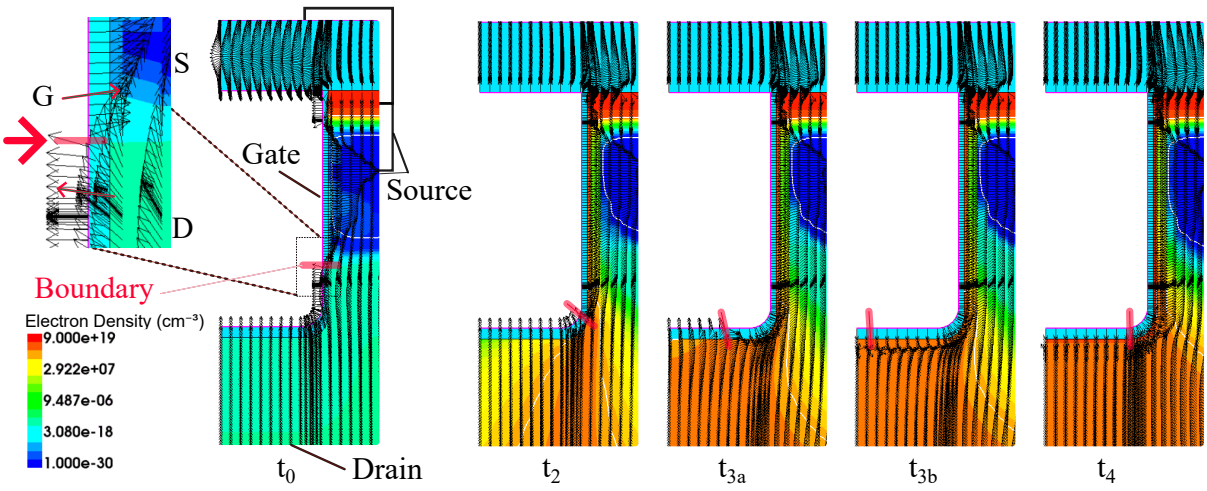


Fig. 4. Electric field vector diagrams and electron density maps at key time points (t_0, t_2, t_{3a}, t_{3b}, and t_4). The black arrows indicate the direction and relative strength of the electric field. The red lines indicate the estimated boundary between gate-to-source and gate-to-drain field regions, based on the direction of the local electric field.

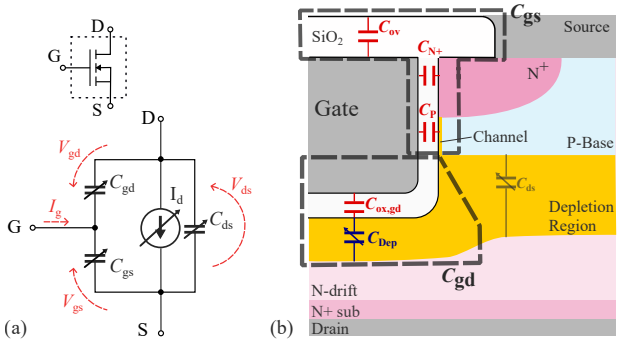


Fig. 5. (a) Equivalent circuit including parasitic capacitances; (b) Cross-sectional view of a trench-gate SiC MOSFET structure showing the physical locations of C_{gs}, C_{gd}, and depletion regions.

To more accurately reflect this behavior, we propose a capacitance model derived from the TCAD simulations, wherein a voltage-dependent partitioning boundary determines the oxide capacitances.

B. Dynamic Gate-oxide Partitioning

In conventional models, the boundary between $C_{\mathrm{ox,gs}}$ and $C_{\mathrm{ox,gd}}$ is statically located at the channel end, assuming a fixed field distribution. However, the TCAD simulations reveal that this boundary shifts over time as the terminal voltage changes. As shown in Fig. 4, the internal electric field within the oxide dynamically changes as $V_{\mathrm{gs}}(t)$ and $V_{\mathrm{gd}}(t)$ evolve, altering the effective contribution areas to $C_{\mathrm{ox,gs}}$ and $C_{\mathrm{ox,gd}}$.

To capture this behavior, we define $C_{\mathrm{ox,gs}}$ and $C_{\mathrm{ox,gd}}$ as time-varying functions of the instantaneous terminal voltages. In what follows, the bold symbols denote fitting parameters. The proposed formulation is as follows:

$$C_{\mathrm{ox,gs}}(t) = (\mathbf{CG} - \mathbf{CC} - \mathbf{CD})\frac{|V_{\mathrm{gs}}|}{|V_{\mathrm{gs}}| + |V_{\mathrm{gd}} - \mathbf{VJ}|} + \mathbf{CC}, \tag{3}$$

$$C_{\mathrm{ox,gd}}(t) = \mathbf{CG} - C_{\mathrm{ox,gs}}(t), \tag{4}$$

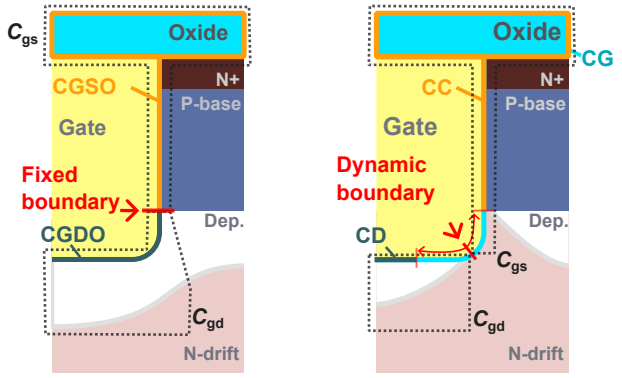
where **CG** denotes the total gate oxide capacitance distributed along the trench; **CC** is the minimum gate-to-source oxide capacitance (i.e., C_{gs} in the off-state at the channel end); and **CD** is the minimum contribution of oxide to C_{gd} near the drain-side depletion region. Note that these oxide capacitances, $C_{\mathrm{ox,gs}}$ and $C_{\mathrm{ox,gd}}$, always sum up to **CG** by definition.

This empirical formulation uses a simple voltage ratio to approximate the voltage-dependent partitioning of the gate oxide field, reflecting the directionality of the electric field observed in the TCAD simulations. Figure 6 illustrates the conceptual difference between the conventional and proposed models. In the conventional model, the C_{gs}–C_{gd} boundary is fixed, giving constant **CGSO** and **CGDO**. In contrast, the proposed model uses a voltage-dependent boundary that better captures the transient response, consistent with the TCAD results in Fig. 4. While the conventional model employs four fitting parameters: **CGSO**, **CGDO**, **ZETA**, and **VJ**, our model introduces five parameters: **CG**, **CC**, **CD**, **ZETA**, and **VJ**. The inclusion of an additional parameter allows the model to more faithfully reproduce the time- and voltage-dependent shift in the internal capacitance boundary, as observed in the TCAD simulations.

IV. Model Validation

A. Gate Input Charge Measurement

To validate the proposed capacitance model, we employed a measurement methodology based on switching trajectories obtained from DPT [13], which enables accurate extraction of the total gate charge Q_{g}. The DPT setup used in this work is illustrated in Fig. 7. The device under test (DUT) was a commercial trench-gate SiC MOSFET (SCT3080AL, ROHM Co., Ltd. [15]). The circuit parameters of the DPT are listed in TABLE II. Note that, to slow down the switching trajectories and clearly observe the capacitive behavior of the device, a relatively large gate resistance ($R_{\mathrm{g}} = 511\,\Omega$) was intentionally chosen.



(a) Conventional Model (b) Proposed Model

Fig. 6. Comparison between (a) the conventional model with a fixed boundary and (b) the proposed model with a dynamically varying boundary between C_{gs} and C_{gd}.

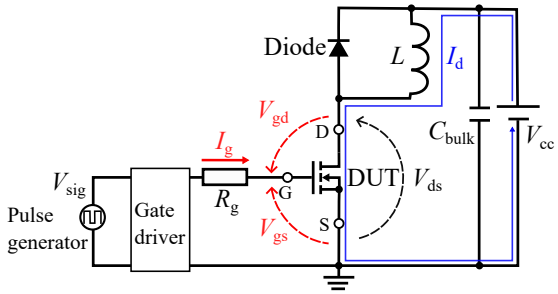


Fig. 7. DPT circuit diagram used for the charge measurement. Each value of the circuit parameters is listed in TABLE II.

The model parameters were optimized by fitting the simulated Q_g to the measured one over a two-dimensional voltage space defined by V_{gs} and V_{gd}. In this method, the gate current $I_g(t)$ is measured during switching transients and numerically integrated to compute the total gate charge:

$$Q_g(t) = \int_0^t I_g(\tau)\,d\tau. \tag{5}$$

Q_g consists of two charge components, Q_{gs} and Q_{gd}, associated with C_{gs} and C_{gd}, respectively: $Q_g = Q_{gs}+Q_{gd}$. This decomposition links the physically stored charge in the gate oxide regions to measurable gate charge waveform and serves as the basis for the parameter extraction. Each component can be expressed as:

$$Q_{gs} = \int C_{gs}(V_{gs}, V_{gd})\,dV_{gs}, \tag{6}$$

$$Q_{gd} = \int C_{gd}(V_{gs}, V_{gd})\,dV_{gd}. \tag{7}$$

Because C_{gs} and C_{gd} are functions of both V_{gs} and V_{gd}, closed-form integration is generally not feasible. Therefore, during the model fitting, the predicted capacitance values of C_{gs} and C_{gd} are numerically integrated using the measured voltage waveform, and the resulting Q_g is compared with experimental data. The model parameters are then optimized by minimizing the discrepancy between the simulated and measured Q_g across the V_{gs}–V_{gd} space.

TABLE II
CIRCUIT PARAMETERS OF THE DPT CIRCUIT

Parameter	Value
Gate signal amplitude	$V_{sig} = 0$–$18\,V$
Gate resistance	$R_g = 511\,\Omega$
Load inductance	$L = 220\,\mu H$
Drain voltage	$V_{cc} = 44\,V$
Bulk capacitor	$C_{bulk} = 200\,\mu F$

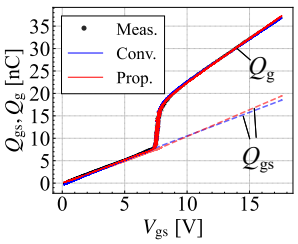


Fig. 8. Measured and modeled Q_g as a function of V_{gs}. (Q_{gs} is obtained from the model.)

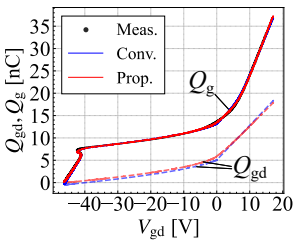


Fig. 9. Measured and modeled Q_g as a function of V_{gd}. (Q_{gd} is obtained from the model.)

B. Results

Figures 8 and 9 present the fitting results of both the proposed and conventional models in comparison with the measured gate charge characteristics. Both the models successfully capture the overall trend of Q_g over the relevant voltage range. The conventional model assumes a constant value for C_{gs}, whereas the proposed model introduces a dynamic C_{gs} that depends on V_{gs} and V_{gd}. Despite the increased complexity, the proposed model achieves comparable or even superior accuracy. This indicates that incorporating the dynamic behavior of the gate-to-source capacitance does not compromise the model's ability to fit measured data and, in fact, better reflects the actual device physics. As observed in both the figures, the proposed model closely matches the measured Q_g values across the entire voltage range, particularly in the Miller plateau region. In this region, the dynamic shift of the internal boundary between the gate-to-source and gate-to-drain regions significantly affects charge distribution, a phenomenon more accurately captured by the proposed formulation.

Quantitatively, the proposed model yields a lower root-mean-square error (RMSE) of 1.62 nC, compared to 2.01 nC for the conventional model under identical conditions. This improvement highlights the enhanced accuracy in reproducing the gate charge characteristics. Furthermore, as shown in Figure 10, significant differences can be observed in the overall shape of the extracted capacitance characteristics. The conventional model maintains a constant C_{gs} throughout the switching event, whereas the proposed model reflects its variation during transient operation. This dynamic behavior more accurately represents the redistribution of the gate charge resulting from a time-evolving field boundary within the gate oxide region.

The fitting process involves numerical integration and multivariate optimization, which may affect computation time; however, the simulation speed when using the final-

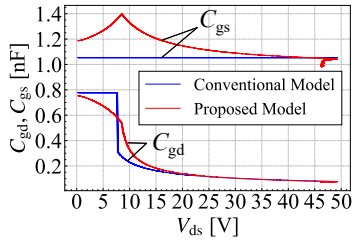


Fig. 10. Modeled C_{gs} and C_{gd} characteristics as a function of V_{ds} for both proposed and conventional models.

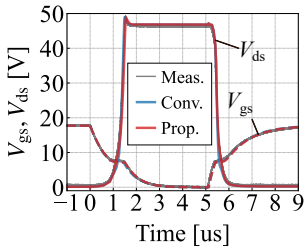


Fig. 11. Measured and simulated waveforms of V_{gs} and V_{ds} using conventional and proposed models.

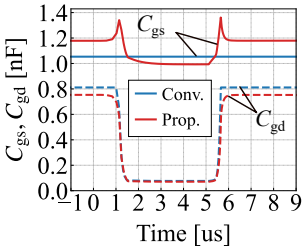


Fig. 12. Simulated dynamic variation of C_{gs} and C_{gd} during the switching transition.

ized model in circuit-level simulations is not significantly affected.

To further validate the proposed model in the time domain, transient simulations were performed using a commercial SPICE simulator [16] under the same DPT measurement conditions shown in Fig. 7. A baseline compact model for the DUT is developed according to a method utilized in [13]. Then, we replaced its C_{iss} characteristics with the proposed model. Figure 11 compares the measured and simulated V_{gs} and V_{ds} waveforms for the conventional and proposed models. With the proposed model, the transient RMSE decreases from 0.439 V to 0.433 V for V_{gs} and from 1.34 V to 0.941 V for V_{ds}, reflecting the impact of the improved C_{gd} modeling and yielding a clear enhancement in transient accuracy. Figure 12 shows the corresponding time variations of C_{gs} and C_{gd}, consistent with the static characteristics in Fig. 10. In particular, the proposed model transitions dynamically between distinct on- and off-state values of C_{gs}, capturing the time-varying capacitance behavior during switching.

V. Conclusion

This paper proposed a dynamic input capacitance model for trench-gate SiC MOSFETs, grounded in transient charge distribution behavior observed in TCAD simulations. In contrast to conventional models that assume a fixed C_{gs}, the proposed model incorporates a dynamically evolving boundary between the gate-to-source and gate-to-drain regions of the gate oxide, governed by the instantaneous terminal voltages V_{gs} and V_{gd}. The model was applied to a commercial trench-gate SiC MOSFET and validated using gate charge measurements obtained from DPT. Compared to the conventional fixed-capacitance model, the proposed formulation achieved improved fitting accuracy while successfully capturing the transient variation in C_{gs}, particularly in the Miller plateau region, where the location of the internal boundary strongly influences charge dynamics. Future work will extend this validation through transient circuit simulations and broader experimental studies to evaluate the model's applicability and robustness under various operating conditions.

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