Variation-Aware Circuit Simulation of Parallel-Connected SiC MOSFETs Based on Individual Device Modeling

Kazuki Matsumoto
Graduate School of Science and Technology, Kyoto Institute of Technology
Kyoto, Japan
kmatsumoto@vlsi.es.kit.ac.jp

Taiki Nishioka
Graduate School of Science and Technology, Kyoto Institute of Technology
Kyoto, Japan
tnishioka@vlsi.es.kit.ac.jp

Hajime Takayama
Graduate School of Science and Technology, Kyoto Institute of Technology
Kyoto, Japan
hajime-takayama@kit.ac.jp

Jun Furuta
Graduate School of Comp. Sci. and Syst. Eng., Okayama Prefectural University
Okayama, Japan
furuta@c.oka-pu.ac.jp

Kazutoshi Kobayashi
Graduate School of Science and Technology, Kyoto Institute of Technology
Kyoto, Japan
kazutoshi.kobayashi@kit.ac.jp

Michihiro Shintani
Graduate School of Science and Technology, Kyoto Institute of Technology
Kyoto, Japan
shintani@kit.ac.jp

***Abstract*—Silicon carbide (SiC) MOSFETs exhibit significant device-to-device variation, which cannot be accurately simulated using the SPICE models provided by manufacturers. This paper presents a variation-aware circuit simulation framework based on individual device modeling. The proposed method is applied to two commercial SiC MOSFETs with parametric variations, whose device parameters are extracted from measured switching waveforms and implemented into a SPICE simulation of the parallel connection of the two devices. Transient analyses under double-pulse test conditions successfully reproduce the current imbalance in experiments, with rise time and fall time showing good agreement between simulation and measurement (errors within 0.9–5.2%). Furthermore, the simulation environment enables the evaluation of countermeasures using an active gate driver with individually tuned waveforms. The agreement between simulation and measurement validates the effectiveness of the proposed method. This variation-aware simulation methodology facilitates early-stage evaluation of imbalance mitigation techniques. It contributes to design quality of high-power SiC-based converter circuits.**

***Index Terms*—SiC MOSFET, device modeling, characteristic variation, SPICE simulation, parallel connection, active gate drive**

I. Introduction

The research and development of power conversion circuits using silicon carbide (SiC) MOSFETs have been rapidly accelerated in recent years. Their installation into various industrial applications, including electric vehicles and railway traction, is steadily expanding [1], [2]. SiC-based power converters are increasingly operated at higher voltages and switching frequencies to achieve higher power density, making circuit simulation a crucial step in reducing development time and cost in the design process.

However, the simulation models of SiC MOSFETs provided by manufacturers often fail to reproduce the actual characteristics of the devices at hand. This is partially due to the limited fidelity of the internal model equations and the potential inaccuracies in the measurement data itself [3]. More importantly, the manufacturer's models cannot reproduce the device-to-device variation of SiC MOSFETs, which results from their still-immature fabrication processes compared to Si-based power devices [4], [5]. Such variation becomes a critical concern when multiple SiC MOSFETs are connected in parallel to achieve higher current capacity [6], [7]. Differences in device characteristics lead to a current imbalance among the devices, which causes localized power losses and thermal stress, eventually degrading the reliability and lifetime of the system [8].

Circuit-level approaches, including active gate drivers (AGDs), have been found promising for mitigating current imbalance in parallel-connected SiC MOSFETs [9], [10]. However, there is currently no simulation environment that enables circuit designers to evaluate such countermeasures in advance. As a result, mitigation strategies are often developed through trial and error after deploying actual hardware, making it challenging to implement effective solutions during the design phase [8]. Consequently, there is a growing demand for circuit simulation methods that can explicitly account for individual device variation.

This study develops a SPICE simulation environment that can reproduce the non-ideal behavior arising from the parametric variation of parallel-connected SiC MOSFETs. A modeling methodology proposed in [11] is utilized to construct individual device models to account for the device-to-device variation, enabling the analysis of current imbalance that manufacturer models cannot capture. The simulation results are compared with experiments under several gate-driving conditions to validate the accuracy and applicability

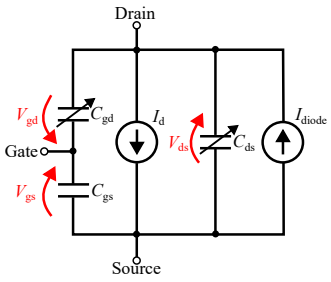


Fig. 1. Equivalent circuit model of the SiC MOSFET, including current and capacitance components.

of the proposed variation-aware modeling approach.

The remainder of this paper is organized as follows. Section II reviews the device modeling methodology presented in [11], which is deployed to construct the proposed simulation environment. Section III presents the modeling results for two selected SiC MOSFETs and discusses their characteristic differences. Section IV describes the parallel operation of the two devices in a double-pulse test setup under different gate driving conditions. The SPICE simulation results are compared with measurements to validate the accuracy of the models. Finally, Section V concludes this paper.

II. Modeling Method for SiC MOSFETs

To construct a simulation environment for SiC MOSFETs with parametric variation, each MOSFET needs to be measured and implemented with different model parameters. For this purpose, we employ the device modeling methodology proposed in [11]. In this method, the current characteristics are measured using short pulses to eliminate the influence of self-heating. The capacitance characteristics are dynamically measured using switching waveforms, which enables accurate characterization of device behavior under varying operating points. Several measurements of switching waveforms are performed for each device using ordinary laboratory equipment, and a model fitting is performed individually.

The equivalent circuit of the SiC MOSFET model is illustrated in Fig. 1. The model is composed of three parts: a drain current model (I_d), a body diode current model (I_diode), and capacitance models for the inter-terminal pairs of gate-source (C_gs), gate-drain (C_gd), and drain-source (C_ds). Each component is described by a set of equations in which the characteristics are expressed as functions of the terminal voltages: gate-source voltage (V_gs), gate-drain voltage (V_gd), and drain-source voltage (V_ds). The model parameters, indicated in bold throughout the following discussion, are determined via curve fitting to ensure agreement between the model output and measured switching characteristics.

A. Current model

The drain current I_d is modeled using the α-power law model, which accounts for various non-ideal physical effects in MOSFET operation [12]. The saturation current $I_\mathrm{d,sat}$ and saturation voltage $V_\mathrm{ds,sat}$ are expressed as functions of the gate-source voltage V_gs, as shown in (1) and (2). The parameters **J** and **M** characterize the device behavior in the linear region, while **K** and **N** govern the saturation region.

$$I_\mathrm{d,sat} = \mathbf{K}(V_\mathrm{gs} - \mathbf{VTH})^{\mathbf{N}} \tag{1}$$

$$V_\mathrm{ds,sat} = \mathbf{J}(V_\mathrm{gs} - \mathbf{VTH})^{\mathbf{M}} \tag{2}$$

To capture the effect of the parasitic resistance in the drift region, the internal drain-source voltage $V_\mathrm{ds,int}$ is introduced, as given in (3). It is calculated from V_ds, the drain current I_d, and the parasitic resistance **RD**. A modified voltage $V_\mathrm{ds,mod}$ is then computed to provide a smooth transition between the linear and saturation regions as shown in (4). The parameter **DELTA** controls the smoothness of this transition [12].

$$V_\mathrm{ds,int} = V_\mathrm{ds} - \mathbf{RD} \cdot I_\mathrm{d} \tag{3}$$

$$V_\mathrm{ds,mod} = \frac{V_\mathrm{ds,int}}{\left(1 + \left(\frac{V_\mathrm{ds,int}}{V_\mathrm{ds,sat}}\right)^{\mathbf{DELTA}}\right)^{\frac{1}{\mathbf{DELTA}}}} \tag{4}$$

Using $V_\mathrm{ds,mod}$, the drain current I'_d can be written as shown in (5) [12]. In (6), the hyperbolic tangent (tanh) function is used to express the variation of the drain current I_d in response to changes in gate-source voltage V_gs. Since the drain current exhibits non-ideal behavior, an empirical model using the tanh function and mobility degradation terms is employed to fit the measured characteristics. Furthermore, the expression is extended in (7) by incorporating the channel length modulation parameter **CLM**, and the mobility degradation parameters **MD** and **MOVTH**, resulting in the current equation used in this model [11].

$$I'_\mathrm{d} = I_\mathrm{d,sat} \cdot \left(2 - \frac{V_\mathrm{ds,mod}}{V_\mathrm{ds,sat}}\right) \cdot \frac{V_\mathrm{ds,mod}}{V_\mathrm{ds,sat}} \tag{5}$$

$$I''_\mathrm{d} = I'_\mathrm{d} \cdot 0.5 \cdot \left(1 + \tanh\left(\frac{V_\mathrm{gs} - \mathbf{VTH}}{\mathbf{SMLV}}\right)\right) \tag{6}$$

$$I_\mathrm{d} = \frac{I''_\mathrm{d} \cdot (1 + \mathbf{CLM} \cdot V_\mathrm{ds})}{1 + \mathbf{MD} \cdot (V_\mathrm{gs} - \mathbf{MOVTH})} \tag{7}$$

The body diode current I_diode is modeled using a conventional p-n junction expression with series resistance **RS** on the diode current path and thermal voltage scaling parameter **KB** as shown in (8).

$$I_\mathrm{diode} = \mathbf{IS} \cdot \left(\exp\left(\frac{V_\mathrm{ds} - \mathbf{RS} \cdot I_\mathrm{diode}}{\mathbf{KB}}\right) - 1\right) \tag{8}$$

B. Capacitance model

C_gs exhibits relatively weak voltage dependence compared to C_gd and C_ds, and is therefore modeled as a constant value [13]. C_gd is modeled using a piecewise approach that switches between a variable MOS capacitance and a fixed gate oxide capacitance **COXD**, depending on the bias condition. Under reverse bias, C_gd follows a square-root dependence on the gate-drain voltage V_gd, based on the ideal depletion region expansion. Under strong forward bias, the capacitance saturates to the gate-drain oxide capacitance [14]. Both C_gd and C_ds decrease with increasing forward bias due to the widening of the depletion layer, and

TABLE I
EXTRACTED MODEL PARAMETERS FOR DEVICE A AND DEVICE B

Parameter	Dev. A	Dev. B	Model
J	0.1307	0.2085	$I_{\rm d}$–$V_{\rm ds}$
K	0.01692	0.02344	$I_{\rm d}$–$V_{\rm ds}$
M	1.658	1.401	$I_{\rm d}$–$V_{\rm ds}$
N	3.021	2.932	$I_{\rm d}$–$V_{\rm ds}$
RD	0.03748	0.05067	$I_{\rm d}$–$V_{\rm ds}$
VTH	2.792	2.697	$I_{\rm d}$–$V_{\rm ds}$
DELTA	1.130	1.100	$I_{\rm d}$–$V_{\rm ds}$
SMLV	10.11	10.29	$I_{\rm d}$–$V_{\rm ds}$
CLM	0.001208	0.001339	$I_{\rm d}$–$V_{\rm ds}$
MD	0.05080	0.04228	$I_{\rm d}$–$V_{\rm ds}$
MOVTH	13.21	13.05	$I_{\rm d}$–$V_{\rm ds}$
IS	0.001604	0.002553	$I_{\rm diode}$–$V_{\rm ds}$
RS	0.4092	0.4240	$I_{\rm diode}$–$V_{\rm ds}$
KB	0.3008	0.3066	$I_{\rm diode}$–$V_{\rm ds}$
CGSO	1.436×10^{-9}	1.504×10^{-9}	$Q_{\rm gs}$–$V_{\rm gs}$
COXD	1.501×10^{-9}	1.443×10^{-9}	$Q_{\rm gd}$–$V_{\rm gd}$
CDGO	3.483×10^{-10}	3.614×10^{-10}	$Q_{\rm gd}$–$V_{\rm gd}$
VJ	17.80	17.21	$Q_{\rm gd}$–$V_{\rm gd}$
CDSO	2.201×10^{-9}	2.148×10^{-9}	$Q_{\rm ds}$–$V_{\rm ds}$
CDSV	0.09576	0.1038	$Q_{\rm ds}$–$V_{\rm ds}$

their voltage dependence is modeled using inverse-square-root expressions. The complete set of capacitance models is given as shown in (9) to (11).

$$C_{\rm gs} = \mathbf{CGSO} \tag{9}$$

$$C_{\rm gd} = \begin{cases} \dfrac{\mathbf{CDGO}}{\sqrt{V_{\rm gd}+0.5\cdot\mathbf{VJ}}} & (V_{\rm gd} < -0.5\cdot\mathbf{VJ}) \\ \mathbf{COXD} & (V_{\rm gd} \geq -0.5\cdot\mathbf{VJ}) \end{cases} \tag{10}$$

$$C_{\rm ds} = \frac{\mathbf{CDSO}}{\sqrt{1+\frac{V_{\rm ds}}{\mathbf{CDSV}}}} \tag{11}$$

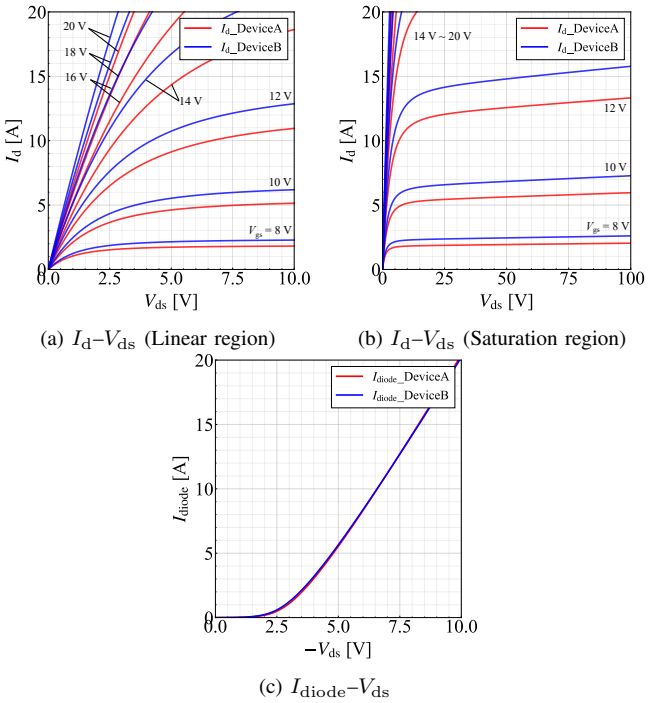
III. MODEL FITTING OF TWO SiC MOSFETS WITH VARIATION

The model equations described in Section II are applied to commercial SiC MOSFETs to extract individual model parameters. This process is partially automated to reduce the required workload. The devices under test (DUTs) are SCT2160KE from ROHM Co., Ltd., rated at 1200 V and 22 A. Two devices are selected from two different manufacturing lots and are hereafter referred to as Device A and Device B, respectively.

The measurements of current and capacitance characteristics are performed for each device, following the procedure presented in [11]. Nonlinear least squares fitting was then employed to optimize the parameters of the model equations described in Section II, and the extracted model parameter values are listed in TABLE I. The model fitting results are presented in this section.

A. Current characteristics

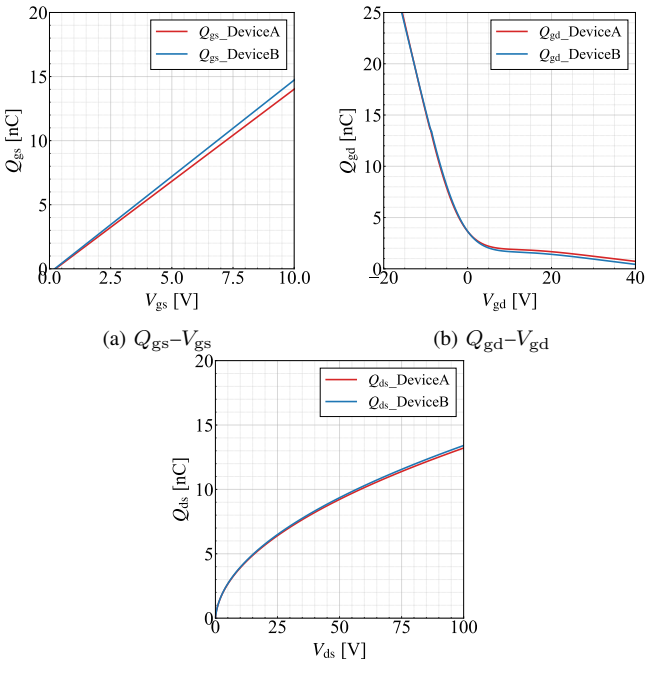
The fitted current characteristics of the two devices are shown in Fig. 2. For the $I_{\rm d}$–$V_{\rm ds}$ characteristics, notable variations are observed in both the linear and saturation regions, with Device B exhibiting higher drain current than Device A under the same gate bias conditions. These differences are attributed to process-induced variations, such as threshold voltage shifts and differences in channel conductance. Such variations affect the transient and steady-state behavior during the switching operation and can result in current



(a) $I_{\rm d}$–$V_{\rm ds}$ (Linear region) (b) $I_{\rm d}$–$V_{\rm ds}$ (Saturation region)

(c) $I_{\rm diode}$–$V_{\rm ds}$

Fig. 2. Model fitting results of current characteristics for Device A and Device B.



(a) $Q_{\rm gs}$–$V_{\rm gs}$ (b) $Q_{\rm gd}$–$V_{\rm gd}$

(c) $Q_{\rm ds}$–$V_{\rm ds}$

Fig. 3. Model fitting results of capacitance characteristics for Device A and Device B.

imbalance when the devices are connected in parallel. In contrast, the variation in the body diode characteristics ($I_{\rm diode}$–$V_{\rm ds}$) is negligible as confirmed in Fig. 2(c).

B. Capacitance characteristics

The fitting results for the three inter-terminal capacitance characteristics are shown in Fig. 3. Note that each capaci-

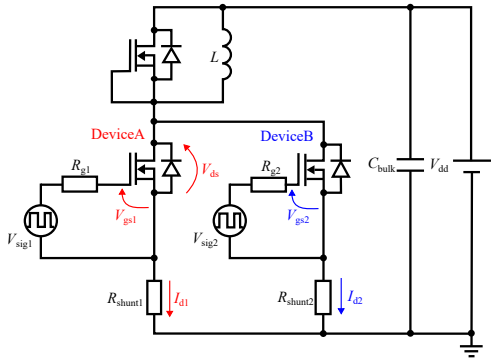


Fig. 4. Schematic diagram of the double-pulse test circuit with two parallel-connected SiC MOSFETs.

tance is fitted based on the charge profile. No significant variation is observed in the gate-to-source charge Q_{gs} between the two devices. In contrast, variations in the gate-to-drain charge Q_{gd} are observed in the negative V_{gd} region, and variations in the drain-to-source charge Q_{ds} increase at higher V_{ds}. However, these differences are relatively minor, and the overall impact of capacitance variation on the circuit behavior is considered negligible compared to that of current characteristics variation.

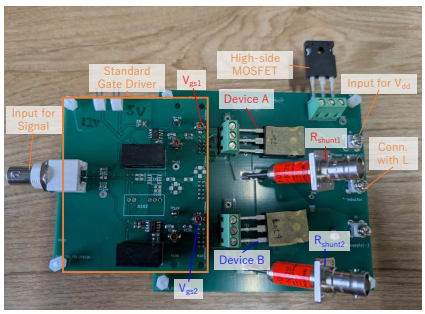
IV. Comparison between Simulation of Parallel-Connected Circuit and Actual Circuit Operation

The individual device models developed in Section II are implemented using an analog hardware description language Verilog-A [15]. Transient simulations were performed using a commercial SPICE simulator (Synopsys HSPICE [16]) to evaluate turn-on and turn-off behaviors of parallel-connected SiC MOSFETs in a double-pulse testing circuit. The simulation results are compared with experimental data to verify their accuracy.

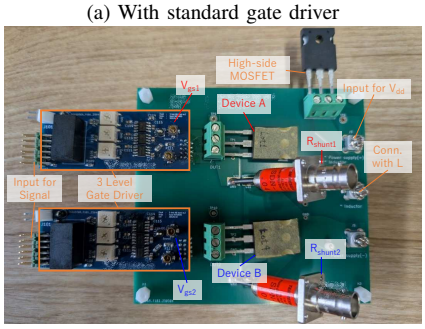
A. Experimental setup

The schematic diagram of the switching test circuit is shown in Fig. 4. Each of the two parallel-connected SiC MOSFETs was driven by an individual gate driver. The fabricated circuit board is presented in Fig. 5. Coaxial shunt resistors (SDN-414-05, T&M Research Product, Inc.) are placed adjacent to the source terminals of each device to enable an independent, high-bandwidth measurement of the drain current. The gate drivers are connected via pin header connectors for testing under different gate-driving conditions.

Two types of gate driving conditions are employed: a standard gate driving and an active gate driving. The corresponding gate drive waveforms are shown in Fig. 6. Figure 5(a) shows the setup with a standard gate driver. A commercial gate driver generates the rectangular-wave gate voltage profile as shown in Fig. 6(a). The gate supply voltage V_{gg} is set at 18 V and a gate resistor of 11 Ω is used for both devices. Figure 5(b) shows the setup with an active gate driver. The gate driver is constructed by a series connection of three gate-driver modules, which generates

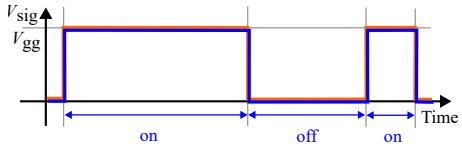


(a) With standard gate driver

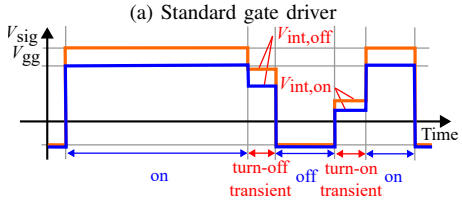


(b) With 3-level gate driver

Fig. 5. Photographs of two parallel double-pulse test circuit boards.



(a) Standard gate driver



(b) 3-level gate driver

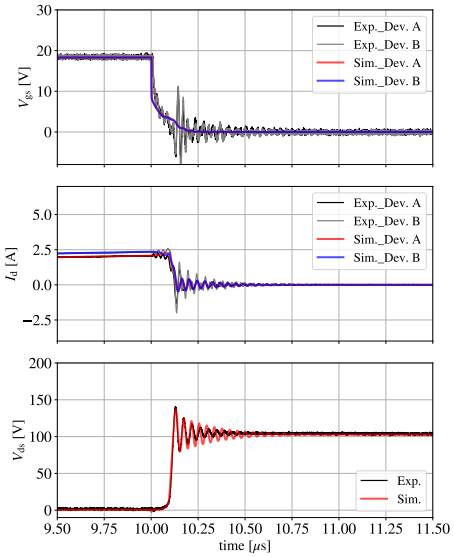
Fig. 6. Gate drive waveforms applied to the devices.

a 3-level gate voltage profile as shown in Fig. 6(b) [17]. Intermediate voltage levels, $V_{\mathrm{int,on}}$ and $V_{\mathrm{int,off}}$ are applied during the turn-on and turn-off transients, enabling gradual on/off switching of switching devices. The intermediate voltage levels can be individually tuned for each device, enabling precise control of switching behavior considering the variation of the device characteristics.

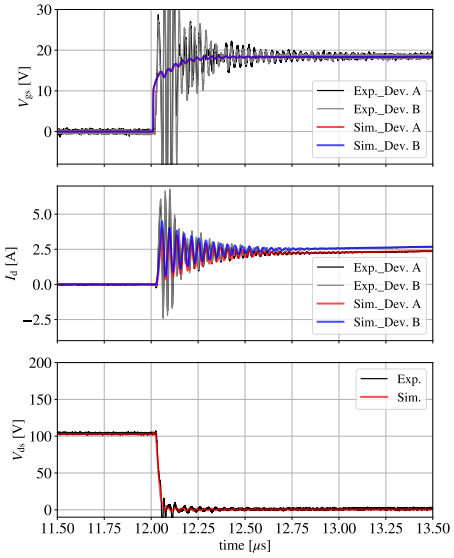
The experimental conditions are as follows: the primary power supply voltage V_{dd} is set to 100 V; the inductor L is 220 μH; and the load current is set to 2 A. Under these conditions, the waveforms of V_{gs}, V_{ds}, and I_{d} were compared between the simulation and the experiment.

B. Operation with standard gate drive

Fig. 7 compares the simulated and measured waveforms when a gate voltage of $V_{\mathrm{gg}} = 18$ V is applied to Tboth devices. During the on-state period, where the influence of noise is small, the root-mean-squared error (RMSE) values are 8.95 mA for Device A and 14.5 mA for Device B.

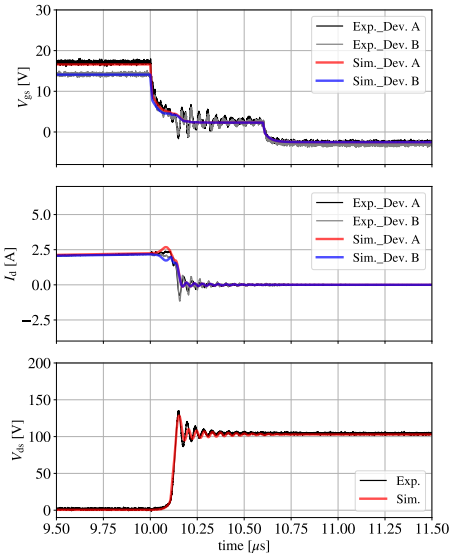


(a) Turn-off

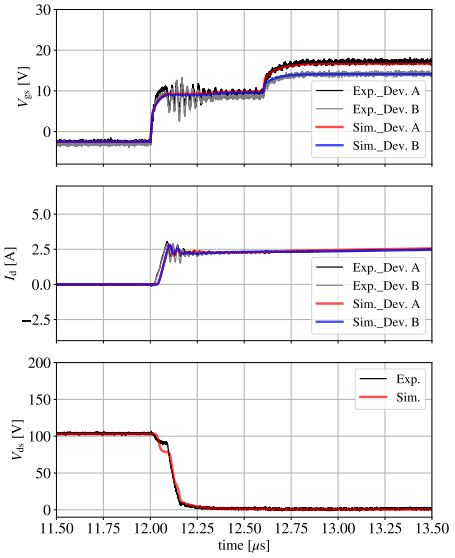


(b) Turn-on

Fig. 7. Transient analysis of two parallel double-pulse tests with standard gate driver.



(a) Turn-off



(b) Turn-on

Fig. 8. Transient analysis of two parallel double-pulse tests with separate gate drive for each device.

Considering that the steady-state load current is 2 A, these deviations correspond to 0.448% and 0.725%, respectively. Therefore, the simulation results accurately reproduce the waveform shape observed in the experiment. In particular, the drain current I_{d} waveforms clearly reflect the current imbalance between the two devices during the on-state, with I_{d2} being about 13.9 % larger than I_{d1}, where I_{d1} and I_{d2} are the currents flowing through Device A and Device B, respectively. This current imbalance leads to unequal power dissipation, resulting in thermal stress concentrated on a single device, which may ultimately degrade the reliability of the module. The proposed variation-aware simulation method can predict such an imbalance during the design stage, allowing for the consideration of appropriate countermeasures in advance.

C. Operation with tuned active gate drive

To mitigate the current imbalance observed in Section IV-B, the gate signals applied to each device were independently adjusted. The gate drive consists of two levels, a reference level and a drive level, and includes a three-level signal configuration that enables intermediate voltage control during the turn-on and turn-off transitions. Fig. 8 compares the simulated and measured waveforms when these gate signals are tuned to balance the drain current through each device. Due to the use of independent gate signals, the gate-source voltages V_{gs} differ between the devices; however, the simulation continues to reproduce the measured waveforms closely. During the on-state period, where the influence of noise is small, the RMSE values are 47.7 mA for Device A and 11.0 mA for Device B. Considering that the steady-state load current is 2 A, these correspond

TABLE II
COMPARISON OF TRANSIENT CHARACTERISTICS (STANDARD GATE DRIVE)

	Parameter [Unit]	SIM.	EXP.	Error [%]
Turn-off	Rise time [μs]	0.114	0.115	0.9
	Settling time [μs]	0.702	0.600	17.0
Turn-on	Fall time [μs]	0.0297	0.0311	4.5
	Settling time [μs]	0.538	0.516	4.3

TABLE III
COMPARISON OF TRANSIENT CHARACTERISTICS (ACTIVE GATE DRIVE)

	Parameter [Unit]	SIM.	EXP.	Error [%]
Turn-off	Rise time [μs]	0.139	0.136	2.2
	Settling time [μs]	0.633	0.550	15.1
Turn-on	Fall time [μs]	0.161	0.153	5.2
	Settling time [μs]	0.483	0.395	22.3

to deviations of 2.385% and 0.550%, respectively, indicating that the simulation reproduces the actual circuit behavior with high accuracy. In particular, the drain current I_{d} shows a marked improvement in current balance, which is accurately captured by the simulation. These results confirm that the proposed variation-aware simulation method can be effectively used to evaluate and optimize countermeasures against the current imbalance in parallel-connected SiC MOSFETs.

Table II and III compare the simulated and measured transient characteristics obtained from the results in Sections IV-B and IV-C. In both the standard gate drive and the active gate drive conditions, the simulation and measurement show comparable results. The rise time, fall time, and settling time show good agreement between simulation and measurement, indicating that the transient behavior is accurately reproduced by the simulation. As a future task, since the present evaluation includes the effect of noise, it will be necessary to perform noise-suppressed measurements and revalidate the results using those data.

V. CONCLUSION

This paper presented a SPICE simulation environment that accounts for the device-to-device parametric variations of SiC MOSFETs through the individual device modeling approach. Two devices exhibiting characteristic differences were modeled and implemented in SPICE simulations to evaluate the current imbalance in the parallel connected configuration. The simulation results successfully reproduced the imbalance observed in the measurements, confirming the validity of the proposed approach. The accuracy was also verified under active gate drive operations, indicating that the design of such countermeasure circuits can be performed with the developed simulation environment. These findings demonstrate that variation-aware modeling and simulation provide an effective means to predict and mitigate current imbalance, thereby contributing to the design of more reliable high-power converter systems. As future work, it will be necessary to extend the method to account for self-heating during continuous operation and to construct a corresponding simulation environment.

ACKNOWLEDGMENT

This work was partially supported by JSPS KAKENHI Grant Numbers 24K22954 and 23K26094. This work was also supported through the activities of d-lab VDEC, the University of Tokyo, in collaboration with NIHON SYNOPSYS G.K.

REFERENCES

[1] X. She, A. Q. Huang, Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8193–8205, 2017.

[2] M. Östling *et al.*, "SiC power devices — present status, applications and future perspective," in *Proceedings of International Symposium on Power Semiconductor Devices and ICs*, 2011, pp. 10–15.

[3] M. Shintani *et al.*, "Comprehensive MOSFET capacitance characterization based on charge trajectories," *IEEE Transactions on Electron Devices*, vol. 72, no. 7, pp. 3758–3766, 2025.

[4] D. Maksimovic *et al.*, "Modeling and simulation of power electronic converters," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 898–912, 2001.

[5] K. Shimozato *et al.*, "Adaptive outlier detection for power MOSFETs based on Gaussian process regression," in *Proceedings of IEEE Applied Power Electronics Conference and Exposition*, 2022, pp. 1709–1714.

[6] H. Li *et al.*, "Influence of paralleling dies and paralleling half-bridges on transient current distribution in multichip power modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6483–6487, 2018.

[7] A. Borghese *et al.*, "Statistical analysis of the electrothermal imbalances of mismatched parallel SiC power MOSFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1527–1538, 2019.

[8] H. Li *et al.*, "Parallel connection of silicon carbide MOSFETs—Challenges, mechanism, and solutions," *IEEE Transactions on Power Electronics*, vol. 38, no. 8, pp. 9731–9749, 2023.

[9] S. Zhao *et al.*, "A review of switching slew rate control for silicon carbide devices using active gate drivers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4096–4114, 2021.

[10] L. Du *et al.*, "Digital active gate driving system for paralleled SiC MOSFETs with closed-loop current balancing control," in *Proceedings of IEEE Energy Conversion Congress and Exposition*, 2022, pp. 1–6.

[11] H. Takayama *et al.*, "Accurate power MOSFET modeling with off-the-shelf instruments," in *Proceedings of International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2025, pp. 2640–2646.

[12] T. Sakurai and A. Newton, "A simple MOSFET model for circuit analysis," *IEEE Transactions on Electron Devices*, vol. 38, no. 4, pp. 887–894, 1991.

[13] M. Shintani *et al.*, "Surface-potential-based silicon carbide power MOSFET model for circuit simulation," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 774–10 783, 2018.

[14] N. Phankong *et al.*, "Evaluation of inherent elements in a SiC power MOSFET by its equivalent circuit," in *Proceedings of European Conference on Power Electronics and Applications*, 2011, pp. 1–8.

[15] C. C. McAndrew *et al.*, "Best practices for compact modeling in Verilog-A," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 5, pp. 383–396, 2015.

[16] Synopsys Inc., "HSPICE User Manual, Version U-2023.03-SP1," Synopsys Inc., 2023.

[17] H. Takayama, S. Fukunaga, and T. Hikihara, "Binary-weighted modular multi-level digital active gate driver," in *Proceedings of European Conference on Power Electronics and Applications*, 2023, pp. 1–8.