A Large-Signal Characterization Method for Dynamic Gate Capacitances of p-GaN HEMTs

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***Abstract*—Small-signal C–V characterization is widely used to extract parameters in simulation models of gallium nitride (GaN) high-electron-mobility transistors (HEMTs). However, it fails to reproduce the gate charge behavior under dynamically varying bias conditions during the switching transient, resulting in significant inaccuracies in circuit simulations. This work presents a large-signal characterization method that captures the dynamic gate-charging behavior of Schottky-gate p-GaN HEMTs. Switching tests are conducted under two distinct bias conditions to extract the gate-source charge profile, which is subsequently subtracted from the total gate charge to obtain the gate-drain charge profile. The extracted C–V characteristics are compared with the industry-standard SPICE model and also with the conventional small-signal measurements, clearly demonstrating the necessity of large-signal characterization for accurate modeling of GaN HEMT gate capacitances.**

***Index Terms*—p-GaN HEMT, gate capacitance, large-signal characterization**

I. Introduction

The enhancement-mode gallium nitride (GaN) high-electron-mobility transistors (HEMTs), such as Schottky-gate p-GaN HEMTs, have been increasingly adopted in various power electronics applications due to their superior performance over silicon counterparts, particularly in high-frequency and high-efficiency power converters such as power supplies for datacenters [1]. Accurate compact models of these devices are essential for predicting their switching behaviors in circuit operation [2], [3]. Among the key device parameters, gate capacitance plays a critical role in determining the gate-charging dynamics and thus the overall switching timing. Conventional small-signal *C–V* measurement, which measures capacitance at fixed bias points, cannot capture the time-varying large-signal behavior that occurs during switching transients [3]. Moreover, the floating node inside the p-GaN/AlGaN gate stack of Schottky-gate p-GaN HEMTs exhibits peculiar dynamic characteristics, such as dynamic threshold voltage [4], which further deviates from the small-signal analysis. These limitations highlight the need for a measurement methodology capable of accurately evaluating the dynamic gate-charge profile under switching conditions.

To address these limitations, this work develops a large-signal characterization method for gate capacitances of Schottky-gate p-GaN HEMTs. The proposed method extracts the dynamic gate-charge profile during the switching transient through switching tests, with particular emphasis on accurately evaluating the gate-drain capacitance characteristics.

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II. Large-Signal Characterization Method

The proposed large-signal characterization aims to extract the gate-source and gate-drain capacitances, $C_{\rm gs}$ and $C_{\rm gd}$, from their respective charge components, $Q_{\rm gs}$ and $Q_{\rm gd}$, calculated from the actual switching waveforms. The primary focus is placed on accurately extracting $C_{\rm gd}$, which undergoes a dynamic transition of the bias voltage during the switching transient, a behavior that is difficult to capture in the conventional small-signal measurement with fixed bias conditions [5]. Considering the total gate charge $Q_{\rm g} = Q_{\rm gs} + Q_{\rm gd}$, $Q_{\rm gd}$ is obtained by a simple subtraction of $Q_{\rm gs}$ from $Q_{\rm g}$ if $C_{\rm gs}$ is accurately modeled as a function of $V_{\rm gs}$. Therefore, we first establish an analytical model of the gate capacitances and then develop an extraction procedure to obtain $C_{\rm gs}$–$V_{\rm gs}$ parameters. Subsequently, $C_{\rm gd}$–$V_{\rm gd}$ characteristics are derived by subtraction.

A. Analytical Gate Capacitance Model

To describe the voltage dependence of each capacitance, a simplified analytical model is employed, as shown in Fig. 1 [4], [6]. Here, $C_{\rm sch}$ represents the metal/p-GaN Schottky junction capacitance, $C_{\rm int,gs}$ and $C_{\rm int,gd}$ denote the sum of AlGaN/GaN hetero junction capacitance and inter-terminal field-plate capacitances at gate-source and gate-drain, and $C_{\rm fri,gs}$ and $C_{\rm fri,gd}$ denote the inter-terminal fringe capacitances, respectively. It is reasonable to assume $C_{\rm fri,gs}$ and $C_{\rm int,gs}$ as constant values [4], while $C_{\rm sch}$ follows the junction capacitance relation: $C_{\rm sch}(V_{\rm sch}) = \sqrt{A/2\,(V_{\rm sch} + B)}$, where A and B are fitting parameters. $C_{\rm fri,gd}$ and $C_{\rm int,gd}$ are voltage-dependent capacitances, as the depletion region is formed at reverse bias conditions.

We define $C_{\rm gs}$ as composed of $C_{\rm fri,gs}$, $C_{\rm int,gs}$, and $C_{\rm sch}$, whereas $C_{\rm gd}$ consists of the remaining two capacitances. The total gate capacitance, $C_{\rm g} = C_{\rm gs} + C_{\rm gd}$, can be expressed according to the formation of the Schottky junction capacitance near the threshold voltage $V_{\rm th}$ as follows [6]:

$$C_{\rm g}(V_{\rm gs}, V_{\rm gd}) = \begin{cases} C_{\rm fri,gs} + C_{\rm fri,gd}(V_{\rm gd}), & V_{\rm gs} < V_{\rm th} \\ C_{\rm fri,gs} + C_{\rm fri,gd}(V_{\rm gd}) + C_{\rm ser}, & V_{\rm gs} \geq V_{\rm th} \end{cases} \tag{1}$$

$$\text{where } \frac{1}{C_{\rm ser}} = \frac{1}{C_{\rm sch}(V_{\rm sch})} + \frac{1}{C_{\rm int,gs} + C_{\rm int,gd}(V_{\rm gd})}. \tag{2}$$

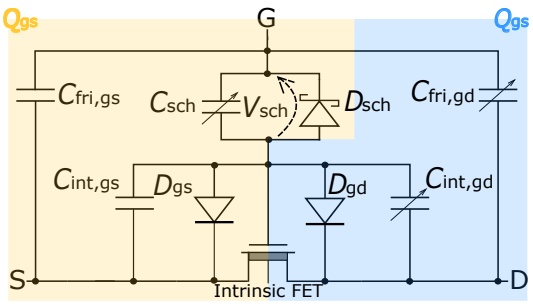


Fig. 1. Gate capacitance model of a Schottky-gate p-GaN HEMT.

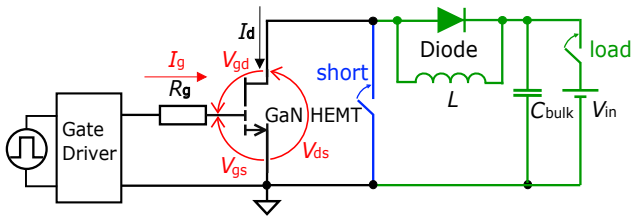


Fig. 2. Schematic diagram of a DPT circuit with load and short conditions.

B. Characterization Procedure

The transient switching waveforms of I_g, V_{gs}, and V_{gd} are measured using a double-pulse test (DPT), from which the total gate charge Q_g is obtained by time integration of the gate current I_g. Subsequently, Q_{gs} is computed from (1) and subtracted from Q_g to yield Q_{gd}. This process requires determining the three capacitances that constitute C_{gs}.

For this purpose, two distinct DPT conditions are employed, that is the *shorted* condition with $V_{ds} = 0\,\mathrm{V}$ and the *load* condition with $V_{ds} \gg 0\,\mathrm{V}$. The corresponding switching test circuits are illustrated in Fig. 2. The details of the procedure are as follows.

1) C_{sch} and $C_{int,gs}$ extraction from shorted condition: Under the *shorted* condition, $C_{int,gd}$ and $C_{fri,gd}$ are assumed constant, as these regions are not depleted. Because $C_{int,gd}$ is negligibly smaller than $C_{int,gs}$ and no Miller effect occurs, the contribution of $C_{int,gd}$ in (2) can be ignored. From the off-state region ($V_{gs} < V_{th}$), the sum of the two fringe capacitances $C_{fri,gs} + C_{fri,gd}$ is extracted as a constant value, as shown in (3). In the on-state region ($V_{gs} \geq V_{th}$), parameter fitting yields a constant value of $C_{int,gs}$ and the two fitting parameters for C_{sch}, as shown in (4):

$$Q_g^{\mathrm{short}}(V_{gs}) = \begin{cases} (C_{fri,gs} + C_{fri,gd})V_{gs}, & V_{gs} < V_{th} \\ (C_{fri,gs} + C_{fri,gd})V_{gs} + C_{ser}^{\mathrm{short}}(V_{gs})V_{gs}, & V_{gs} \geq V_{th} \end{cases} \tag{3}$$

$$\text{where } \frac{1}{C_{ser}^{\mathrm{short}}(V_{gs})} \sim \frac{1}{C_{sch}(V_{sch})} + \frac{1}{C_{int,gs}}. \tag{4}$$

2) $C_{fri,gs}$ extraction from load condition: In the *load* condition, $C_{int,gd}$ and $C_{fri,gd}$ act as Miller capacitances as the switching proceeds. During the off-state ($V_{gs} < V_{th}$), these two capacitances are reverse-biased and hence depleted. Therefore, we can satisfactorily assume that $C_{fri,gs} \gg C_{fri,gd}$ and $C_{int,gs} \gg C_{int,gd}$. From this region, we obtain $C_{fri,gs}$ as a constant parameter as follows:

$$Q_g^{\mathrm{load}}(V_{gs}) \sim C_{fri,gs}V_{gs}, \qquad V_{gs} < V_{th}. \tag{5}$$

3) Modeling of Q_{gs} and separation of Q_{gd}: By combining C_{sch} and $C_{int,gs}$, extracted under the *short* condition with $C_{fri,gs}$, C_{gs} can be modeled as a function of V_{gs}:

$$C_{gs}^{\mathrm{model}}(V_{gs}) = \begin{cases} C_{fri,gs}, & V_{gs} < V_{th} \\ C_{fri,gs} + C_{ser}(V_{gs}), & V_{gs} \geq V_{th} \end{cases} \tag{6}$$

$$\text{where } \frac{1}{C_{ser}(V_{gs})} = \frac{1}{C_{sch}(V_{sch})} + \frac{1}{C_{int,gs}}. \tag{7}$$

The corresponding charge Q_{gs}^{model} is calculated as $Q_{gs}^{\mathrm{model}} = C_{gs}^{\mathrm{model}} \cdot V_{gs}$. By subtracting this modeled charge from the measured total gate charge Q_g, Q_{gd} is consequently obtained.

III. Experimental Validation

A. Devices, Fixtures, and Operating Conditions

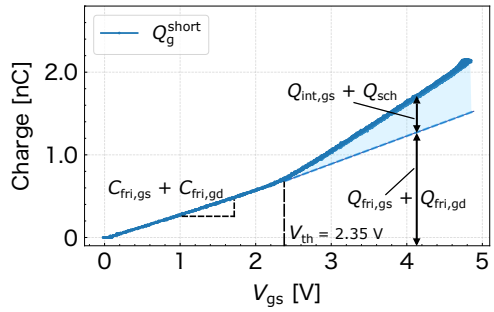
The proposed large-signal characterization was performed on a 100 V-class Schottky-gate GaN-on-SOI HEMT manufactured by imec [7]. A unified experimental setup was configured to perform DPT under the *short* ($V_{ds} = 0\,\mathrm{V}$) and *load* ($V_{ds} = 100\,\mathrm{V}$) conditions. A commercial gate driver IC generated a V_{gs} swing between 0 and 5 V. The gate current I_g was calculated from the measured voltage drop across the resistor R_g, where a relatively large value ($R_g = 1\,\mathrm{k\Omega}$) was selected to suppress oscillations. It should be noted that Schottky-gate p-GaN HEMTs exhibit increased gate leakage current $I_{g,leak}$, which affects the accuracy of the I_g calculation. To eliminate this influence, the $I_{g,leak}$–V_{gs} characteristics were measured in advance, and their contribution was subtracted from the calculated Q_g–V_{gs} data.

B. Large-signal Characterization Results

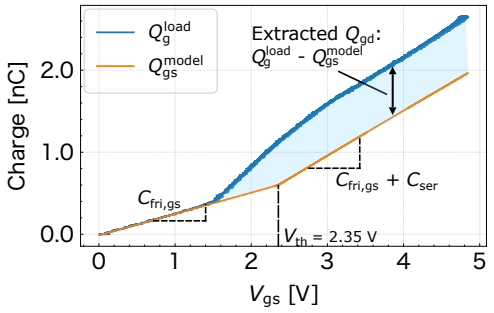
Fig. 3 summarizes the measured gate-charge characteristics obtained at turn-on transient under the two DPT conditions. Fig. 3(a) shows the Q_g^{short}–V_{gs} characteristics. The slope at $V_{gs} < V_{th}$ corresponds to $C_{fri,gs} + C_{fri,gd}$, while the parameters of $C_{int,gs}$ and C_{sch} were determined by fitting (1) and (2) to the data in the region $V_{gs} \geq V_{th}$. Fig. 3(b) shows the Q_g^{load}–V_{gs} characteristics, from which $C_{fri,gs}$ was extracted from its slope at $V_{gs} < V_{th}$. By combining $C_{fri,gs}$, $C_{int,gs}$, and C_{sch} obtained from the above measurements, C_{gs} was modeled as shown in Fig. 3(c), and the corresponding charge profile was calculated as $Q_{gs}^{\mathrm{model}} = C_{gs}^{\mathrm{model}}V_{gs}$. Finally, Q_{gd} was derived by subtracting Q_{gs}^{model} from the measured Q_g^{load}, as also indicated in Fig. 3(b).

C. Comparison with MVSG Model

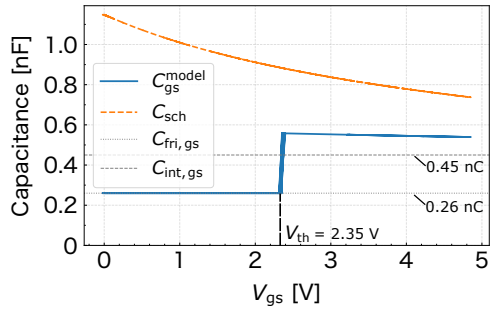
The large-signal characterization results were compared with SPICE simulation using the MIT Virtual Source GaN HEMT (MVSG) model, developed according to the standard parameter extraction procedure described in its user's manual [2]. Fig. 4 presents the Q_g–V_{gs} and Q_{gs}–V_{gs} characteristics. While the Q_{gs}–V_{gs} characteristics show close agreement between measurement and simulation, significant differences appear in the Q_g–V_{gs} plots. Around the Miller plateau, the MVSG model exhibits a sharp increase in Q_g, whereas the measured Q_g shows a gradual rise as the switching proceeds. This difference is attributed to the dynamic charging behavior of C_{gd} captured by the proposed method. Furthermore, the total gate charge Q_g at the completion of the turn-on is larger in the MVSG model, including its tendency to overestimate the charge due to reliance on small-signal characterization. These



(a) Q_g^{short}–V_{gs} plot obtained from *short* condition.



(b) Q_g^{load}–V_{gs} plot obtained from *load* condition.



(c) Extracted $C_{gs}(V_{gs})$ model.

Fig. 3. Large-signal measurement results of Q_g–V_{gs} profiles, obtained C_{gs} parameters, and extracted Q_{gd} profile.

results highlight the limitation of MVSG models extracted from small-signal measurements, which fail to reproduce the dynamic charging behavior of C_{gd} and consequently overestimate Q_g under actual switching operation.

D. Comparison with Small-Signal Measurement

Finally, the proposed large-signal measurement results were compared with the conventional small-signal characterization. The small-signal C_{gd}–V_{ds} characteristics were measured using a semiconductor device analyzer (B1505A, Keysight) and converted to Q_{gd}–V_{gd} plot, where $V_{gd} = -V_{ds}$. Fig. 5 shows the Q_{gd}–V_{gd} curves obtained from the proposed large-signal and conventional small-signal measurements. A notable difference appears as V_{gd} approaches 0 V during the switching. This difference arises from the measurement methodology: in the small-signal C_{gd}–V_{ds} measurement, V_{gs} is fixed at 0 V while V_{ds} is swept, meaning that the metal/p-GaN Schottky junction remains forward-biased and therefore does not contribute to Q_g. In contrast, under the large-signal conditions, V_{gs} and V_{gd} dynamically transition, leading to the formation of the Schottky junction and a corresponding decrease in the equivalent C_g. As a result, less charge is stored in C_{gd}, as clearly indicated in Fig. 5.

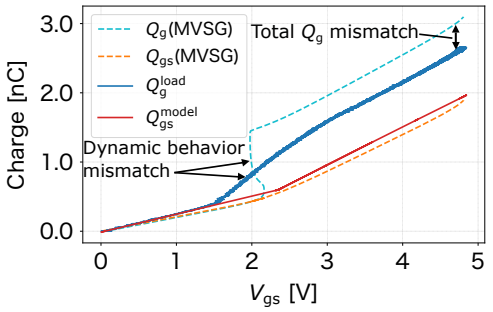


Fig. 4. Comparison of Q_g–V_{gs} characteristics simulated by MVSG model and extracted by large-signal measurements.

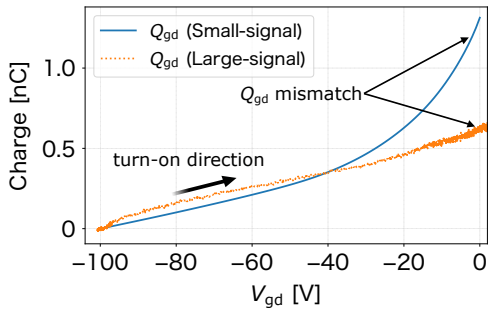


Fig. 5. Comparison of Q_{gd}–V_{gd} characteristics between conventional small-signal and proposed large-signal measurements.

IV. Conclusion

This work presented a large-signal characterization method for evaluating the gate capacitances of Schottky-gate p-GaN HEMTs. The proposed workflow determines Q_g from the measured switching waveforms and separates it into Q_{gs} and Q_{gd} components based on the modeled $C_{gs}(V_{gs})$. The extracted Q_{gd} characteristics revealed distinct dynamic behavior during the switching transients, which is not captured by the MVSG model and can lead to overestimation of gate charge in circuit simulations. A significant deviation in the Q_{gd}–V_{gd} characteristics between large-signal and conventional small-signal measurements further confirms the necessity of large-signal analysis for an accurate device modeling of p-GaN HEMTs.

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