A Multilevel Gate Driver Operating with a Single Voltage Supply and Simple Control Signals for Monolithic Integration of Power GaN HEMT

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***Abstract*—This paper presents a monolithic Gallium Nitride Integrated Circuit (GaN IC) which integrates a multilevel gate driver and a power Gallium Nitride High Electron Mobility Transistor (GaN HEMT). It is effective to prevent false turn-on and reduce reverse conduction loss in the half bridge converter with simple control signals. The multilevel gate driver using a capacitor can apply negative voltage without any additional voltage supply. In order to improve performance of power converters, we monolithically integrated the multilevel gate driver and a power HEMT. To further improve efficiency, we also fabricated another type of a GaN IC which integrates two power HEMTs for half-bridge configuration and the multilevel gate driver with an MIM capacitor. The GaN ICs were fabricated using a GaN-on-SOI process. We evaluated the proposed GaN ICs implemented in a synchronous rectifier (SR) buck converter. Measurement results show that the proposed GaN ICs succesfully operated. The GaN IC with half-bridge configuration and MIM capacitor achieves higher efficiency and smaller voltage spike than the GaN IC without them.**

***Index Terms*—GaN HEMTs, monolithic integration, GaN-on-SOI, gate driver, false turn-on, reverse conduction loss, half-bridge**

I. Introduction

GaN HEMTs have the advantages such as high switching speed capability, zero recovery loss and low on-resistance compared to Sillicon (Si) power devices [1]. GaN HEMTs are suitable for power converters with bridge configuration such as a synchronous rectifier (SR) buck converters because of no p-n junctions between drain and source terminals [2]. Thanks to superior characteristics of GaN HEMTs, switching and conduction losses can be reduced. Since power converters implemented GaN HEMTs can operate at high frequency, passive elements such as capacitors and inductors can be replaced smaller ones, resulting in downsizing the circuit area and improving the power density.

However, in bridge circuits, GaN HEMTs have some problems such as false turn-on due to the low threshold voltage V_{th} and high-speed switching [3]. If the false turn-on occurs, the shoot-through current flows. This can cause a large amount of power loss and overheating. In the worst case, GaN HEMTs may break down. In the conventional gate driving method, negative voltage is applied to the gate terminal during off-state to suppress false turn-on [4]. This method improves the tolerance to voltage oscillations by increasing the margin between V_{th} and the gate-source voltage during off-state. However, it requires an additional power supply for negative voltage, resulting in increasing the circuit area. Moreover, negative V_{GS} increases reverse conduction loss due to the I_{D}-V_{DS} curve unique to GaN HEMTs [5]. In the previous work, a multilevel gate driver is proposed [6]. Since it uses a capacitor as a negative voltage supply, no additional voltage supply is required to apply negative voltage. After applying negative voltage, V_{GS} goes back to 0 V gradually, reducing the reverse conduction loss. It is possible to suppress false turn-on and reduce reverse conduction loss at the same time by using a single voltage supply and a single control signal.

Monolithic integration of power GaN HEMTs with a gate driver, to take advantages of the lateral structure, is promising to reduce parasitic inductance [7]. In a conventional implementation consisting of discrete components, switching speed is restricted by gate resistance to suppress the switching noise induced by parasitic inductance from packaging and PCBs. On the other hand, GaN integrated circuit (GaN IC) can minimize parasitic inductance since the power HEMT and the gate driver on a same die. Therefore, it can utilize high-speed switching capability of GaN HEMTs, resulting in improving power conversion efficiency.

In this work, we monolithically integrated a multilevel gate driver and a power HEMT by GaN-on-SOI process [8]. To further improve efficiency, we also fabricated another type of a GaN IC which integrates two power HEMTs for half-bridge configuration and a multilevel gate driver with an MIM

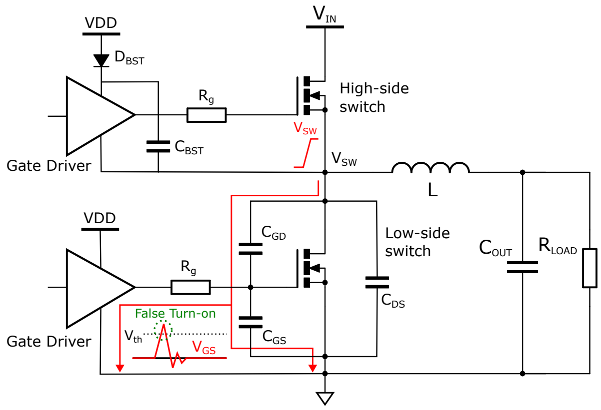

Fig. 1. The mechanism of the false turn-on in a SR-buck converter.

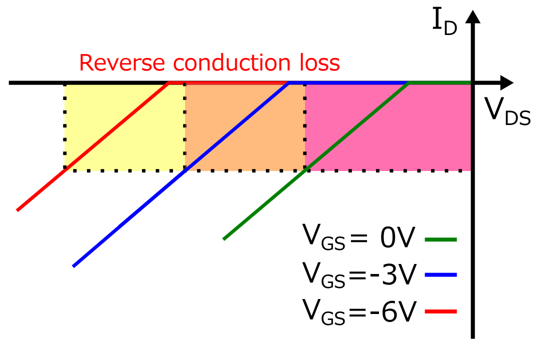

Fig. 2. I_D-V_DS characteristics of GaN HEMTs in the third quadrant.

capacitor. Measurement results show that the proposed GaN ICs have capability to prevent false turn-on. The GaN IC with half-bridge configuration and the MIM capacitor achieves higher efficiency and lower voltage spike than the GaN IC without them.

This paper is organized as follows. We explain issues of GaN HEMTs and related works in Section II. Section III presents proposed GaN integrated circuit (GaN IC). Section IV shows measurement results and Section V conclude this work.

II. Issues of GaN HEMTs and Related Works

A. False turn-on

A half-bridge configuration is used in many types of power converters. In these circuits, an unintentional turn-on due to the Miller effect, called the false turn-on, is a serious problem in terms of power loss and power device failure. When the false turn-on occurs, a shoot-through current flows across the channels of both power devices of the half-bridge configuration. This can cause additional power loss and damage to power devices.

Fig. 1 shows the mechanism of the false turn-on in an SR-buck converter. When the high-side switch turns on during off-state of the low-side switch, high positive dV/dt is generated at the switching node of the half-bridge configuration. This induces the Miller current I_Miller flowing the gate and source terminals of the low-side switch through the Miller capacitor C_GD. The Miller current flowing to ground through the gate resistor R_g and the gate driver generates some amount of positive voltage spike at the gate terminal. If the voltage spike exceeds V_th, the low-side switch turns on unintentionally.

V_th of GaN HEMTs is typically lower than that of Si and SiC MOSFETs. In addition, GaN HEMTs generate a higher dV/dt due to their high switching speed capability. This lead to a larger voltage spike. Therefore, GaN HEMTs are more likely to cause the false turn-on. In the conventional gate driving method to prevent the false turn-on is to apply a negative voltage to the gate terminal of the low-side switch during off-state. This method increases the margin between off-state drive voltage and V_th, improving the tolerance to the voltage spike.

B. Reverse conduction loss

Si and SiC MOSFETs have a parasitic diode , called a body diode, between the source and drain terminals that provides a path for reverse conduction current. In the reverse conduction mode, drain current I_D flows through the body diode, so the drain to source voltage V_DS is equal to the forward voltage of the body diode. In contrast, GaN HEMTs have no body diode. However, GaN HEMTs behave like a diode in the reverse conduction mode, allowing reverse conduction current to flow from source to drain through the channel [9].

Since GaN HEMTs have a lateral structure, when gate-drain voltage V_GD exceeds their threshold voltage $V_\mathrm{th,GD}$, the channel is formed as when V_GS exceeds V_th. V_GD is expressed as:

$$V_\mathrm{GD} = V_\mathrm{GS} - V_\mathrm{DS}. \tag{1}$$

When current flows to GaN HEMT from source terminal, parasitic capacitor C_GD and C_DS are charged. After V_GD reaches $V_\mathrm{th,GD}$, the channel is formed and reverse conduction current flows through the channel. In the reverse conduction mode, V_GD is typically approximately the equal to $V_\mathrm{th,GD}$. The voltage drop across source and drain V_SD is as:

$$V_\mathrm{SD} = V_\mathrm{th,GD} - V_\mathrm{GS} + R_\mathrm{SD} \cdot I_\mathrm{D}, \tag{2}$$

where R_SD is the effective channel resistance. V_SD is increased by applying negative voltage during off-state. Fig. 2 shows I_D-V_DS characteristics of GaN HEMTs in the third quadrant.

In an SR-buck converter, the reverse conduction loss during dead time P_DT is expressed as:

$$P_\mathrm{DT} = V_\mathrm{SD} \cdot I_\mathrm{OUT} \cdot T_\mathrm{DT} \cdot f_\mathrm{SW}, \tag{3}$$

where I_OUT is the output current, f_SW is the operation frequency and T_DT is the length of dead time. I_D and I_OUT are approximately equal in the reverse conduction mode. In the same I_OUT, applying negative V_GS increases V_SD. This leads to increase the reverse conduction loss during the dead time. Therefore, it is undesireble for GaN HEMTs to drive by negative voltage during off-state.

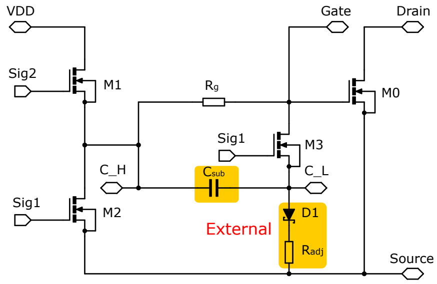

Fig. 3. Schematic of the proposed GaN IC.

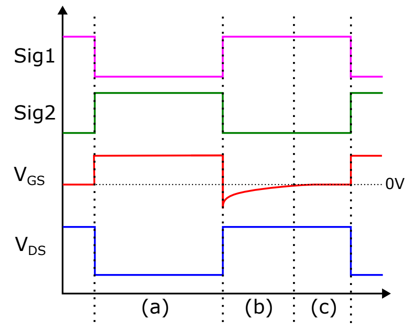

Fig. 4. Control waveforms of the multilevel gate driver on the GaN ICs.

C. Related works

There is a trade-off between preventing the false turn-on and increasing reverse conduction loss. To overcome the trade-off, various gate drivers are proposed [10] [11] [12]. In [10], a gate driver with a negative turn-off bias voltage is proposed. It generates a negative voltage internally by a charge pump consisting of one resistor, one capacitor, two diodes and two transistors. However, the circuit is more complex. In [11], a capacitor-based three-level gate driver is proposed. This gate driver consists of six transistors and one capacitor. Since the capacitor works as a negative voltage source, no additional voltage source is required. In [12], a three-level gate driver and a power HEMT are integrated monolithically, expanding on [11]. However, the three-level gate driver needs an additional control signal. In [13], a negative voltage self-recovery driver is proposed. It consists of passive components only, and the structure is simple. However, the verified operating frequency is 100 kHz. The losses of the gate driver may increase at higher frequency.

These gate drivers apply negative voltage at turn-off. After the period when the false turn-on may occur, V_{GS} goes to 0 V to reduce reverse conduction loss. This gate driving method is effective to establish both suppressing false turn-on and reducing reverse conduction loss. Moreover it speeds up the turn-off transient and reduces switching loss at turn-off.

III. Proposed GaN Integrated circuit

A. Structure and operation principle of the GaN IC

Fig. 3 shows the schematic of the proposed GaN IC. It integrates a multilevel gate driver and a power HEMT. C_{sub} and R_{adj} are connected externally to adjust the negative voltage by changing their value. Since the forward voltage of D_1 should be low, D_1 is also connected externally.

Fig. 4 shows the control waveforms of the multilevel gate driver on the GaN ICs. The operation principle of the multilevel gate driver is as follows (Fig. 5).

(a) Current flows along the gate terminal, the power HEMT turns on. During on-state, current flows through C_{sub} and energy is stored in C_{sub}.

(b) Current flows to the ground through C_{sub}, the power HEMT turns off. C_{sub} works as a negative voltage supply. The power HEMT is driven by negative voltage to suppress false turn-on.

(c) Current flows from C_{sub} to the gate terminal and then C_{sub} is discharged. V_{GS} gradually goes back to 0 V. It leads to reduce reverse conduction loss in the dead time before turn on.

The multilevel gate driver can operate at negative bias turn-off without any additional voltage source, owing to C_{sub}. Since only n-channel devices can be used for GaN ICs, the control signal for M1 must invert the others. Although monolithic integration increase control signals, the control of the multilevel gate driver is simple due to ease of signal generation.

C_{sub} works as a negative voltage source during turn-off transient. C_{sub} must discharge during off-state in order to sufficiently reduce reverse conduction loss during dead time before turn-on. Since the recommended negative voltage for suppressing the false turn-on is about -2.5 - -3 V, C_{sub} is set to nF or more. R_{adj} adjust the charge time of C_{sub}. R_{adj} need to be set considering the negative voltage.

The characteristics of the multilevel gate driver compared with related works are summarized in Table I. It can be seen that the gate driver of this work have the advantages of simple control signals despite monolithic integration and fewer elements to generate negative voltage.

In order to improve the efficiency, we also fabricated another type of a GaN IC as shown in Fig. 6. It additionally integrates a MIM capacitor and a power HEMT for half-bridge configuration. By integrating half-bridge configuration, parasitic components of the main circuit are suppressed. It will lead to improve conversion efficiency. By integrating the MIM capacitor, Miller current flows through the MIM capacitor instead of an external capacitor with large parasitic inductance. Therefore, the proposed half-bridge GaN IC (HB-GaN IC) is expected to reduce gate voltage spike come from Miller effect, resulting in improving the tolerance of the false turn-on.

B. Fabrication and layout of the GaN IC

The GaN ICs ware fabricated using 200 V GaN-on-SOI process. Fig. 7 shows the cross section of the enhancement p-GaN HEMTs on GaN-on-SOI substrates. The HEMTs can be isolated from the substrate and from each other by buried oxide (BOX) and a deep trench filled with SiO_2. A deep contact connecting the source terminals to their respective Si

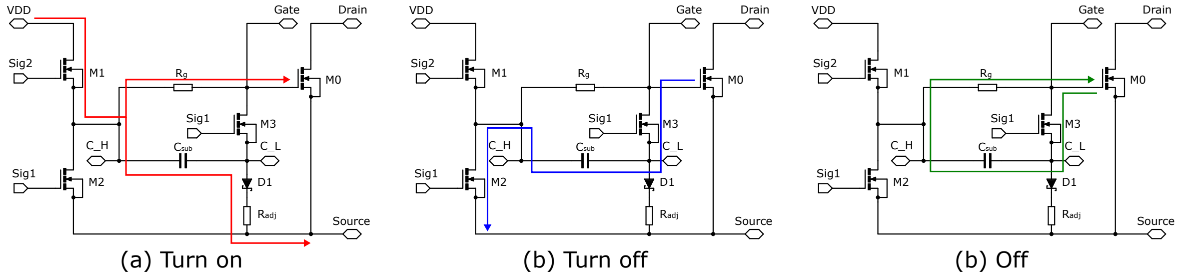

Fig. 5. Principle operation of the multilevel gate driver.

TABLE I
COMPARISON WITH RELATED WORKS.

	This work	[12]	[10]	[11]	[13]
Implementation	monolithic	monolithic	discrete	discrete	discrete
Power supply	1	1	1	1	1
Control signal	2	3	1	2	1
Negative voltage elements	3	5	6	5	6
Operating frequency	1 MHz	1 MHz	100 kHz	1 MHz	100 kHz

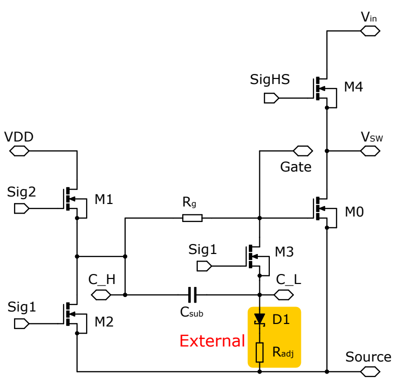

Fig. 6. Schematic of the GaN IC with a MIM capacitor and half-bridge configuration.

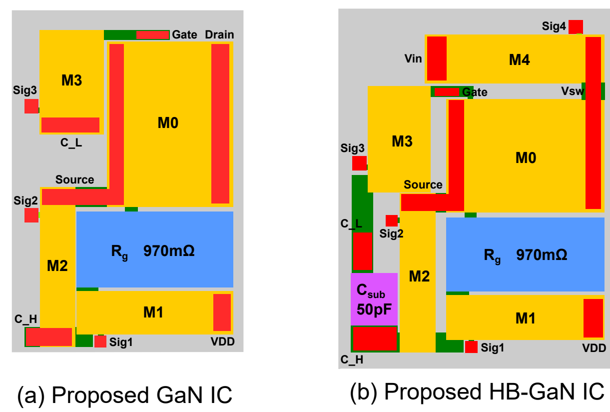

Fig. 8. Layout of GaN ICs

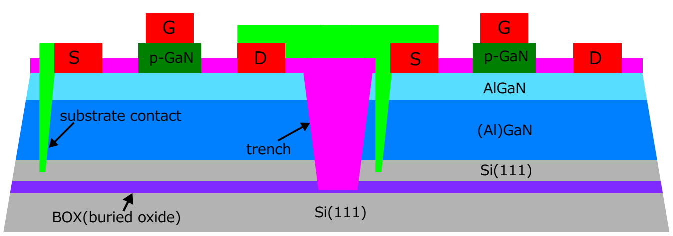

Fig. 7. Cross section of two isolated HEMTs by GaN-on-SOI process.

TABLE II
GATE WIDTH OF THE GAN IC.

	M0	M1	M2	M3	M4
W_g [mm]	86	32	25	23	42

layer on the BOX realize a local substrate contact. The oxide isolation and the local substrate contact provide zero volt bulk-source potential locally, resulting in suppressing back-gating effects [8]. Therefore, GaN-on-SOI technology is suitable for monolithic integration of half-bridge configuration.

The layout and gate width W_g of the GaN ICs are shown in Fig. 8 and Table II, respectively. The integrated gate resistor is 970 mΩ on both GaN ICs and the integrated MIM capacitor on the HB-GaN IC is 50 pF. According to the previous work [7], 50 pF is not enough as a negative voltage supply to suppress the false turn-on. To compensate for the lack of C_{sub}, an external ceramic capacitor is connected in parallel with the integrated MIM capacitor.

IV. MEASUREMENT RESULTS

To evaluate and compare the tolerance for the false turn-on phenomenon, and power conversion efficiency, the proposed GaN ICs are implemented on the 48 V-to-12 V SR-buck converter. Fig. 9 shows a simplified schematic of the SR-buck converter. The parameters of the SR-buck converter are shown in Table III. The tolerance of the false turn-on is evaluated by the margin voltage V_{margin} between V_{th} and the peak of the voltage spike at the gate voltage of low-side switch V_{GL}.

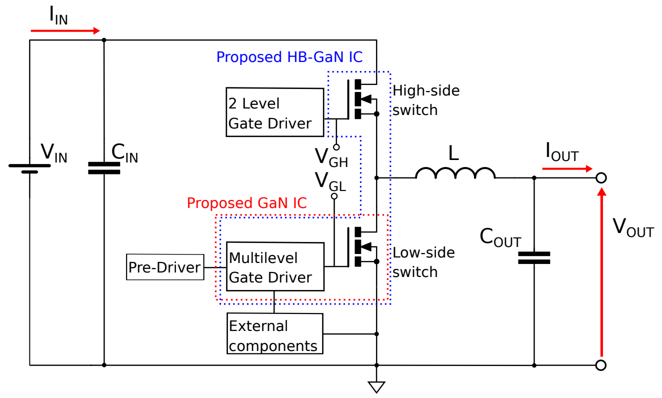

Fig. 9. Simplified schematic of SR-buck converter.

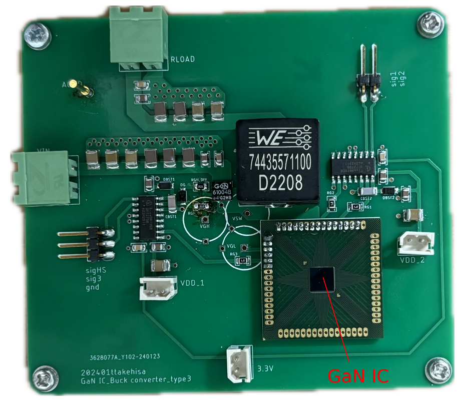

Fig. 10. The SR-buck converter using the proposed GaN IC.

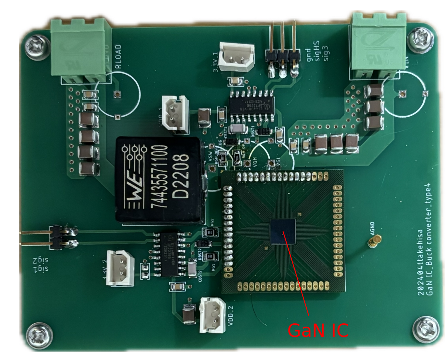

Fig. 11. The SR-buck converter using the proposed HB-GaN IC.

TABLE III
PARAMETERS OF SR-BUCK CONVERTER.

Input voltage	V_{IN}	48 V
Output voltage	V_{OUT}	12 V
frequency	f_{SW}	1 MHz
Dead time	t_{DT}	30 ns
Power	P	12 W
Inductor	L	10 µH
Input capacitance	C_{IN}	44 µF
Output capacitance	C_{OUT}	29 µF

TABLE IV
PARAMETERS OF SR-BUCK CONVERTER.

	Proposed GaN IC	Proposed HB-GaN IC
V_{IN} [V]	48.4	48.1
I_{IN} [mA]	273	269
V_{OUT} [V]	12.1	12.0
I_{OUT} [mA]	963	972
P_{IN} [W]	13.2	12.9
P_{OUT} [W]	11.7	11.7
Efficiency	88.6%	90.7%

The external capacitor C_{sub} and the resistor R_{adj} are 22 nF and 22 Ω, respectively. The external diode $D1$ is schottky barrier diode. The GaN HEMT GS61004B (GaN systems) was used for the high-side switch when using the GaN IC without integrated high-side switch. The dual-channel gate drivers IC for the high-side switch and pre-driver for the GaN IC were 2EDF7275F (Infineon). The high-side switch was driven by a conventional 2-level method. The control signal is generated by Analog Discovery2 (Digilent Inc.). The oscilloscope used for the experiment is MSO56B (Tektronix). The photograph of the SR-buck converter is shown in Fig. 10 and Fig. 11.

Fig. 12 and Fig. 13 show the magnified measurement waveforms of gate voltages when the proposed GaN IC and the proposed HB-GaN IC are implemented, respectively. When using the propsed GaN IC, the peak of the voltage spike of V_{GL} is 1.34 V. Since the typical V_{th} of the integrated power HEMT is 2.5 V, the peak of the voltage spike do not exceed V_{th}, preventing the false turn-on. V_{margin} is 1.16 V. On the other hand, When using the propsed HB-GaN IC, the peak of the voltage spike of V_{GL} is 0.86 V. V_{margin} is 1.4 times larger than using the GaN IC without high-side switch and MIM capacitor. This is because integrated MIM capacitor provide the current path with smaller parasitics compared to the GaN IC without MIM capacitor. Therefore, the voltage spike caused by the Miller current can be suppressed by integrating MIM capacitor.

Table IV shows measurement results of the SR-buck converter. The efficiency of the SR-buck converter using the proposed GaN IC is 88.6%, while the proposed HB-GaN IC is 90.7%. The HB-GaN IC improve conversion efficiency by 2.1%. This is because parasitic components of the main circuit are suppressed by integrating even the high-side switch of the half-bridge configuration.

From the measurement results, the proposed GaN ICs suppress the false turn-on without any additional voltage supply. Furthermore, it is demonstrated that integrating half-bridge configuration and MIM capacitor improves conversion efficiency and tolerance of the false turn-on.

V. CONCLUSION

In this paper, we propsed monolithic GaN IC which integrates a multilevel gate driver and a power HEMT to improve performance of power converters. The multilevel gate driver can prevent from the false turn-on and reduce the reverse conduction loss during dead time before turn-on with a single voltage supply and simple control signals. In order

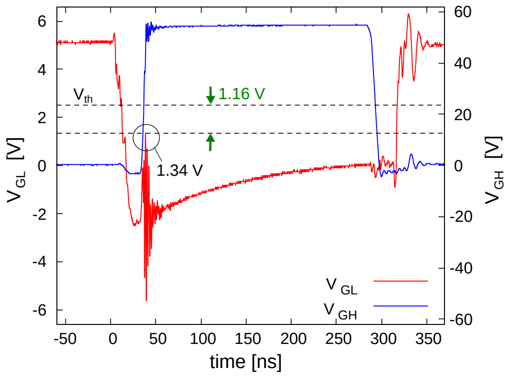

Fig. 12. Magnified measurement waveform of gate voltages using the proposed GaN IC.

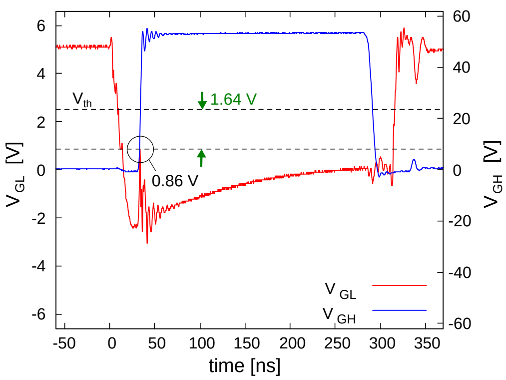

Fig. 13. Magnified measurement waveform of gate voltages using the proposed HB-GaN IC.

to further improve efficiency, we also fabricated another type of a GaN IC which integrates two power HEMTs for half-bridge configuration and a multilevel gate driver with a MIM capacitor. In the 48 V-to-12 V SR-buck converter with output power 12W, proposed GaN ICs can suppress the false turn-on. When using the HB-GaN IC, the tolerance of the false turn-on is 1.4 times larger than when using the GaN IC without the half-bridge configuration and the MIM capacitor. Furthermore, the HB-GaN IC improve the efficiency by 2.1%.

ACKNOWLEDGMENT

This work was supported by the European Union's Horizon 2020 project ASCENT+, grant agreement no. 871130.

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