(Invited Paper) Physics-based Modeling to Extend a MOSFET Compact Model for Cryogenic Operation

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Abstract

This paper extends the low-temperature modeling capabilities of an industry-standard compact metal-oxide-semiconductor field-effect transistor (MOSFET) model by incorporating physics-based representations of cryogenic effects in semiconductors. Specifically, the incomplete dopant ionization effect is integrated into the bulk Fermi potential calculation of the compact model and applied as a threshold voltage shift in the formulation of Poisson's equation. Temperature-related models for bandgap energy, saturation velocity, and contact resistance at the source/drain regions are also enhanced. Using transistors fabricated with 22 nm process technology, we demonstrate that this consistent modeling approach accurately reproduces current-voltage and threshold voltage-temperature characteristics across a temperature range from 300 K to 4 K.

CCS Concepts

• **Hardware → Modeling and parameter extraction**.

Keywords

Cryo-CMOS, Compact model, Cryogenic, HiSIM, Incomplete dopant ionization, Bandgap energy, Saturation velocity, Contact resistances

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1 Introduction

Operating complementary metal-oxide-semiconductor (CMOS) devices at cryogenic temperatures offers advantages such as improved device current, steeper sub-threshold slope (SS), and reduced thermal noise [4, 17, 33]. These benefits have fueled advancements in high-performance computing and deep space exploration [8–10]. In addition, CMOS-based circuits capable of operating at cryogenic temperatures to control and read out qubit information have been intensively discussed in the scaling of quantum computers [28, 30, 31]. While the theoretical foundations of semiconductor behavior at low temperatures are well established [7, 11, 12, 15, 27], tranlating these theories into practical compact models for circuit simulation remains a significant challenge [5, 14, 19, 29].

Current industry-standard metal–oxide–semiconductor field-effect transistor (MOSFET) models [1, 16, 26] used in commercial circuit simulators are limited to reproducing I-V characteristics at temperatures down to approximately 150 K. These models are unsuitable for simulations at cryogenic temperatures (as low as 4 K) because the implemented physical models do not fully account for physical phenomena, such as incomplete dopant ionization that occur at these low temperatures.

The Hiroshima University STARC IGFET (HiSIM) model is a compact MOSFET model developed for bulk-CMOS [26]. This model describes the electrical characteristics of the device based on source and drain surface potentials, derived by iteratively solving Poisson's equation. By using the surface potentials, HiSIM achieves a consistent description of current and capacitance characteristics, enabling the direct implementation of advanced modeling features such as device degradation and aging effects [20]. HiSIM is also scalable with device length (L) and width (W), minimizing the need for parameter binning and facilitating predictive analysis of process and technology variations [3, 25]. Furthermore, due to its surface potential-based formulation, HiSIM has been effectively extended to model other MOS device structures, such as high voltage (HV) [23] and silicon-on-insulator (SOI) [24] has been well established as standardized compact models.

Despite these advantages, HiSIM, like other existing industry-standard compact models, is limited in reproducing current-voltage (I-V) characteristics at temperatures below approximately 150 K as shown in Fig. 1, in comparison with device simulation results obtained using a 0.4 μm technology. Although the model accurately reproduces the $I_{\rm ds}$-$V_{\rm gs}$ characteristics at room temperature (T = 300 K), it fails to predict subthreshold current and threshold voltage ($V_{\rm th}$) characteristics at temperatures below 150 K. Theoretically, at low temperatures, the intrinsic carrier concentration decreases drastically (by approximately 10^{-250}), as also confirmed by the HiSIM calculation in Fig. 2(a). The resulting bulk Fermi potential exhibits an unphysical dip near 4 K as shown in Fig. 2(b).

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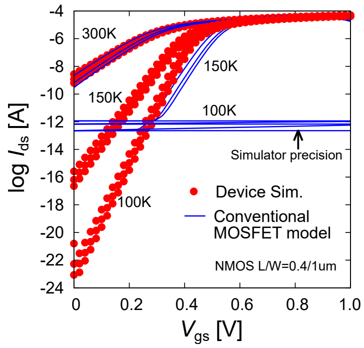

Figure 1: Example of conventional MOSFET compact models failing to predict current characteristics at or below 150 K, as the incorporated physical models do not account for low-temperature effects.

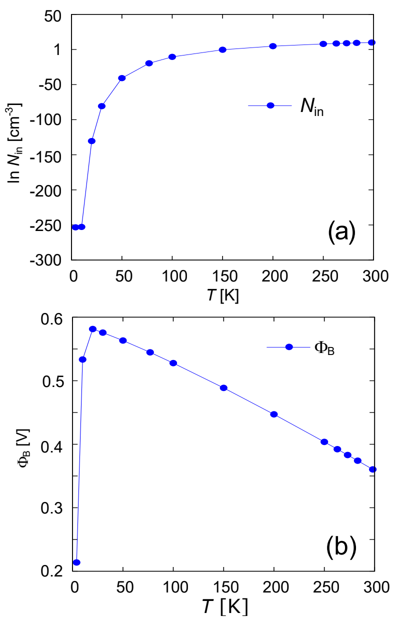

Figure 2: (a) As-calculated intrinsic carrier concentration and (b) bulk Fermi potential using a conventional MOSFET compact model without incorporating cryogenic temperature effects.

One approach to account for the cryogenic effects is to include incomplete ionization in the surface potential formulation, which requires developing a new model core [6, 22, 34]. Other approaches involve introducing temperature-related parameters for the flat-band voltage to model the temperature effects on $V_{\rm th}$ [21]. Additionally, laterally diffused MOS (LDMOS) type transistors have also been modeled with low-temperature effects on the drift region [18].

In this paper, we extend HiSIM by including the incomplete ionization effect in the calculation of the Fermi bulk-potential, as well as in the threshold voltage shift ($\Delta V_{\rm th}$) that is solved in Poisson's equation. Owing to its surface potential formulation, the implementation of these physical changes due to low-temperature effects is straightforward. Enhancements are also made to the temperature-dependent models for bandgap energy, saturation velocity, and source/drain resistances. The reproduction of I-V and $V_{\rm th}$-T characteristics from T=300 K to 4 K is verified using an nMOS transistor fabricated with a commercial 22 nm technology.

The remainder of this paper is organized as follows. Section 2 provides an overview of the HiSIM model, and Section 3 describes the extensions implemented in HiSIM to consider changes in the cryogenic I-V characteristics. Section 4 presents the application of the proposed model to the I-V characteristics of nMOS transistors fabricated by 22 nm-process technology at 4 K. Finally, we conclude the paper in Section 5.

2 Surface-potential-based model HiSIM

In HiSIM [26], the surface potential ($\phi_{\rm s}$) is calculated to derive the electrical characteristics of the MOSFET from Poisson's equation by utilizing Gauss's law as follows[1]:

$$\begin{aligned}
&C_{\rm ox}(V_{\rm G}^{'} - \phi_{\rm S}(y)) = \sqrt{\frac{2\epsilon_{\rm Si} q N_{\rm sub}}{\beta}}\,[\exp\{-\beta(\phi_{\rm S}(y) - V_{\rm bs})\} \\
&+ \beta(\phi_{\rm S}(y) - V_{\rm bs}) - 1 \\
&+ \frac{n_{\rm p0}}{p_{\rm p0}}\{\exp(\beta(\phi_{\rm S}(y) - \phi_{\rm f}(y))) - \exp(\beta(V_{\rm bs} - \phi_{\rm S}(y)))\}]^{1/2},
\end{aligned} \tag{1}$$

where

$$C_{\rm ox} = \frac{\epsilon_0 \mathbf{KAPPA}}{\mathbf{TOX}},$$
$$V_G^{'} = V_{\rm gs} - V_{\rm FB},$$
$$\beta = \frac{q}{kT}, \quad \text{and}$$
$$n_{\rm p0} = \frac{n_{\rm i}^2}{p_{\rm p0}}.$$

Here, ϵ_0 is the permittivity of a vacuum, **KAPPA** is the gate oxide permittivity, **TOX** is the oxide thickness, β is the inverse of the thermal voltage, q is the electric charge, and k is the Boltzmann constant. $p_{\rm p0}$ and $n_{\rm p0}$ are the hole and electron concentrations at equilibrium, respectively. $V_{\rm FB}$ is the flat-band voltage, equivalent to model parameter **VFBC**. $V_{\rm gs}$ and $V_{\rm bs}$ refer to the gate-source and bulk-source voltages, respectively. HiSIM solves Eq. (1) for $\phi_{\rm s}$ through an iterative approach, using the calculated surface potentials at the source and drain to determine the MOSFET current and capacitance characteristics.

The intrinsic carrier concentration ($n_{\rm i}$) is described as follows:

$$n_{\rm i} = n_{\rm i0} T^{3/2} \exp\left(-\frac{E_{\rm g}}{2}\beta + \frac{E_{\rm g,TNOM}}{2}\beta_{\rm TNOM}\right), \tag{2}$$

where the bandgap energy ($E_{\rm g}$) is expressed as:

$$\begin{aligned}
E_{\rm g} &= E_{\rm g,TNOM} - \mathbf{BGTMP1}(T - \mathrm{TNOM}) \\
&\quad - \mathbf{BGTMP2}(T^2 - \mathrm{TNOM}^2),
\end{aligned} \tag{3}$$

where $E_{\rm g,TNOM}$ is the bandgap energy value at the nominal temperature (**TNOM**) and is expressed as follows:

$$E_{\rm g,TNOM} = \mathbf{EG0} - 90.25 \times 10^{-6}\mathrm{TNOM} - 1 \times 10^{-7}\mathrm{TNOM}^2. \tag{4}$$

[1]Hereafter, the model parameters are represented in bold texts.

Table 1: Introduced model parameters for applicability at cryogenic temperatures

Parameter	Description	Section
NSUBCIONT	Impurity ionization energy effects at high doping	3.1
EIONFAC	Ionization energy coefficient	3.1
VTHTEMPC	Incomplete ionization coefficient on V_{th}	3.1
VBITEMP	Built-in voltage temperature dependence	3.2
VMAXT1	Saturation velocity temperature dependence	3.3
RDTEMP1	Drain contact resistance temperature dependence	3.4
RSTEMP1	Source contact resistance temperature dependence	3.4

EG0 is set to 1.1785 eV, and **BGTMP1** and **BGTMP2** are the model parameters to capture the temperature dependence.

The effects of advanced MOSFET technologies, such as short-channel, pocket implantation, and vertical doping inhomogeneity, are incorporated as a shift of the threshold voltage ΔV_{th} and included in the effective gate voltage V'_G as follows:

$$\Delta V_{th} = \Delta V_{th,SC} + \Delta V_{th,P} + \Delta V_{th,VD} \tag{5}$$

and

$$V'_G = V_{gs} - V_{FB} + \Delta V_{th}. \tag{6}$$

V'_G is used in the solution of Poisson's equation. This approach facilitates the consistent incorporation of the aforementioned effects of technological advancements. The bulk potential (Φ_B) is given by

$$\Phi_B = \frac{1}{\beta} \ln\left(\frac{N_{sub}}{n_i}\right), \tag{7}$$

where N_{sub} is the substrate impurity concentration and is equal to the model parameter **NSUBC**.

3 Extension for cryogenic temperatures

To simulate the current characteristics at cryogenic temperatures using HiSIM, we developed four extensions: incomplete dopant ionization, built-in potential, saturation velocity effects, and contact resistances. The model parameters newly introduced in the extensions are listed in Table 1.

3.1 Incomplete dopant ionization

The incomplete dopant ionization at low temperatures can be accounted for by introducing a temperature-dependent degeneracy factor to the ionized donor N_D^+ and acceptor N_A^- concentration [13]. For N_A^-, the Fermi potential with incomplete ionization ($\Phi_{B,FI}$) is formulated as follows [7]:

$$n_i \exp\left(\beta \cdot \Phi_{B,I}\right) = \frac{N_A}{1 + \left(g_A \exp\left(\beta(\Phi_{B,I} - \Phi_A)\right)\right)}, \tag{8}$$

where N_A is the acceptor concentration, and g_A is the degeneracy factor: 2 for the donor and 4 for the acceptor. Φ_A relates to the difference between intrinsic and acceptor energy levels.

The solution of Eq. (8) leads to

$$\Phi_{B,I} = \Phi_B - \Delta\Phi_{FO}, \tag{9}$$

$$\Delta\Phi_{FO} = \frac{1}{\beta} \ln\left(\frac{1 + \sqrt{1 + 4\lambda \frac{\mathrm{NSUBC}}{n_i}}}{2}\right), \quad \text{and} \tag{10}$$

$$\lambda = g_A \exp\left(\beta E_D\right), \tag{11}$$

where E_D represents the ionization energy, which is modeled as

$$E_D = \mathbf{EIONFAC} \cdot \left(E_{D0} - \mathbf{NSUBCIONT} \cdot \mathbf{NSUBC}^{\frac{1}{3}}\right). \tag{12}$$

Here, $E_{D0} = 0.045$ eV with **NSUBCIONT** as a parameter denoting impurity concentration effects with a default value of 3.6×10^{-8} [11]. **EIONFAC** represents the ionization energy coefficient. Eq. (9) reveals that incomplete ionization reduces the Fermi potential at low temperatures, with the reduction also depending on the concentration of substrate impurities. The HiSIM model is extended by using the Fermi potential expressed in Eq. (9).

The MOSFET threshold voltage equation is related to the bulk potential as follows:

$$V_{th} = 2\Phi_B + \frac{1}{C_{ox}} \sqrt{4\varepsilon_{Si} q N_{sub} \left(2\Phi_B\right)} + V_{FB}, \tag{13}$$

wherein complete ionization is assumed. Owing to incomplete ionization, some compact models introduce temperature-dependent parameters into the flat-band voltage to account for temperature and N_{sub}.

In this work, the incomplete ionization effect is incorporated into the HiSIM model as a shift in the threshold voltage. Eq. (6) can be extended as follows:

$$V'_G = V_{gs} - V_{FB} + \Delta_{th} - \Delta\Phi_{BP,\,temp}, \tag{14}$$

$$\Delta\Phi_{BP,\,temp} = \mathbf{VTHTEMPC} \cdot \Delta\Phi_{FO}. \tag{15}$$

$\Delta\Phi_{FO}$ is derived in Eq. (10), and **VTHTEMPC** is a parameter introduced to compensate for the approximation.

3.2 Built-in voltage

The HiSIM model employs the built-in potential (**VBI**) of the junction vertical to the channel, which is constant and temperature independent. In the proposed model, the temperature dependence is modeled as follows:

$$\mathbf{VBI} = \mathbf{VBI} - \mathbf{VBITEMP} \cdot \left(\frac{T}{\mathrm{TNOM}} - 1\right), \tag{16}$$

where **VBITEMP** is the model parameter. T is the device temperature provided by the simulator, and TNOM is the nominal temperature.

3.3 Saturation velocity effects

The temperature dependence of the saturation velocity (**VMAX**) follows [32] and is expressed as follows:

$$\mathbf{VMAX} = \frac{\mathbf{VMAX}}{(1 - \mathbf{VMAXT1}) + \mathbf{VMAXT1} \cdot \left(\frac{T}{\mathrm{TNOM}} - 1\right)}, \tag{17}$$

where the numerator refers to the saturation velocity at the nominal temperature. **VMAXT1** is a parameter dependent on the material, which is employed in the model as a fitting parameter.

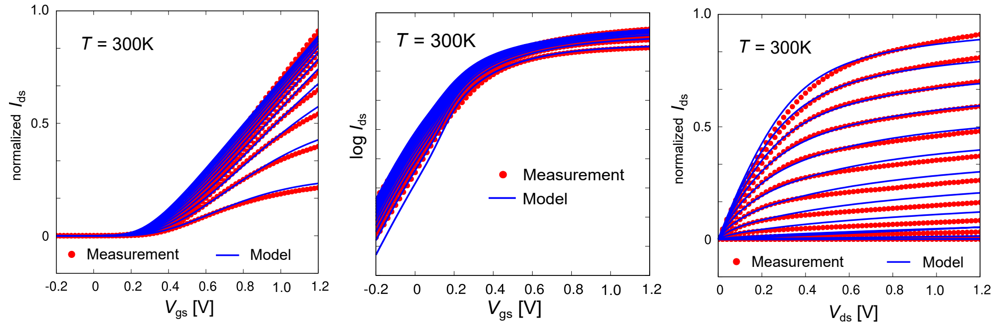

Figure 3: Results of HiSIM model in comparison with measurements at T=300 K.

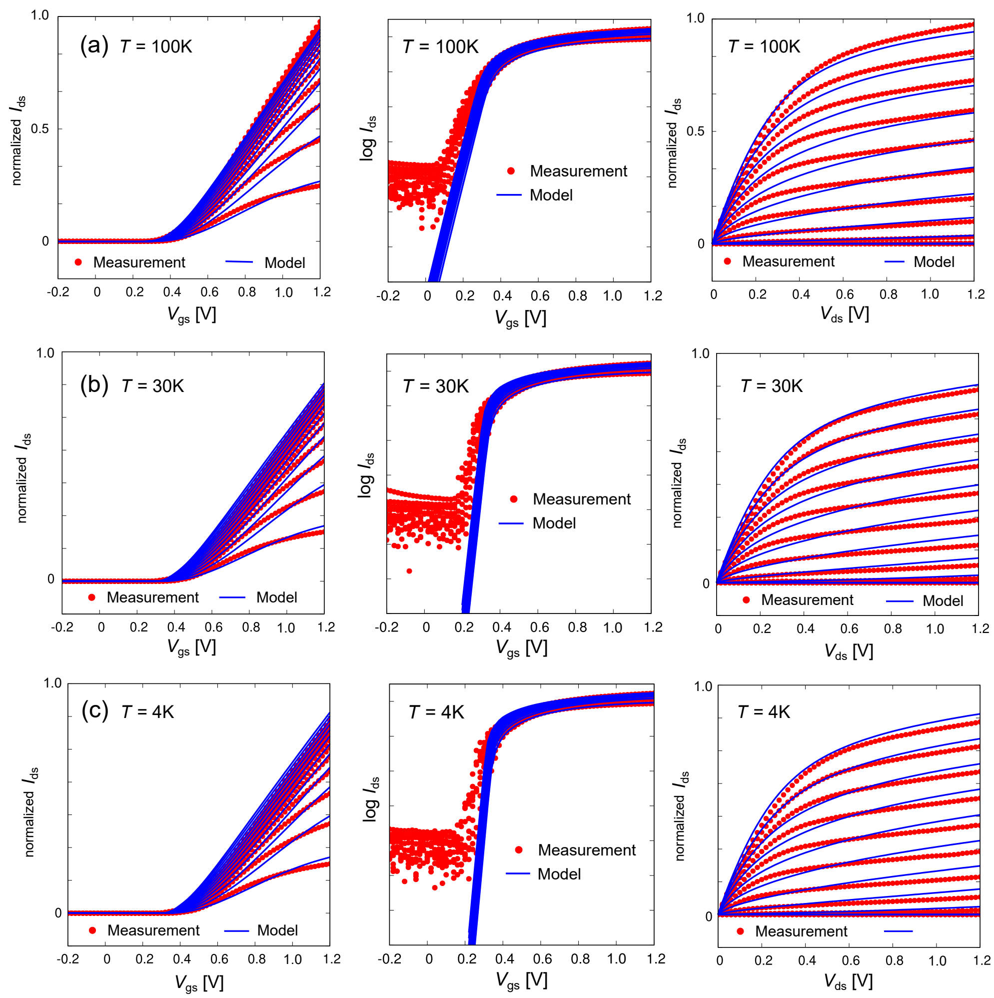

Figure 4: Results of extended HiSIM model, incorporating cryogenic effects, in comparison with measurements at T = (a) 100 K, (b) 30 K, and (c) 4 K.

3.4 Contact resistances

Aggressively scaled MOSFET devices exhibit significant effects due to the contact resistance of the drain and source (R_d and R_s, respectively). The temperature dependences of the contact resistances are modeled as follows:

$$R_d = \mathbf{RD} + \mathbf{RDTEMP1} \cdot \left(\frac{T}{\mathrm{TNOM}} - 1\right) \quad \text{and} \tag{18}$$

$$R_s = \mathbf{RS} + \mathbf{RSTEMP1} \cdot \left(\frac{T}{\mathrm{TNOM}} - 1\right), \tag{19}$$

where **RD** and **RS** are the resistances measured at the nominal temperature. **RDTEMP1** and **RDTEMP2** are the parameters used to capture the temperature dependence.

4 Model validation

The temperature-related models described in Section 3 were implemented as extensions to the Verilog-A code of HiSIM [2]. The extended HiSIM model was then compiled and verified using a commercial SPICE circuit simulator [35]. For verification, we compared the model's ability to fit the characteristics of an nMOS transistor fabricated with a 22 nm process technology. The device was electrically characterized at temperatures ranging from 300 K to 4 K using a cryostat with a liquid helium dewar. The measured I_{ds}-V_{gs} and I_{ds}-V_{ds} characteristics at 300 K are indicated by the red circles in Fig. 3[2]. To facilitate the fitting of the temperature-related characteristics, the HiSIM model parameters were first extracted with measurements at T=300 K. This parameter extraction includes effects such as short channel effect, mobility degradation, channel length modulation, and soft punch-through effects, all of which are originally modeled in HiSIM. Fig. 3 shows the model-fitting capability, including the *SS* characteristics.

The evaluation of the lower-temperature characteristics is described as follows. The V_{th}-T characteristics were initially fitted using E_g-related parameters: **BGTMP1** and **BGTMP2** in Eq. (4). The saturating V_{th} characteristics at low temperatures were reproduced owing to the incomplete ionization effect on the bulk-potential; the parameter **EIONFAC** modulates the ionization energy, and **NSUBCIONT** captures N_{sub} dependence. The extracted V_{th} was well replicated by the model, as shown in Fig. 5. A comparison of the bulk potentials calculated by the model for complete and incomplete ionization for N_{sub} = 5×10^{15} and 5×10^{16} cm^{-3} is presented in Fig. 6. The results show that incomplete ionization becomes discernible at lower temperatures and higher substrate impurity concentrations. Similarly, the parameter **VTHTEMPC** in Eq. (14) facilitates the V_{th} saturation.

The intrinsic carrier concentration n_i as expressed in Eq. (2) inherently results in an extremely small value because of the $T^{3/2}$ dependence and causes numerical issues in the surface potential calculation in Eq. (1). These numerical issues, governed by the precision of the circuit simulator, limit the precise calculation of the internal model variables [14]. In this work, as the measured V_{th} and *SS* attain saturation at ∼30 K as shown in Figs. 5 and 7, respectively, the model is set to have a saturation value at this temperature.

The temperature-dependence of *I*-*V* characteristics were fitted with the mobility at low V_{ds} using the conventional HiSIM model. At high V_{ds}, **VMAXT1** velocity was tuned for the saturation. The *SS*-*T* characteristics with saturation at 30 K is well replicated by the model, as shown in Fig. 7. The leak current, discernible at negative V_{gs} and extending to V_{gs} = 0.2 V at lower temperatures, is attributed to induced gate-drain currents, which influence the subthreshold characteristics but are not accounted for in the present model.

The validation results demonstrate that the extended HiSIM model successfully reproduces the current characteristics at cryogenic temperatures.

[2]Hereafter, the normalized magnitudes of measured currents and extracted threshold voltages are shown to maintain data confidentiality.

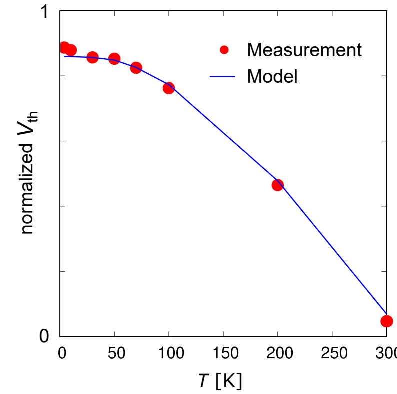

Figure 5: Extracted V_{th}-T characteristics from measurements and those reproduced using the extended HiSIM model.

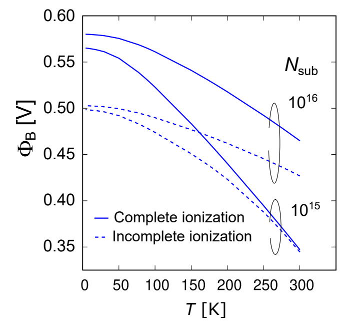

Figure 6: Bulk Fermi potential calculated using the extended HiSIM model.

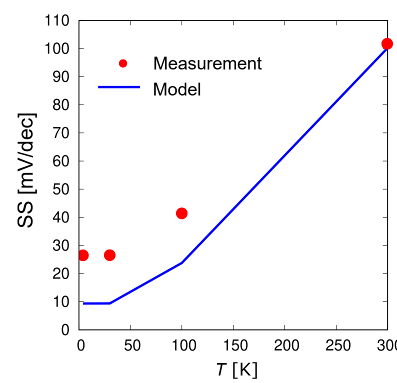

Figure 7: Extracted *SS*-*T* characteristics from measurements and those reproduced by the extended HiSIM model.

5 Conclusion

Compact MOSFET models that accurately capture device phenomena at low temperatures are crucial for designing integrated circuits aimed at cryogenic temperatures. In this paper, we extended the HiSIM model, enhancing it beyond standard models with ease due to its surface potential framework, making it well-suited for cryogenic circuit design. Models for incomplete dopant ionization, built-in voltage, saturation velocity effects, and contact resistance were implemented into the Verilog-A code of HiSIM and compiled in a commercial SPICE simulator. The evaluation of our model, using measurements of an nMOS transistor fabricated with 22 nm process technology, demonstrated its ability to accurately simulate drain current and threshold characteristics from 300 K to 4 K.

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