Extracting a Random Component of Variation from Measurement Results of a 90 nm LUT Array

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Abstract— From the measurement results of a 90 nm process, we propose a model of WID variations of reconfigurable devices. The model is separated into, four components, and we defined, 4th component, the residue of the former three component, as the random component. In this paper, we confirm whether, the residue of the three component is actually random from the viewpoint of skewness, kurtosis and spatial correlation.

I. INTRODUCTION

Problem of the variations is getting more serious as process scaling. Degradations of transistor performance by variations degrade the speed and yield of the LSIs. However, reconfigurable devices can utilize the WID variations by reconfiguration. First of all, we measure the WID variations of reconfigurable devices after manufacturing. Then, reconfigure optimally considering the WID variations. This method increases the performance of almost all reconfigurable devices and it results in the boosting yield and slashing the timing margin.

Modeling variations of reconfigurable devices is necessary to prove the effectivity of the proposed method. In this paper, we explain the variation model from the measurement results of a 90 nm LUT array and analyze the extracted random component.

II. 90 NM LUT ARRAY

90 nm LUT array is designed to measure the variations of reconfigurable structure. In this section, we explain the specifications of the chip and measurement results.

A. Chip Specifications

Fig. 1 shows the structure of a logic block (LB) which contains a 4-bit LUT and a scan flip-flop (SDFF). An LUT consists of 16 flip-flops to store an LUT configuration and five MUX4s (4-input multiplexers). The output signal **Mout** from the MUX4 is sent to the adjacent LUT. Fig. 2 shows the array structure of logic blocks in the fabricated chip. They are laid out in a fractal structure to observe scalable process variations. If they are laid out in a line, WID variations may be canceled. The fractal structure makes it possible to measure WID variations in scalable square regions.



Fig. 1. Structure of a logic block. A signal is transmitted along the dashed arrow through two MUX4s per LB at the measurement.



Fig. 2. Structure of the LUT array. LBs are connected in a fractal structure to observe scalable process variations.



Fig. 3. Chip micrograph of a 90nm LUT array LSI including 2,048 logic blocks located at the bottom.

On measuring the process variations, a signal is rushing through LUTs from the first LB in a square region, which is captured by the SDFF in each LB. LUTs are configured as follows during the measurement.

- The LUT in the first LB is configured to become true at any input value.
- The LUT in the second LB is configured to become true if the input **B** from the previous Sout becomes true.
- The LUTs in the other LBs are configured to become true only if the input **A** from **Mout** becomes true.

Applying a clock pulse to SDFFs under the above LUT configuration, **Sout** of the first LB becomes true, which is transmitted through LBs. During the transmission, let us apply another clock pulse to SDFFs. Then the SDFFs in the LBs where the true signal have been transmitted become true. If WID variations are observed, number of transmitted LBs will be different in each square region as shown in Fig. 2. Fig. 3 shows a micrograph of a fabricated LSI.

B. Measurement Results



In a single measurement, very little variations appear since the transistor speed is quantized as the number of LBs. To avoid the quantization and measure the difference clearly, clock cycle (time to transmission) is varied from 4.0ns to 8.0ns at 0.1ns interval. We repeat it 100 times per cycle at the resolution of 16 (4×4) LBs. The average value of 100 results is regarded as the number of transmissions at the cycle. By setting the clock cycle on the horizontal axis and the average number of transmissions on the vertical axis, the gradient is calculated using the least square method. The gradient depends on the performance of each block of LBs. The ratio of the gradients is equivalent to the ratio of the speeds. We can regard these gradients as the performance indicator.

Fig. 4 shows the statistic of WID variations from a fabricated chip. The peripheral LBs tend to be fast and the central LBs are slow. The other 24 chips have the same



Fig. 4. Statistics of a fabricated dice by regarding the gradient from the least square method as the performance indicator. Peripheral LBs are fast and central ones are slow.

tendency. Averaging the WID variations from every chip, we obtain the D2D variations represented in Fig. 5.



Fig. 5. Observed D2D variations of 25 dice, which are the average WID variations Θ_{k} every chip.

III. VARIATION MODEL FROM THE MEASUREMENT RESULTS

From the measurement results, we propose a model of WID variations of reconfigurable devices separated into the following four components.

| (Performance of a Chip) | |
|---|-------|
| = (1. Typical Performance) | |
| + (2. Systematic Component across the Waf | er) |
| + (3. WID Systematic Distributions from all | Chips |
| + (4. Random Component) | (1 |

The typical performance component is the device original performance with no variations. We define this component as the average performance of all chips, all part of the chips

Fig. 6 explains the systematic component from D2D variations. Because the systematic variations are smooth across the wafer [1, 2], we model the systematic variations on the wafer from the measured D2D variations by the response surface methodology as in Fig. 6. Then, we define the part of the curved surface corresponding a chip as the WID systematic variations. However, locations of the LUT array LSI on the wafer are unknown. So in this paper we assume the systematic variations is completely flat within a die because the systematic variations change smoothly across the wafer and the area of LUT array is very small, only 1mm². It means that we regard the systematic component from D2D variations as just the measured D2D variations.

Average distributions on the chips, which represents the tendencies written in section 2, is obtained from averaging the measurement results on each part of the chip. The distributions contain the effect of IR drops, layout dependent variations, location dependent variations, clock skew and so on, which affect all chips in the same way.

We regard the residue of three component as the random component and use the normal distributed pseudorandom numbers for modeling the component. In section 4, we analyze whether the residue is actually random.



Fig. 6. Model of the systematic component on the wafer. We guess the systematic variations from the D2D variations by the response surface methodology.

IV. ANALYSIS OF THE RANDOM COMPONENT

In this section, we analyze whether the residual component is actually random and can be modeled by the normal distributed pseudorandom numbers from the viewpoint of skewness, kurtosis and spatial correlation.

A. Skewness and Kurtosis

Skewness and Kurtosis are important values of the probability distribution. Both values represent the shape of distribution.

Skewness, written as α_3 and defined by the following equation, is a measure of the asymmetry.

$$\alpha_3 = E(X-\mu)^3/\sigma^3 \tag{2}$$

 μ is the expectation of the random variable X and σ is the standard deviation. If the distribution is completely symmetric, $\alpha_3 = 0$. And if the higher tail is longer, $\alpha_3 > 0$. $\alpha_3 < 0$ means that the lower tail is longer. Of course, skewness of the normal distribution is $\theta_{\mathbf{x}}$ Kurtosis, written as β_3 and defined by the following equation, is a measure of the sharpness.

$$\alpha_4 = E(X-\mu)^4/\sigma^4$$

$$\beta_4 = \alpha_4 - 3$$
(3)

 α_4 of the normal distribution is 3. Defining the kurtosis as $\alpha_4 - 3$ makes the kurtosis of the normal distribution zero. If β_4 is bigger than zero, the distribution has a sharper peak than the normal distribution. A distribution which has negative kurtosis has more rounded peak.

Fig. 7 is the histogram of the residual components. The solid line is the fitted curve of the normal distribution. As you can see, the shape is approximately the normal distribution. Skewness is -0.0406 and kurtosis is -0.0965. Both is very close to zero.



Fig. 7. Histogram of the residual components of all chips.

B. Spatial Correlation

Skewness and kurtosis are not enough to say that the residual component is random in a spatial region. It is important that there is no spatial correlation. To confirm the spatial correlation, we calculated the correlation coefficient like Fig. 8. Shifting the measurement results of a chip, we calculated the correlation coefficient of the shared area between the shifted and fixed. We can get the spatial correlation by changing the shift amount with respect to the horizontal and vertical axises.

Fig. 9 is the results. For comparison, we calculate including the 3rd. component (WID systematic distributions from all chips) too. Typical performance has nothing to do with the correlation 2nd. component (systematic component across the wafer) is just only D2D variations in this paper, and D2D variations increase the correlation even if there is no spatial correlation on each chip. There is very little correlation when calculated just only the residual component_A

Because the shape of the distribution is very near to the normal distribution and the correlation is very little, we can model the residue using the normal distributed pseudorandom numbers.



Fig. 9. Calculated spatial correlation of the extracted random component (LEFT), and calculated including the 3rd. component of equation (1).



Fig. 8. Calculating the spatial correlation. Shifting the residual components of measurement results, we calculate the correlation coefficient of the shared area between the shifted and fixed.

V. CONCLUSION

Variations model is proposed from the measurement results of LUT array and we defined the residue of three component as the random component. It is confirmed that the random component extracted by the proposed variations model is actually random from the viewpoint of skewness, kurtosis and correlation.

References

- James Chen, Michael Orshansky, Chenming Hu, and C-P. Wan. Statistical Circuit Characterization for Deep-Submicron CMOS Designs. In *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pages 90–91, 1998.
- [2] Ying Liu, Sani R. Nassif, Lawrence T. Pileggi, and Andrzej J. Strojwas. Impact of Interconnect Variations on the Clock Skew of a Gigahertz Microprocessor. In 37th Design Automation Conference Proceedings 2000, pages 168–171, 2000.
- [3] Kazuya Katsuki, Manabu Kotani, Kazutoshi Kobayashi, and Hidetoshi Onodera. A Yield and Speed Enhancement Scheme under Within-die Variations on 90nm LUT Array. In *Proceedings of IEEE* 2005 Custom Integrated Circuits Conference, pages 601–604, 2005.