A YIELD AND SPEED ENHANCEMENT TECHNIQUE USING RECONFIGURABLE DEVICES AGAINST WITHIN-DIE VARIATIONS ON THE NANOMETER REGIME

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ABSTRACT

A reconfiguralbe device can be utilized to enhance speed and yield on the sub-100nm device technologies, in which large within-die (WID) variations will degrade speed and cause huge yield loss in conventional fixed-structured ASICs. In the proposed scheme, configurations of all fabricated chips are optmized according to measured intra variations of LUTs and switch matrixes. Two LSIs are fabricated in a 90nm CMOS process. We successfully measured WID variations on the first LUT array LSI. The speed is enhanced by 4.1% in average on the second variation-aware FPGA LSIs to optmize configurations by the measured WID variations.

1. INTRODUCTION

The feature size of transistors is minimized year by year according to the Moore's law. We are now facing to the sub-100nm regime, in which the quantum physics must be applied instead of the current classical physics. In the classical micro-meter fabrication processes, device characteristics are changing very smoothly on a wafer, which is called the "Die to die (D2D) variation." In the sub-100nm regime, device characteristics are different one by one within a chip, which is called the "within-die (WID) variation." If one of critical paths become slower than the expected speed, a fabricated chip does not meet the specification. Fig. 1 compares the yield between the D2D-dominant(a) and WID-dominant(b) situations. In the WID dominant one, large intra variations cause huge yield loss.

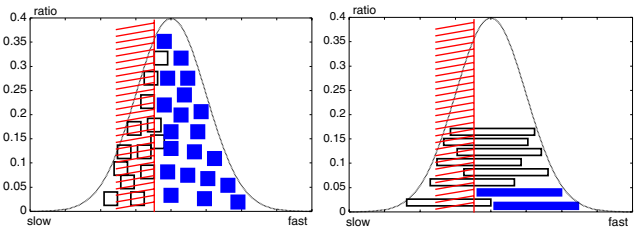
Conventional approaches against WID variations just mitigate them using process, device and circuit technologies. For example, the back-gate biasing[1] adjusts the bulk voltage chip by chip or functional-block by block to control threshold voltages of transistors. It is less effective against the high-frequency WID variations in the current sub-100nm devices reported in [2], since it is impossible to provide various voltage levels to such small areas with different characteristics.

Mitigating or suppressing device variations will be failed in the future sub-100nm process. Instead of those, we propose a variation-aware reconfigurable device to utilize within-die device variations as they are[3]. In the conventional approaches, WID variations are hateful enemies, while in the proposed one, they become good friends. Larger WID variations become, better we can optimize the circuit performance. First we measure all fabricated reconfigurable devices, and then these configurations are optimized to maximize performances. We have already fabricated two devices in a 90nm process. One is an LUT array to measure WID variations on regular structures. Another is an FPGA with functionalities to measure device variations using ring oscillators configured with LUTs and switch matrixes (SWMs).

In this paper, we explain the fundamental ideas to utilizing WID device variations with reconfigurable devices. Then measured variations on the sub-100nm process are reported and the speed and yield enhancement by reconfiguration using WID variations is shown.

2. FUNDAMENTAL IDEAS OF VARIATION-AWARE RECONFIGURATION

In the sub-100nm regime, WID variations are dominant instead of D2D variations. In such situations, fabricated LSIs cannot meet the specifications at the design time. We utilize reconfigurable devices to optimize an implemented circuit according to the measured WID variations. Fig. 2 shows the conventional fixed-structured ASICs and the proposed variation-aware reconfiguration. In the conventional approach,



(a) D2D dominant (b) WID dominant

Fig. 1. Speed distributions of fabricated chips. The bricks are the expected operating speed at the design phase. Filled rectangles are fabricated chips to meet specifications

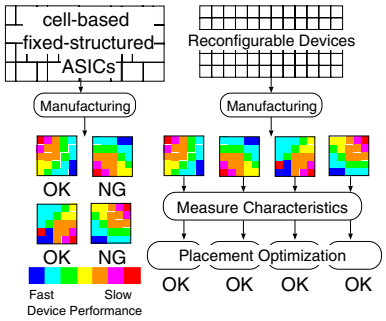


Fig. 2. Comparison between the conventional fixed-structured ASICs and the proposed variation-aware reconfiguration.

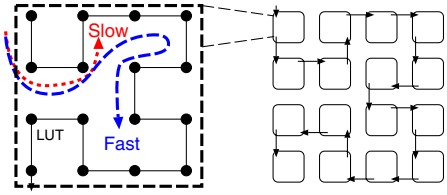


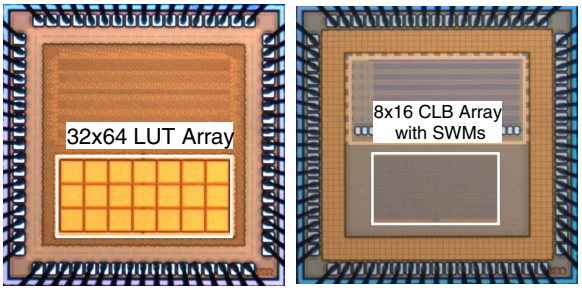
Fig. 3. Fractal structure for scalable measurement in the LUT array LSI. Dots are LUTs, which are connected with fixed wires in the fractal structure.

some amount of fabricated devices do not meet the specification due to the process variations. On the other hand, fabricated devices are reconfigured one by one according to measured variations, which enhances speed and yield.

3. AN LUT ARRAY TO MEASURE WID VARIATIONS

It is said that the regular structures on SRAMs or FPGAs are less affected by device variations than the irregular structures on ASICs or micro processors. But [4] reveals that the commercial LUT-based FPGA have some amount of WID variations. We have fabricated an LUT array including fixed-wired 32×64 LUTs to measure their speed variations[3]. Fig. 3 shows the structure of the LUT array. All LUTs are connected in a fractal structure, which enables scalable measurement in square regions ranged from 4×4 to 32×32. Fig. 4(a) shows a chip micrograph. The LUT array is located at the bottom of the 2.5×2.5mm die. Device variations are measured to count the number of LUTs within a period of time, through which a propagated signal is passing. If the LUTs are slow, the number of LUTs must be small.

In order to measure accurate device variations, the period of time for signal propagation is varied. The number of LUTs is changed according to the period (hereafter called as the clock cycle). Fig. 5 shows a graph with the number of LUTs on the y-axis and the clock cycles on the x-axis. The gradient of slower LUTs are moderate, while that of faster LUTs are steep. Fig. 6 shows WID variations from three fabricated chips in the resolution of 4×4 LUTs. Note that the unit on the Y axis is arbitrary (a.u.) because of the nondisclosure agreement for the device variations. They seems to be similar but WID variations differentiates them, which can be used to optimize placement and routing of each fabricated device utilizing them.



(a) LUT array (b) Variation-aware FPGA

Fig. 4. Chip micrographs of the LUT array to measure WID device variations (a) and the FPGA with WID-variation measurement capabilities (b).

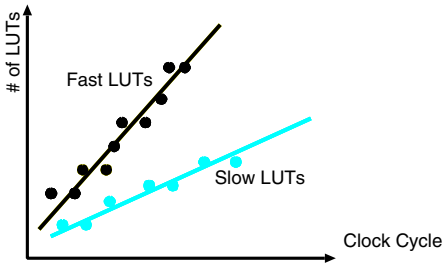


Fig. 5. The number of LUTs vs the clock cycles. The diagonal lines are linearly complemented by the least-square method.

4. AN FPGA DEVICE FOR VARIATION-AWARE PERFORMANCE OPTIMIZATION

The LUT array in the last section has no capability to implement a real functional circuit, since wires are fixed. We fabricate a fully-functional FPGA with capabilities to measure WID variations in the same 90nm process. Fig. 7 shows the detailed structure of the FPGA. Its architecture is almost same as the conventional LUT-based one. The embedded counter sums up the number of oscillations to measure WID variations. Fig. 4(b) shows a chip micrograph, in which 8×16 CLBs are laid out at the bottom of the 2.5×2.5mm die.

Device variations are measured to implement a ring oscillator using its reconfigurable capability. Fig. 8 shows the structure of the CLB. No additional circuit is required for the ring oscillator itself. But small additional circuit elements shaded in Fig.8 are added to count the number of oscillation and measure oscillated waveforms, which are used to implement a frequency divider in the CLB. These area penalty is about 1.0%.

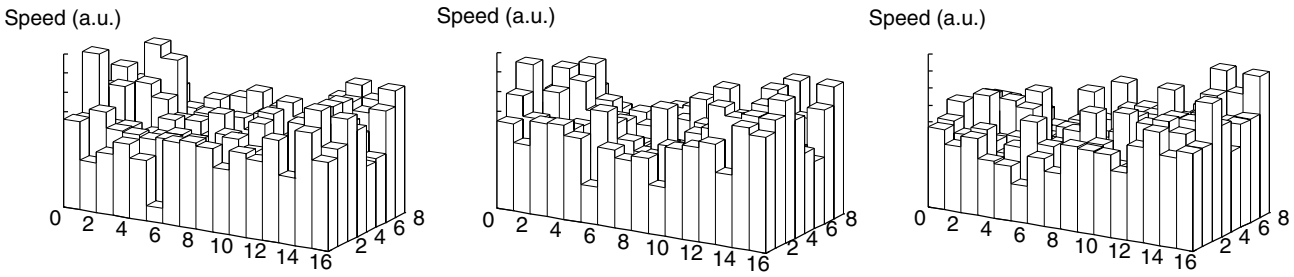


Fig. 6. WID variations from 3 chips on the fabricated LUT array in the resolution of 4×4 LUTs.

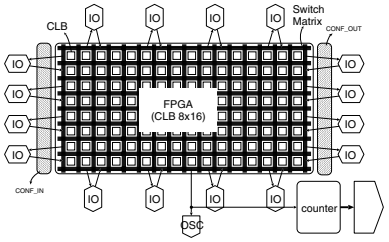


Fig. 7. Structure of the FPGA with WID-measurement capability. The counter modules counts the number of pulses from ring oscillators within a certain time.

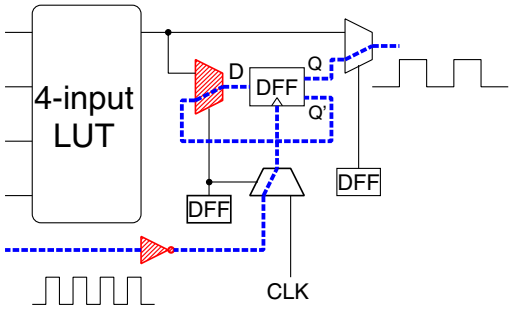


Fig. 8. Structure of a CLB. Shaded elements are used to configure a frequency divider.

5. VARIATION-AWARE RECONFIGURATION USING MEASURED WID VARIATIONS

We implemented a test circuit on the fabricated FPGAs to evaluate the speed and yield enhancement by the proposed variation-aware reconfiguration. Fig. 9 shows the test circuit that consists of 8 individual signal paths with two Flip Flops at the head and tail. Between these two FFs, CLBs are configured as buffers. Two clock pulses are given to the FFs. The number of CLBs between the FFs are ranged from 11 to 13. These 8 paths are rearranged using the measured WID variations. The first pulse starts the signal propagation from the head FF and the second one captures it at the tail FF. If the CLBs on the critical path are slower, the tail FF cannot capture the propagated signal.

Fig. 10 (a) shows results of the variation-aware reconfiguration from the fabricated 31 chips. The X axis is the speed

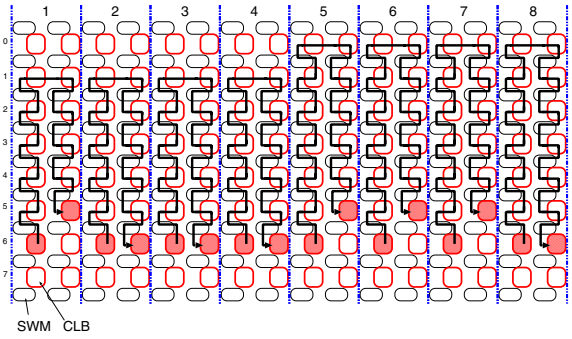


Fig. 9. A test circuit including 8 different-length individual signal paths with two Flip Flops at the shaded head and tail CLBs. Thick lines are signal propagation paths through CLBs and SWMs.

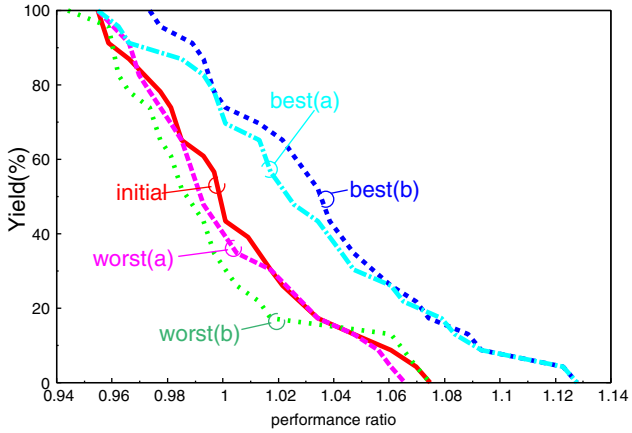


Fig. 11. Yield curves for the method (a), (b) and the initial.

of the worst case, while the Y axis is that of the best case. If a cross hair is placed above the diagonal line (slope=1), the performance of the chip is enhanced. Device speed is enhanced by 3.0% in average which is almost same as the measured WID variations. Device speeds are decreased in some chips, which is due to the difference of the signal paths between the measured ring oscillators and the implemented circuit. Fig. 10 (b) shows results of the other variation-aware reconfiguration. In (a), configurations are optimized using the measured frequencies of ring oscillators implemented in a single CLB. On the other hand, in (b) they are optimized using the measured frequencies of ring oscillators

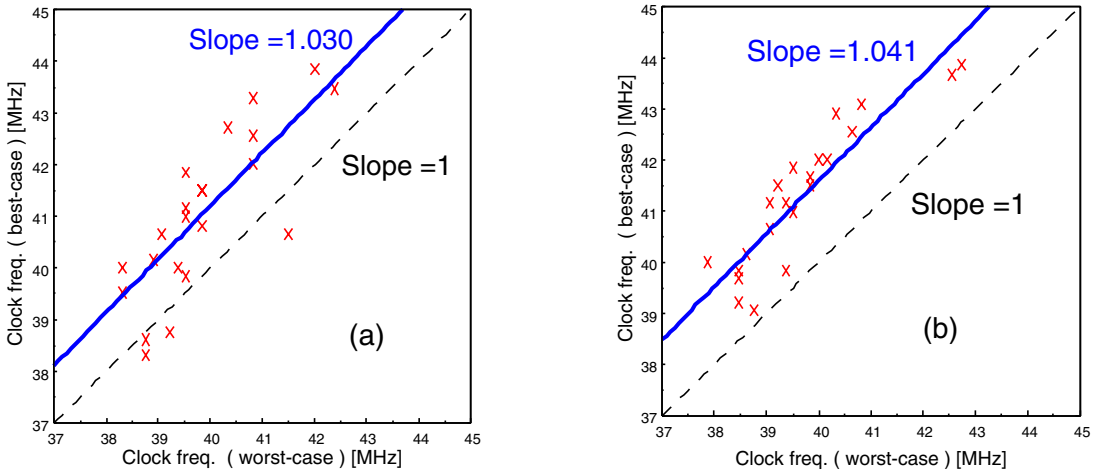


Fig. 10. (a)Variation-aware reconfiguration using WID variations on every CLB. (b) Variation-aware reconfiguration using total WID variations on CLBs in two columns.

implemented in 16 CLBs in the two columns. All the results are above the diagonal line in (b) and the performance is enhanced by 4.1% in average. Fig. 11 shows the yield and speed enhancement for the measured 31 chips. The X axis shows the chip speed (performance ratio) and the Y axis shows the cumulative ratio of working chips from right to left. The best(a) and worst(a) show the yield curve from the best and worst cases from the optimization method (a). The curve named "initial" shows that a fixed (initial) placement is applied to all fabricated chips. The yields at the performance ratio = 1 become 71%, 76% and 88% respectively from the worst, initial and best placement in (a). While they are 62%, 76% and 94% in (b). It can be said that the yield is better from the optimization using the WID variations on the actual signal paths (method(b)). But the optimization using the WID variations of every ring oscillator (method(a)) increase yield a certain amount. It is time-consuming to measure WID variations on the actual paths for each configuration. But the speed of ring oscillators can be measured automatically by an embedded BIST (Built-in Self-test) circuit, which must be integrated in our future devices.

The speed enhancement is just a few percent, which is mainly because the WID variations on the 90nm process is not so large. The speed enhancement must be accelerated according to the increase of WID variations in the future sub-100nm process.

6. CONCLUSION

This paper explains the fundamental idea of the variation-aware reconfigurable architecture, which utilize WID device variations as they are to enhance yield and speed of reconfigurable devices. We have fabricated two LSIs, one is an LUT array for the measurement of WID variations, another is an variation-aware FPGA for variation-aware optimization using measured WID variations.

In the LUT array, we have measured visible WID variations as the number of LUTs through which a signal is passing. The variation-aware placement optimizations on the variation-aware FPGA increase the speed by 3.0% and 4.1% in average. The 3.0% increase is obtained from the WID variations of ring oscillators implemented in a single LUT. The 4.1% increase is obtained from those of actual signal paths by multiple LUTs.

7. REFERENCES

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