A 90nm 8×16 LUT-based FPGA Enhancing Speed and Yield Utilizing Within-Die Variations

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***Abstract*— We have fabricated an LUT-based FPGA device with functionalities measuring within-die variations in a 90nm process. Measured variations are used to configure each device to maximize the operating frequency by allocating critical paths in faster portions. Variations are measured using ring oscillators implemented as a configuration of the FPGA. Placement optimization using a simple model circuit reveals that performance of the circuit is enhanced by 4% in average, which is the same amount as the measured within-die variations. The yield is enhanced by 32% to the worst case.**

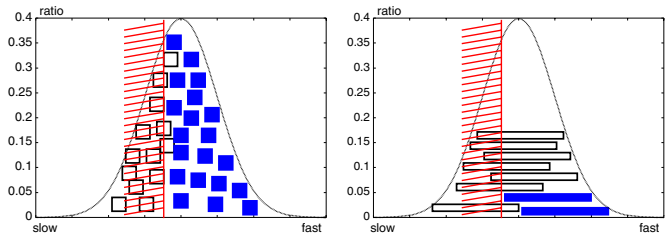
I. Introduction

The feature size of transistors is minimized year by year according to the Moore's law and the sub-100nm regime is now coming. While the steady improvement of fabrication technologies contributes to the remarkable growth of integration scale, variations of circuit performance caused by fluctuation of device characteristics has been increasing. In the micro-meter fabrication process, device characteristics are changing very smoothly on a wafer, which is called the "Die to die (D2D) variation". In the sub-100nm regime, in which the quantum physics must be applied. Device characteristics are different one by one within a chip according to some probabilistic distribution, which is called the "Within-die (WID) variation".

If one of critical paths becomes slower than the expected speed, a fabricated chip does not meet the specification. Fig. 1 compares the timing yield between the D2D-dominant(a) and WID-dominant(b) situations. As WID variations become dominant, they degrade all of fabricated LSIs and causes the drastic yield losses.

Mitigating or suppressing device variations will be failed in the future sub-100nm process. Instead of those, we propose variation-aware reconfiguration to utilize within-die device variations as they are [1]. On reconfigurable devices such as FPGAs, configurations are allocated after manufacturing. In conventional reconfigurable hardwares, each reconfigurable functional block is considered to have the same performance. In the proposed method we measure WID variations after manufacturing, and allocate the functional blocks suitably considering the measurement results. In the conventional approaches, WID variations are hateful enemies, while in the proposed one, they become friendly amigos. Larger WID variations become, better we can optimize the circuit performance.

Section II explains the principle of the proposed method to utilize WID variations with reconfigurable devices. We have designed and fabricated a FPGA in a 90nm process with a functionality to measure variations by the performance of a self-excited ring oscillators implemented. Section III explains it in detail. Section IV shows experimental results of yield and speed enhancement by the proposed method considering measurement results. Finally conclusion are written in section V.



(a) D2D dominant (b) WID dominant

Fig. 1. Speed distributions of fabricated chips. The bricks are the expected operating speed at the design phase. Filled rectangles are fabricated chips to meet specifications.

II. The Principle of Variation-aware Reconfiguration

In the sub-100nm regime, WID variations are dominant instead of D2D variations [2]. In such situations, fabricated LSIs cannot meet the specifications at the design time. We

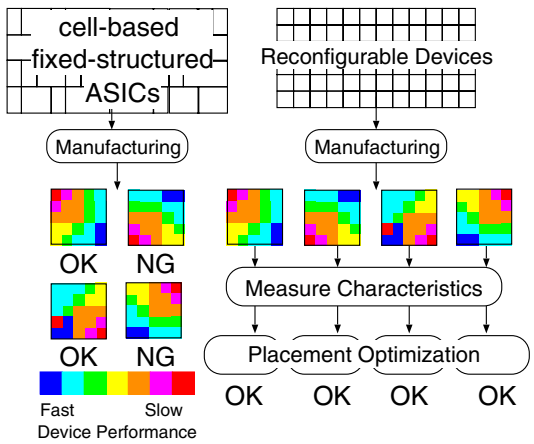


Fig. 2. Comparison between the conventional fixed-structured ASICs and the proposed variation-aware reconfiguration.

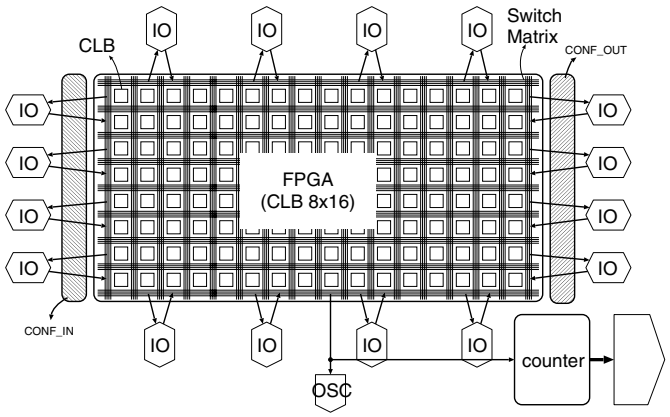


Fig. 3. Structure of the FPGA with WID-measurement capability. The counter modules counts the number of pulses from ring oscillators within a certain time.

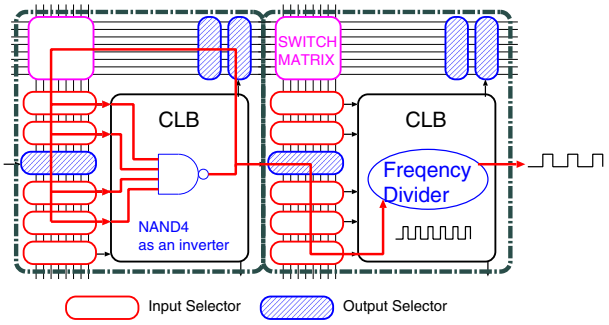


Fig. 4. The minimum ring oscillator using a single CLB, peripheral SWMs and wires. The adjacent CLB is worked as a frequency divider as in FIg.5.

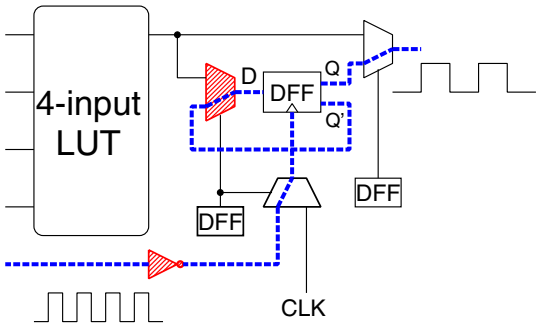


Fig. 5. Structure of a CLB. Shaded elements are used to configure a frequency divider.

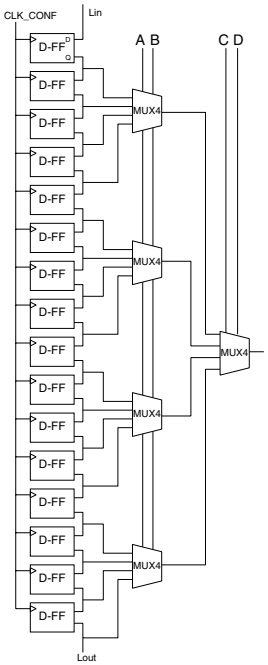


Fig. 6. Structure of an LUT. Configurations are stored in D-FFs instead of SRAMs.

utilize reconfigurable devices to optimize an implemented circuit according to the measured WID variations. Fig. 2 shows the conventional fixed-structured ASICs and the proposed variation-aware reconfiguration. In the conventional approach, some amount of fabricated devices do not meet the specification due to the process variations. On the other hand, fabricated devices are reconfigured one by one according to measured variations, which enhances speed and yield.

III. An FPGA Device for Variation-aware Performance Optimization

We fabricate a fully-functional FPGA with capabilities to measure WID variations in a 90nm process. Fig. 3 shows the structure of the FPGA. The embedded counter sums up the number of oscillations to measure WID variations. Fig.7 shows a chip micrograph, in which 8×16 CLBs (configurable logic blocks) are laid out at the bottom of the 2.5mm$\times$2.5mm die.

Device variations are measured to implement a ring oscillator using its reconfigurable capability. Fig. 4 shows the minimum ring oscillator implemented in a single CLB and peripheral SWMs and wires. The adjacent CLB is configured as a frequency divider. Frequency dividers are connected in series to reduce the frequency of oscillation. Fig.5 shows the structure of the CLB. No additional circuit is required for the ring oscillator itself. But small additional circuit elements shaded in Fig. 5 are added to implement the frequency divider in the CLB. These area penalty is about 1.0%. Fig.6 shows a schematic diagram of an LUT, which consists of 16 DFFs and five 4-multiplexers. DFFs store configuration data which are connected in series to construct a shift register. In commercial FPGAs, configuration data is stored in SRAMs. We designed the proposed FPGA in a conventional cell-based design flow. It is hard to integrate SRAMs in the flow. In addition to that, configuration data can be easily stored in the FPGA since it is sequentially given clock by clock along the shift register.

We can configure any size of ring oscillators. Fig. 4 is the minimum oscillator. The maximum one is configured using all CLBs in a chip. The embedded counter counts the number of oscillation within a certain period. Actually the number is fluctuated at every measurement. But the fluctuation is just 2% in the minimum ring and 0.5% in the maximum ring.

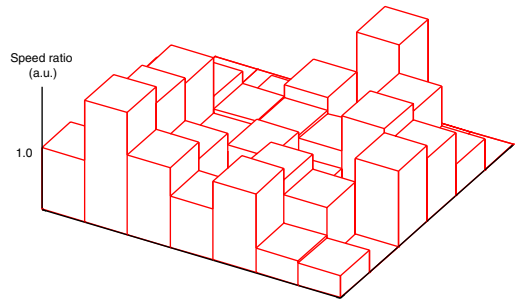


Fig. 8. Die-to-die variations extracted from the minimum-size ring oscillators as in Fig. 4(VDD=1V). (The X-Y plane shows locations of dies in a wafer.)

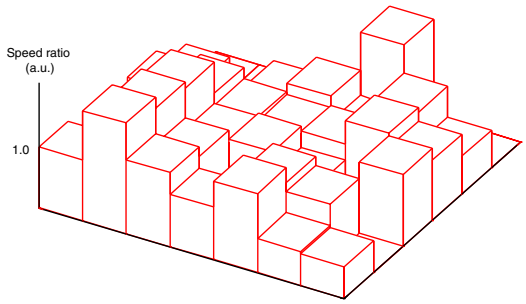


Fig. 9. Die-to-die variations extracted from the maximum ring oscillator(VDD=1V).

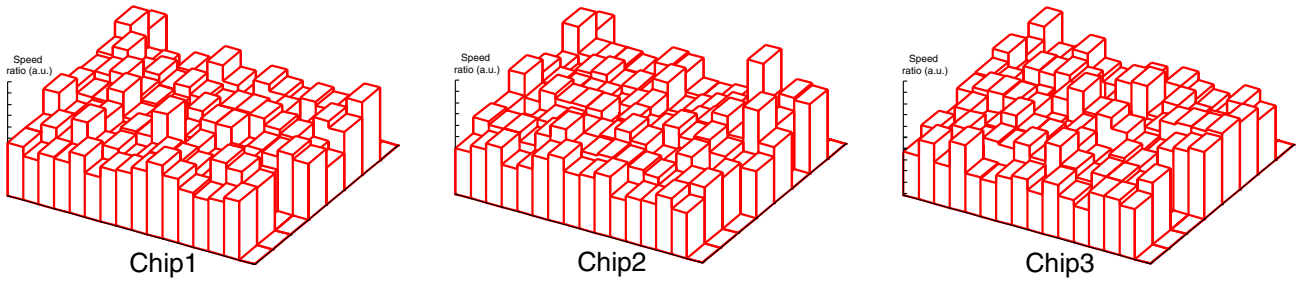
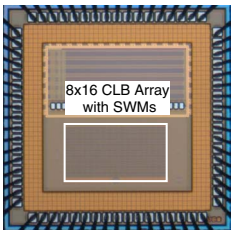


Fig. 10. Within-die variations of 3 fabricated chips.



Process	90nm 6Layer-Metal CMOS
# of Trs.	.5M
Area	2.5mm×2.5mm(Die), 0.6mm^2(FPGA core)
# of IOs	16 (for FPGA)

Fig. 7. Chip micrographs and specifications of the variation-aware FPGA.

Fig. 8 and Fig. 9 shows die-to-die variations extracted from the minimum and the maximum oscillators respectively. Note that the value along the Z axis is written in arbitrary unit due to the NDA issue. The former is obtained to average all measured frequencies from 8×16 oscillators in a chip. These two figures are almost same. The correlation factor is 0.999. Fig. 10 show within-die variations of three chips. They looks similar. They have the same tendency that the peripheral CLBs are faster than the central CLBs. But the random within-die variations differenciate them, which can be used to enhance speed of fabricated chips.

We show the speed and yield enhancement utilizing these measured WID variations in the next section

IV. Variation-aware Reconfiguration Using Measured WID Variations

We implemented a test circuit on the fabricated FPGAs to evaluate the speed and yield enhancement by the proposed variation-aware reconfiguration. Fig. 11 shows the test circuit that consists of 8 individual signal paths with two Flip Flops at the head and tail. Between these two FFs, CLBs are configured as buffers. Two clock pulses are given to the FFs. The number of CLBs between the FFs are ranged from 11 to 13. These 8 paths are rearranged using the measured WID variations. The first pulse starts the signal propagation from the head FF and the second one captures it at the tail FF. If the CLBs on the critical path are slower, the tail FF cannot capture the propagated signal.

Fig. 12 (a) shows results of the variation-aware reconfiguration from the fabricated 31 chips on a single wafer. The X axis is the speed of the worst case, while the Y axis is that of the best case. The worst case is the placement that minimize the operation frequency. If a cross hair is placed above the diagonal line (slope=1), the performance of the chip is enhanced. Device speed is enhanced by 3.0% in average which is almost same as the measured WID variations. Device speeds are decreased in some chips, which is due to the difference of the signal paths between the measured ring oscillators and the implemented circuit. Fig. 12 (b) shows results of the other variation-aware reconfiguration scheme. In (a), configurations are optimized using the measured frequencies of minimum ring oscillators. On the other hand, in (b) they are optimized using the measured frequencies of ring oscillators implemented in 16 CLBs in the two columns which uses the same CLBs as the signal path in Fig. 11. All the results are above the diagonal line in (b) and the performance is enhanced by 4.1% in average. Fig. 13 shows the yield and speed enhancement for the measured 31 chips. The X axis shows the chip speed (performance ratio) and the Y axis shows the cumulative ratio of working chips from right to left. The best(a) and worst(a) show the yield curve from the best and worst cases from the optimization method (a). The curve

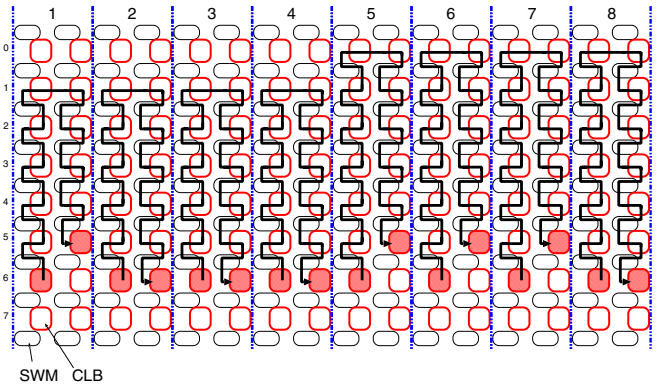


Fig. 11. A test circuit including 8 different-length individual signal paths with two Flip Flops at the shaded head and tail CLBs. Thick lines are signal propagation paths through CLBs and SWMs.

named "initial" shows that a fixed (initial) placement is applied to all fabricated chips. It is correspond to the conventional uniform configuration for all fabricated chips. The yields at the performance ratio = 1 become 71%, 76% and 88% respectively from the worst, initial and best placement in (a). While they are 62%, 76% and 94% in (b). The best placement has the 32% better yield than the worst placement. It can be said that the yield is better from the optimization using the WID variations on the actual signal paths (method(b)). But the optimization using the WID variations of every ring oscillator (method(a)) increase yield by a certain amount. It is time-consuming to measure WID variations on the actual paths for each configuration. But the speed of ring oscillators can be measured automatically by an embedded BIST (Built-in Self-test) circuit, which must be integrated in our future devices.

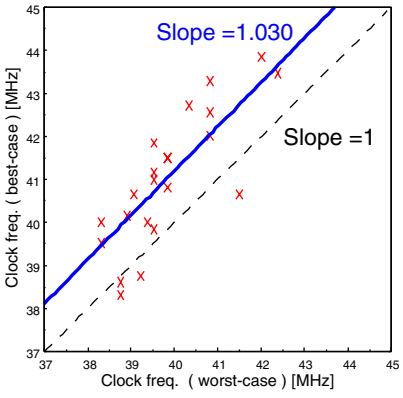
The speed enhancement is just a few percent, which is mainly because the WID variations on the 90nm process is not so large. The speed enhancement must be accelerated according to the increase of WID variations in the future nanometer process.

V. Conclusion

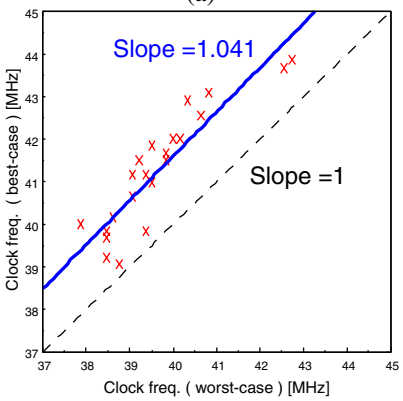
This paper explains the fundamental idea of the variation-aware reconfigurable architecture, which utilize WID device variations as they are to enhance yield and speed of reconfigurable devices. We have fabricated a variation-aware FPGA for variation-aware optimization using measured WID variations. Variations are measured to configure ring oscillators using its configurability. We have measured the fabricated 31 chips of the FPGA. Oscillation frequencies are changing so much within a chip. The variation-aware placement optimizations increase the speed by 3.0% and 4.1% in average. The 3.0% increase is obtained from the WID variations measured by the minimum ring oscillators. The 4.1% increase is obtained from speed variations of actual signal paths by multiple LUTs.

Acknowledgment

The VLSI chip in this study has been fabricated through the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo, with the collaboration by STARC, Fujitsu Limited, Matsushita Electric Industrial Company Limited., NEC Electronics Corporation, Renesas Technology Corporation, and Toshiba Corporatiion.



(a)



(b)

Fig. 12. (a)Variation-aware reconfiguration using WID variations on every CLB. (b) Variation-aware reconfiguration using total WID variations on CLBs in two columns.

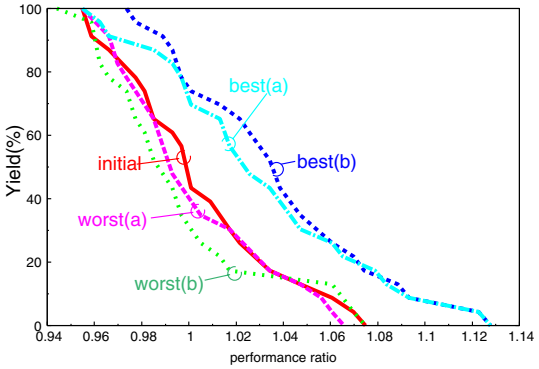


Fig. 13. Yield curves for the method (a), (b) and the initial.

References

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