A 90nm 8×16 FPGA Enhancing Speed and Yield Utilizing Within-Die Variations

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Abstract— We have fabricated an LUT-based FPGA device with functionalities measuring within-die variations in a 90nm process. Measured variations are used to configure each device to maximize the operating frequency by allocating critical paths in faster portions. Variations are measured using ring oscillators implemented as a configuration of the FPGA. Placement optimization using a simple model circuit reveals that performance of the circuit is enhanced by 4% in average, which is the same amount as the measured within-die variations. The yield is enhanced by 32% to the worst case.

I. Introduction

Variations of device performance are getting more serious as process scaling. Die-to-Die (D2D) variations degrades some amount of fabricated LSIs. On the other hand, within-die (WID) variations degrades almost all and causes the drastic yield losses. WID variations will be dominant in the near future. We propose variation-aware reconfiguretion to utilize WID variations as they are [2]. In the proposed method we measure WID variations after manufacturing, and allocate the functional blocks suitably considering the measurement results. Section II explains our proposed method. Section III explains the FPGA with functionalities measuring WID variations. Section IV shows experimental results. Finally, We conclude in section V.

II. The Principle of Variation-aware Reconfiguration

In the sub-100nm regime, WID variations are dominant instead of D2D variations [1]. In such situations, fabricated LSIs cannot meet the specifications at the design time. We utilize reconfigurable devices to optimize an implemented circuit according to the measured WID variations. Fig. 1 shows the conventional fixed-structured ASICs and the proposed variation-aware reconfiguration. In the conventional approach, some amount of fabricated devices do not meet the specification due to the process variations. On the other hand, fabricated devices are reconfigured one by one according to measured variations, which enhances speed and yield.

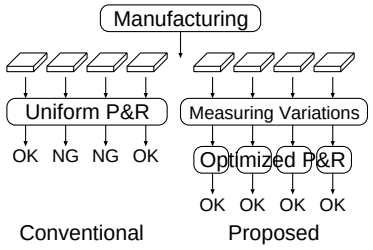


Fig. 1. Comparison between the conventional fixed-structured ASICs and the proposed variation-aware reconfiguration.

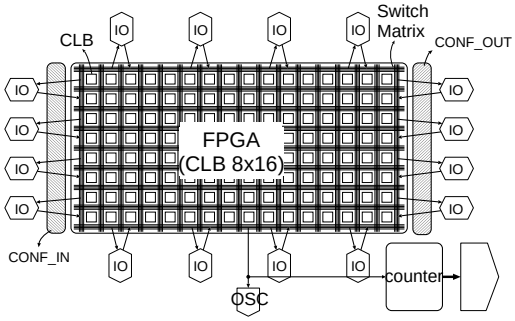


Fig. 2. Structure of the FPGA with WID-measurement capability. The counter modules counts the number of pulses from ring oscillators within a certain time.

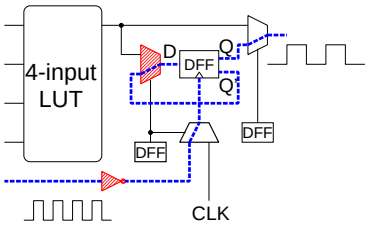
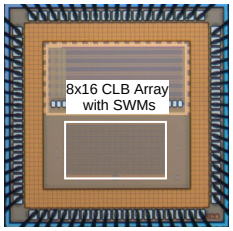


Fig. 3. Structure of a CLB. Shaded elements are used to configure a frequency divider.



Process	90nm 6Layer-Metal CMOS
# of Trs.	.5M
Area	2.5mm×2.5mm(Die), 0.6mm^2(FPGA core)
# of IOs	16 (for FPGA)

Fig. 4. Chip micrographs and specifications of the variation-aware FPGA.

III. An FPGA Device for Variation-Aware Performance Optimization

We fabricate a fully-functional FPGA with capabilities to measure WID variations in a 90nm process. Fig. 2 shows the structure of the FPGA. The embedded counter sums up the number of oscillations to measure WID variations.

Device variations are measured to implement a ring oscillator using its reconfigurable capability. Fig.3 shows the structure of the CLB. No additional circuit is required for the ring oscillator itself. But small additional circuit elements shaded in Fig. 3 are added to implement the frequency divider in the CLB. These area penalty is about 1.0%. We can configure any size of ring oscillators. The minimum oscillator is configured using one CLB and the maximum one is configured using all CLBs in a chip. Fig.4 shows a chip micrograph.

We show the speed and yield enhancement utilizing mea-

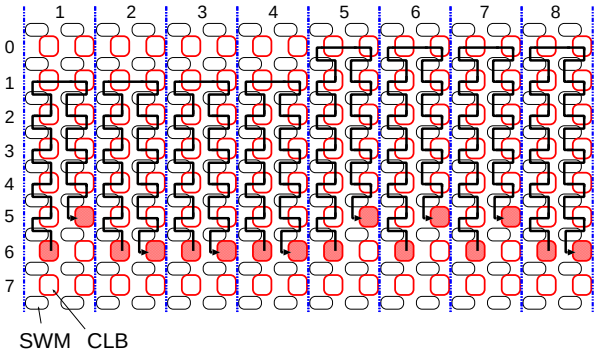
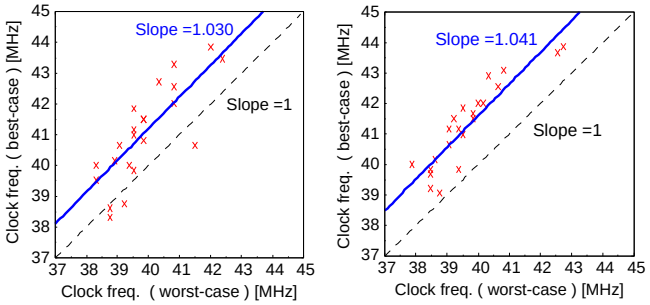


Fig. 5. A test circuit including 8 different-length individual signal paths with two Flip Flops at the shaded head and tail CLBs. Thick lines are signal propagation paths through CLBs and SWMs.



(a) (b)

Fig. 6. (a)Variation-aware reconfi guration using WID variations on every CLB. (b) Variation-aware reconfi guration using total WID variations on CLBs in two columns.

sured WID variations in the next section.

IV. Variation-aware Reconfiguration Using Measured WID Variations

We implemented a test circuit on the FPGAs to evaluate the speed and yield enhancement by the proposed method. Fig. 5 shows the test circuit that consists of 8 individual signal paths with two flip flops at the head and tail. Between these two FFs, CLBs are configured as buffers. Two clock pulses are given to the FFs. The number of CLBs between the FFs are ranged from 11 to 13. These paths are rearranged using the measured WID variations. The first pulse starts the signal propagation from the head FF and the second one captures it at the tail FF. If the CLBs on the critical path are slower, the tail FF cannot capture the propagated signal.

Fig. 6 (a) and (b) shows relationships of measured clock frequencies of the worst and best placement. The worst placement is the placement that minimize the operation frequency. If a cross hair is placed above the line with the slope 1, the performance of the chip is enhanced. In Fig. 6 (a), configurations are optimized using the measured frequencies of minimum ring oscillators. On the other hand, in (b) they are optimized using the measured frequencies of ring oscillators implemented in 16 CLBs in the two columns which uses the same CLBs as the signal path in Fig. 5. In (a), device speed is enhanced by 3.0% in average on the other hand 4.1% in (b) . Fig. 7 shows the yield and speed enhancement. The X axis shows the chip speed (performance ratio) and the Y axis shows the cumulative ratio of working chips from right to left. The best and worst show the yield curve from the best and worst cases from each optimization method (a) and (b). The curve named “initial” shows that a fixed (initial) placement is applied to all fabricated chips. It is correspond to the conventional uniform configuration for all fabricated chips. The yields at the performance ratio = 1 become 71%, 76% and 88% respectively from the worst, initial and best placement in (a). While they are 62%, 76% and 94% in (b). The best placement has the 32% better yield than the worst one. It can be said that the yield is better from the optimization using the WID variations on the actual signal paths (method(b)). But the optimization using the WID variations of every ring oscillator (method(a)) increase yield by a certain amount.

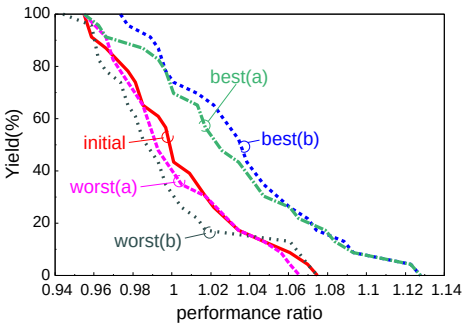


Fig. 7. Yield curves for the method (a), (b) and the initial.

V. Conclusions

In this paper we prppose a placement optimization scheme, which utilize WID variations to enhance speed and yield of reconfigurable devices. We have fabricated a variation-aware FPGA with a functionality to measure WID variations. We have measured the fabricated 31 chips of the FPGA. Oscillation frequencies are changing so much within a chip. The variation-aware placement optimizations increase the speed by 3.0% and 4.1% in average. The 3.0% increase is obtained from the WID variations measured by the minimum ring oscillators. The 4.1% increase is obtained from speed variations of actual signal paths by multiple LUTs.

Acknowledgements

The VLSI chip in this study has been fabricated through the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo, with the collaboration by STARC, Fujitsu Limited, Matsushita Electric Industrial Company Limited., NEC Electronics Corporation, Renesas Technology Corporation, and Toshiba Corporatiion.

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