# Impact of Random Telegraph Noise on CMOS Logic Delay Uncertainty

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Abstract—Statistical nature of RTN-induced delay fluctuation is described by measuring 2,520 ROs fabricated in a commercial 40 nm CMOS technology. Small number of samples have a large RTN-induced delay fluctuation. RTN-induced delay fluctuation becomes as much as 10.4% of nominal oscillation frequency under low supply voltage (0.65V). By slightly increasing the transistor size, more than 50% reduction of frequency uncertainty can be achieved under 0.75V operation. Circuit designers can change various parameters such as operating voltage, transistor size, logic stage number, logic gate type, and substrate bias. The impact of the parameters that can be changed by circuit designers is clarified in view of RTN-induced CMOS logic delay uncertainty.

#### I. INTRODUCTION

Designing reliable systems has become more difficult in recent years[1]-[3]. In addition to conventional problems such as transistor leakage, the degradation and variation of transistor performance have a severe impact on the dependability of VLSI systems. Random Telegraph Noise (RTN)[4] and Negative Bias Temperature Instability (NBTI)[5][6] are major reliability concerns for CMOS circuits. When transistors degrade owing to NBTI, the propagation delay of combinational logic increases. The correct operation of a register may not be guaranteed. Furthermore, the timing of registers that is generated by a clock tree may be skewed. As a result, owing to NBTI degradation, the circuit does not operate correctly or does not reach the lower limit of LSI performance. A remarkable phenomenon regarding NBTI is that the degraded performance of a pMOS transistor recovers when the bias temperature stress applied to the gate oxide is removed or relaxed[7]. RTN has attracted much attention as a temporal transistor performance fluctuation. RTN occurs in both pMOS and nMOS. RTN is an intrinsically random phenomenon. RTN already has a serious impact on CMOS image sensors[8], flash memories[9], and SRAMs[10]-[12]. Recently we have shown that RTN also induces performance fluctuation to logic circuits[13]. In this paper, we investigated the impact of RTN on CMOS logic delay uncertainty based on the measurement data. Circuit designers can change various parameters such as operating voltage, transistor size, logic stage number, logic gate type, and substrate bias. However, the impact of such parameters on RTN is not well understood at the circuit level[14]. The main contribution of this paper is clarifying this impact based on the measurement data.



Fig. 1. Typical synchronous circuit structure.

Power Supply  $(VDD_{RO}, VDD_{DFF})$  can be separately controlled. Substrate Bias (p-type, n-type) can be separately controlled.



Combinational circuit delay... Emulated by RO oscillation frequency Sequential circuit operation... Emulated by DFF toggled by the RO

Fig. 2. Simplest test structure that can emulate the synchronous circuit operation.

## II. TEST STRUCTURE FOR RTN EVALUATION

Figure 1 shows a typical synchronous circuit structure where a logic path exists between two registers. Figure 2 shows the simplest test structure that can emulate the synchronous circuit operation of Fig. 1. Combinational circuit delay is emulated by ring oscillator (RO) oscillation frequency. Sequential circuit operation is emulated by D flip-flop (DFF) toggled by the RO output. The power supply for RO (VDD<sub>RO</sub>) and DFF (VDD<sub>DFF</sub>) can be independently controlled. We can also control the substrate bias for pMOS and nMOS. Figure 3 shows the whole test structure for the RTN measurement. RTN-



Fig. 3. Whole test structure for RTN measurement. One test structure contains 840 ROs.



Fig. 4. Measurement result of RTN-induced RO frequency fluctuation. (a)  $\Delta F/F_{\rm max} = 10.4\%$  (b)  $\Delta F/F_{\rm max} = 0.6\%$ .

induced delay fluctuation is measured by the RO frequency fluctuation. Various type of ROs are contained in one circuit unit, which is called a section (Fig. 3). There are 840 same sections on 2 mm<sup>2</sup> area. Thus the statistical nature of RTN can be evaluated by the RO array. This chip is fabricated in a commercial 40 nm CMOS technology. All measurements are done at the room temperature.

## III. MEASUREMENT RESULTS OF LOGIC DELAY FLUCTUATION

Figure 4 (a) shows the measurement result of the oscillation frequency of a 7-stage RO for about 80 s at VDD<sub>RO</sub>=0.65V. The size of the inverter is smallest in this technology. The body bias for pMOS ( $V_{\rm bs-pMOS}$ ) and nMOS ( $V_{\rm bs-nMOS}$ ) are set to 0V. Measurement results show the large step-like frequency fluctuation. Here,  $F_{\rm max}$  is defined as the maximum



Fig. 5. Measurement results that shows 2-state fluctuation.







Fig. 7. Time constant distribution of Fig. 5

oscillation frequency and  $\Delta F$  is defined as the maximum frequency fluctuation as shown in Fig. 4 (a).  $\Delta F/F_{\text{max}}$  is a good measure for the impact of RTN-induced frequency fluctuation. It is 10.4 % for Fig. 4 (a). However, significant fluctuation is not observed for the case of Fig. 4 (b). Large fluctuation such as Fig. 4 (a) is a rare case that reflects the RTN nature. Figure 5 shows a typical measurement data at



Fig. 8. Estimation of discrete states by EM algorithm for a 2-state case.



Fig. 9. Estimation of discrete states by EM algorithm for a complex case.



Fig. 10. Histogram of measured  $\Delta F/F_{\text{max}}$ .

 $VDD_{BO}=0.65V$  where a large 2-state fluctuation is observed. Time constants  $\tau_{\rm c}$  and  $\tau_{\rm e}$  are defined as the time that the RO stays at high-frequency state and low-frequency state respectively. The power spectrum density (PSD) of Fig. 5 is obtained by quantizing the measurement data of Fig. 5 into the 2-state waveform. Lorentzian power spectrum is observed (Fig. 6). Figure 7 shows time constant ( $\tau_c$ ,  $\tau_e$ ) distributions of Fig. 5. It is found that both distributions for  $\tau_{\rm c}$  and  $\tau_{\rm e}$ follow exponential distribution  $(e^{-t/\tau})$ . Lorentzian PSD and  $e^{-t/\tau}$  distribution are observed for the case of a transistor where a single defect causes RTN fluctuation. This indicates that RTN fluctuation of Fig. 5 is caused by a single defect in a specific transistor in the 7-stage RO. Figure 8 and 9 show the automatic discrete state estimation by the EM (Expectation Maximization) algorithm[15]. Figure 8 shows 2state fluctuation. There are two peaks in the histogram. It is assumed to be composed of two normal distributions. Average values of two normal distributions are identified with discrete two states of RO oscillation by the EM algorithm. Figure 9 shows the complex fluctuation. The EM algorithm works well in such a complex case. It is possible to estimate discrete states of measurement data automatically by the EM method. Figure 10 shows the histogram of measured  $\Delta F/F_{\text{max}}$  for the whole test structure of Fig. 3 over three chips (2,520 ROs). It is found that the small number of samples have a large RTNinduced fluctuation and a long tail exists for larger  $\Delta F/F_{\text{max}}$ .

# IV. IMPACT OF RTN ON DELAY UNCERTAINTY

Figure 11 shows the cumulative distribution function (CDF) of  $\Delta F/F_{\rm max}$  for various VDD<sub>RO</sub>. The impact of RTN-induced delay fluctuation increases rapidly under low voltage operation. Figure 12 shows CDF of  $\Delta F/F_{\text{max}}$  for two transistor sizes. The ratio of nMOS gate area  $(W \times L)$  of the minimum size inverter (INV) to the standard size INV is 0.30. The ratio of pMOS gate area of minimum INV to the standard INV is 0.21. Increasing the gate area slightly is very effective to suppress the delay uncertainty. More than 50% reduction of  $\Delta F/F_{\rm max}$  can be achieved under 0.75V operation. Figure 13 shows the CDF of  $\Delta F/F_{\text{max}}$  for various logic stage numbers. As the stage number decreases, the impact of RTN becomes larger. Figure 14 shows the CDF of  $\Delta F/F_{\text{max}}$  for various logic types of 19-stage ROs. The impact of RTN is most pronounced for the inverter case. Figure 15 shows the the measurement results of frequency fluctuation of one RO for various substrate bias conditions. For this sample, the time constant is modulated considerably only when the pMOS substrate bias is changed from 0V to 0.2V. Figure 16 is the power spectrum density (PSD) for the same sample of Fig. 15. RTN-induced RO frequency fluctuation for 60 s is evaluated under various substrate bias conditions. We observe the effect of one trap at the PMOS inside the RO that induces large delay fluctuation at the circuit level. Figure 17 shows the frequency fluctuation of RO location (section No.) 1 for various substrate bias. Four-state fluctuation due to two traps is clearly observed for the normal substrate bias case. The effect of one of two traps disappears for the forward bias case. Figure 18 shows the frequency fluctuation of RO location 1 when pMOS or nMOS is forward biased. The effect of one of two traps disappears only when nMOS is forward biased. Thus the disappeared



Fig. 11. CDF of  $\Delta F/F_{\text{max}}$  for various VDD<sub>RO</sub>.



Fig. 12. CDF of  $\Delta F/F_{\text{max}}$  for two transistor sizes.



Fig. 13. CDF of  $\Delta F/F_{max}$  for various logic stage numbers.



Fig. 14. CDF of  $\Delta F/F_{\text{max}}$  for various logic types.

two-state fluctuation is caused by a single trap in a specific nMOS in the RO. Figure 19 shows the frequency fluctuation of RO location 219 for various substrate bias conditions. It represents the ROs that still have large fluctuation under the forward body-bias condition. Figure 20 shows ROs that have



Fig. 15. RTN-induced RO frequency fluctuation for various substrate bias conditions.



Fig. 16. Power spectrum of RTN-induced RO frequency fluctuation for various substrate bias conditions.

more than 4 % fluctuation at reverse bias case to evaluate the forward body-bias effect on large  $\Delta F/F_{\rm max}$  samples (28 ROs). When substrate bias is changed from the reverse bias case to the forward bias case,  $\Delta F/F_{\rm max}$  tends to decrease. However, for example,  $\Delta F/F_{\rm max}$  slightly increases in the case of the RO location "68", "160" and "219" when forward substrate bias is applied. The impact of RTN-induced delay fluctuation tends to



Fig. 17. RTN-induced RO frequency fluctuation for various substrate bias conditions (RO Location 1).



Fig. 18. RTN-induced RO frequency fluctuation for various substrate bias conditions (RO Location 1).

be reduced by forward body-biasing technique, but a few ROs do not follow this tendency. Figure 21 shows the histogram of measured  $\Delta F/F_{\rm max}$  for one test structure under various substrate bias. The impact of RTN-induced delay fluctuation tends to be reduced by forward body-biasing technique, but a few ROs still have a large fluctuation.

# V. CONCLUSIONS

Statistical nature of RTN-induced delay fluctuation is described by measuring 2,520 ROs fabricated in a commercial 40 nm CMOS technology. The small number of samples have a large RTN-induced delay fluctuation. RTN-induced delay fluctuation becomes as much as 10.4% of nominal oscillation frequency under low supply voltage (0.65V) operation. It is also indicated that a single defect in a specific transistor



Fig. 19. RTN-induced RO frequency fluctuation for various substrate bias conditions (RO Location 219).



Fig. 20.  $\Delta F/F_{\rm max}$  of different ROs for various substrate bias conditions. RO that have more than 4% fluctuation at reverse substrate bias case are shown.

in an RO causes clear 2-state oscillation fluctuation. The EM algorithm works well to identify discrete states for a complex fluctuation as well as a simple 2-state one. More than 50% reduction of frequency uncertainty ( $\Delta F/F_{max}$ ) can be achieved under 0.75V operation by slightly increasing the transistor size. The impact of the parameters that can be changed by circuit designers such as operating voltage, tran-



Fig. 21. Histogram of measured  $\Delta F/F_{max}$  for various substrate bias conditions.

sistor size, logic stage number, logic gate type, and substrate bias is clarified in view of RTN-induced CMOS logic delay uncertainty.

### **ACKNOWLEDGMENTS**

We are grateful to S. Fujimoto, K. Kitajima, I. Mahfuzul, T. Miki, S. Nishizawa for chip design. The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with STARC.

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