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Evaluation of plasma-induced damage and bias temperature instability depending on type of antenna layer using current-starved ring oscillators

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Plasma-induced damage (PID) and bias temperature instability (BTI) are inevitable reliability issues that degrade the performance of transistors. In this study, PID and BTI, depending on the type of antenna layer, are evaluated in current-starved ring oscillators (ROs) to separate degradations in PMOS and NMOS transistors in a 65 nm silicon-on-insulator (SOI) process. Oscillation frequencies of ROs fluctuate with the performance of MOSFET switches between power/ground rails and virtual power/ground nodes. The initial frequencies of ROs with PMOS switches having antennas on upper layers decrease. However, those with NMOS switches become higher than those without PID because high-k dielectrics are damaged by positive charges. The degradation induced by negative BTI (NBTI) in PMOS is 1.5 times larger than that induced by positive BTI (PBTI) in NMOS. However, both NBTI- and PBTI-induced degradations are the same among different antenna layers. The frequency fluctuation caused by PID is converted to threshold voltage shifts by circuit simulations. Threshold voltages shift by 8.4 and 11% owing to PID in PMOS and NMOS transistors, respectively.

1. Introduction

Plasma-induced damage (PID) is caused by charge during metallization.[1–6] Charge is induced in metal wires during back-end-of-line (BEOL) interlayer dielectric processes. Charged metal wires are called antennas. When an antenna wire is connected to a gate terminal, charge in the antenna flows through gate dielectrics. PID shifts threshold voltage (V_{th}) because defects are generated in the gate dielectrics.[7] If the number of defects in the gate dielectrics increases, bias temperature instability (BTI)-induced degradation accelerates.[8] BTI is one of the causes of aging degradation and V_{th} increases with time.[9–16] BTI-induced degradation accelerates as voltage and temperature increase. Such degradation is induced when defects trap carriers. This degradation can be explained by the atomistic trap-based BTI (ATB) model.[17–23] There are dangling bonds in the gate oxide and at the interface between the gate oxide and the silicon substrate. When these defects trap carriers, the electric field in the gate oxide decreases and V_{th} increases. Each defect has an individual time constant for trapping carriers. V_{th} increases with time in proportion to a logarithm according to the ATB model because time constants are uniformly distributed on the log scale from 10^{-9} to 10^{9} s.[17] BTI-induced degradation is recovered when the gate–source voltage (V_{gs}) is removed because the carriers trapped in the gate oxide are emitted to the channel. Defects with small time constants affect the initial frequency and those with large time constants affect aging degradations such as that induced by BTI.

There are negative BTI (NBTI) and positive BTI (PBTI). NBTI occurs in PMOS when V_{gs} is negative. PBTI occurs in NMOS when V_{gs} is positive. PBTI is especially observed in technologies with high-k (HK) gate dielectrics.[24] When defects in the gate oxide trap carriers, the electric field in the gate oxide decreases and V_{th} increases. BTI-induced degradation accelerates when these defects are generated by PID. PID and BTI are serious reliability issues that shorten the lifetime of very large scale integration (VLSI) circuits.

In previous studies, differences between SiO_2 and HK gate dielectrics[25] in terms of antenna shape (e.g., square and comb)[26] and thickness[27] were evaluated. BTI caused by PID was also evaluated in the study of Choi et al.[28] Our research focused on PID depending on the type of antenna layer, particularly the second to fifth metal layers (M2–M5) in SSDM 2017.[29] These metal layers are used for local routing and have the same thickness. In this study, we evaluate both PID and BTI depending on the type of antenna layers. We evaluate how PID and BTI occur with the change of metal layers.

The degradations caused by PID or BTI are generally measured at the transistor level to evaluate those degradations in NMOS or PMOS independently. However, it is difficult to measure many transistors simultaneously in a short time. On the other hand, many transistors on a chip can be evaluated using ring oscillators (ROs). It is also possible to measure oscillation frequencies on ROs with counters by counting the number of oscillations. However, it cannot separate degradations on PMOS or NMOS. Moreover, it is difficult to convert frequency fluctuation to V_{th} because all MOSFETs on the ROs suffer from degradations. Current-starved ROs are fabricated to address these issues. Oscillation frequencies are measured to evaluate PID and BTI on PMOS and NMOS separately. Frequency fluctuations are converted to V_{th} using circuit simulations. In Sect. 2, we explain the circuits for evaluating PID and BTI depending on the type of antenna layers. In Sect. 3, we show the measurement results. In Sect. 4, frequency fluctuations are converted to V_{th}. Finally, Sect. 5 shows our conclusions.

2. Measurement circuits

Figure 1 shows a cross section of the circuit proposed to measure degradations depending on the type of antenna layers. The leftmost transistor is called the reference switch (REF-SW). The gate metal area of REF-SW is as small as possible to prevent PID. The antenna ratio (AR) calculated from the antenna metal area divided by the gate area is less than 20 on REF-SW. PID in REF-SW can be ignored because the other switches have metal wires with an AR of 2,000. The rightmost transistor called M5-PID-SW has a long fifth metal layer (M5) as the antenna and the other metal layers from first to fourth (M1–M4) are minimized. This M5-PID-SW is mainly damaged by PID from M5. M2- to M4-PID-SWs have similar structures. Each PID-SW has a different antenna layer from the second metal layer (M2) to the fifth metal

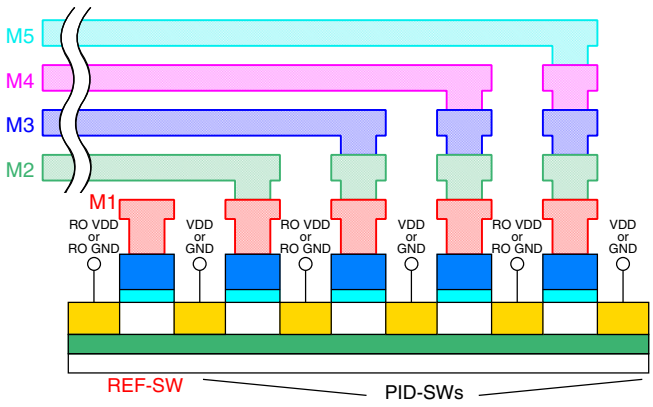


Fig. 1. (Color online) Cross section of measurement circuit for evaluating degradations depending on the type of antenna layer. Each PID-SW has a large metal area for an antenna and the other metal layers are minimized.

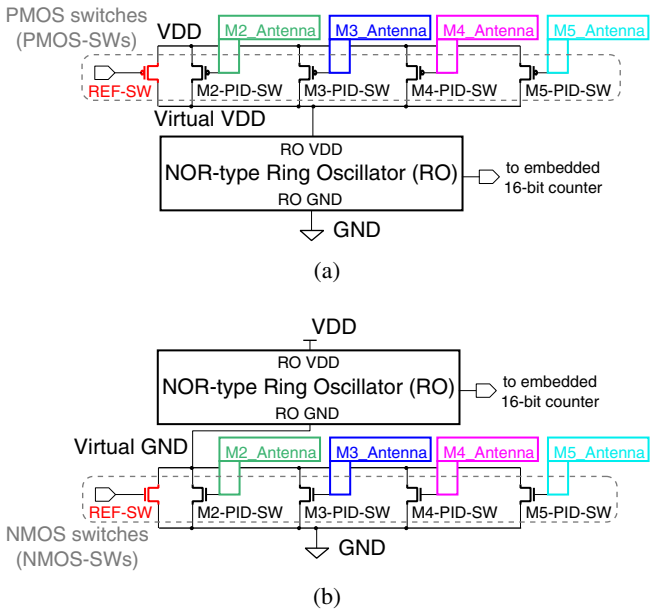


Fig. 2. (Color online) Measurement circuit for evaluating PID and BTI with current-starved switches. A current-starved switch (REF-SW) is inserted as reference and those with antennas (PID-SWs) are also inserted to evaluate PID and BTI depending on the type of antenna layers. (a) PMOS type: PMOS-SWs are inserted between VDD and RO VDD (virtual VDD). (b) NMOS type: NMOS-SWs are inserted between GND and RO GND (virtual GND).

layer (M5). These layers have the same metal thickness and width.

We fabricated a chip including 11-stage ROs in a 65 nm fully depleted silicon-on-insulator (FDSOI) process. In our previous measurement circuits, antennas are directly connected to wires inside ROs.[1,28] This measurement circuit cannot separate PID effects between PMOS and NMOS. Moreover, it is difficult to convert frequency fluctuation to V_{th} because each MOSFET suffers from degradations independently. Figure 2 shows the measurement circuit proposed to address these issues. The PMOS switches (PMOS-SWs) shown in Fig. 1 are inserted between VDD and RO VDD (virtual VDD) as shown in Fig. 2(a). A PMOS-SW without an antenna (REF-SW) is inserted as reference. PMOS-SWs with antennas (PID-SWs) on different layers are also inserted. Each PID-SW is damaged by PID from the antenna on each

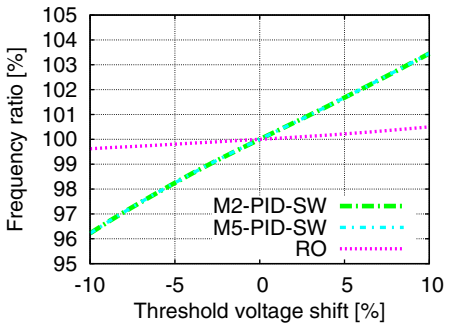


Fig. 3. (Color online) Simulation results of V_{th} sensitivity. PID-SWs have same the sensitivity to V_{th} shift and a tenfold or more sensitivity to V_{th} fluctuation than the MOSFET in RO.

metal layer. When a PID-SW is on, the virtual VDD voltage fluctuates owing to the V_{th} of the PID-SW. The frequency of ROs changes with the voltage of virtual VDD (RO VDD). The V_{th} fluctuation caused by PID is measured by the frequency fluctuation of ROs. Oscillation frequencies are only slightly affected by variations in capacitance with antenna area or the type of antenna layer, but markedly affected by the V_{th} in PID-SWs. Moreover, PMOS-SWs are ten times or more sensitive to V_{th} fluctuation than MOSFETs in ROs. If the V_{th} of a transistor in a n-stage RO changes, the frequency fluctuation is alleviated to $1/n$. However, current-starved-SWs suppress current from VDD to ROs and increase the delay time of all inverters in the ROs. Figure 3 shows simulation results of oscillation obtained by changing the V_{th} of PID-SWs or a MOSFET in ROs. The X- and Y-axis show V_{th} shift (ΔV_{th}) and the frequency ratio based on the frequency without degradation, respectively. Oscillation frequencies proportionally change with V_{th} shift. The simulation results are the same for M2- and M5-PID-SWs. The results of M3- and M4-PID-SWs are also the same. There is no difference in V_{th} sensitivity among PID-SWs. The oscillation frequency of ROs changes when the V_{th} of the transistor in ROs shifts as shown by the pink dotted line in Fig. 3. However, it is one-tenth or less sensitive than those of PID-SWs. Thus, only PID effects can be measured in our measurement circuits. PID depending on the type of antenna layers is evaluated by comparing the frequencies of ROs with REF- and PID-SWs. ROs with PMOS current-starving switches are for PID in PMOS since PID occurs only in PMOS-SWs. NMOS switches (NMOS-SWs) are inserted between GND and RO GND (virtual GND) to evaluate PID on NMOS as shown in Fig. 2(b). If NMOS PID-SW is damaged by PID, the voltage of RO GND (virtual GND) increases and oscillation frequency decreases. It is possible to separate PID effects in NMOS and PMOS using ROs with the PMOS and NMOS current-starved switches.

Each 11-stage RO is composed of NOR gates and an inverter for outputs as shown in Fig. 4. An RO composed of general inverters suffers from both NBTI and PBTI when it stops oscillating. Transistors in the RO should not be affected by BTI in order to evaluate PID on the current-starved MOSFETs. Thus, the NOR RO is used as shown in Fig. 5. Gate terminals of $NMOS_{ENB}$ and $PMOS_{ENB}$ are connected to ENB to control oscillation. Those of $NMOS_{RO}$ and $PMOS_{RO}$ are connected to outputs of previous stages. When ENB is low, the NOR RO oscillates. When ENB is high, the NOR

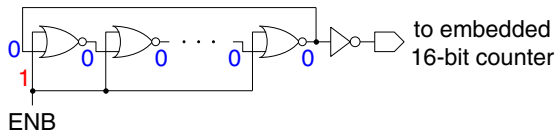


Fig. 4. (Color online) Schematic of NOR-type RO. When ENB is high or low, the RO stops oscillating or oscillates, respectively. All outputs are low when the RO stops.

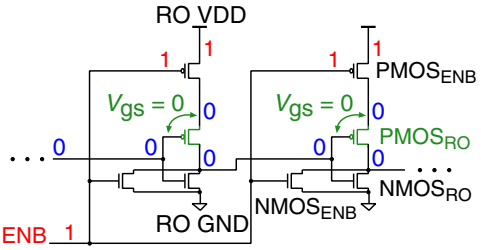


Fig. 5. (Color online) NOR-type RO in transistor level. NBTI does not occur when the RO stops oscillating because the V_{gs} of PMOS$_{RO}$ is 0.

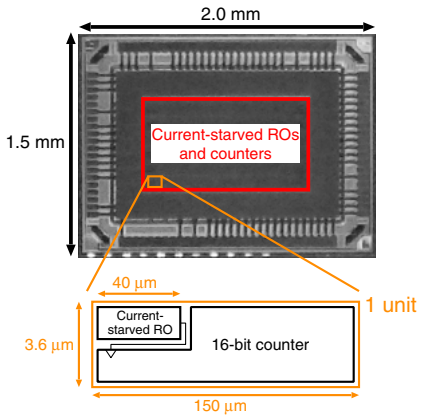


Fig. 6. (Color online) Chip micrograph fabricated in a 65 nm FDSOI process.

RO stops oscillating and all outputs of NOR gates become low. NBTI does not occur because the V_{gs} of PMOS$_{RO}$ is 0. Even if NMOS$_{ENB}$ suffers from PBTI, the oscillation frequency does not change because BTI on logic gates for controlling ENB does not affect the high or low voltage of ENB. NMOS$_{RO}$ does not suffer from PBTI since V_{gs} is 0. On the other hand, current-starved-SWs suffer from BTI while they are on state because the V_{gs} of the current-starved-SWs are always negative. Thus, BTI occurs only on PID-SWs.

Figure 6 shows the test chip fabricated in a 65 nm FDSOI process. The chip size is $2 \times 1.5\,\text{mm}^2$. It has 70 ROs in both PMOS- and NMOS-type current-starved ROs. The antenna ratios calculated from the antenna metal area divided by the gate area are 2,000 in all ROs.

3. Measurement results

3.1 Initial frequency degradation due to PID

To evaluate PID, initial frequencies are measured. First, all transistors except REF-SW are off in an RO. This state means that only REF-SW is on. Then, the RO starts to oscillate for 28 μs. Oscillation frequencies are measured in 70 ROs × 4 chips and the average frequency of those ROs is determined. This average frequency is used as reference. To evaluate the

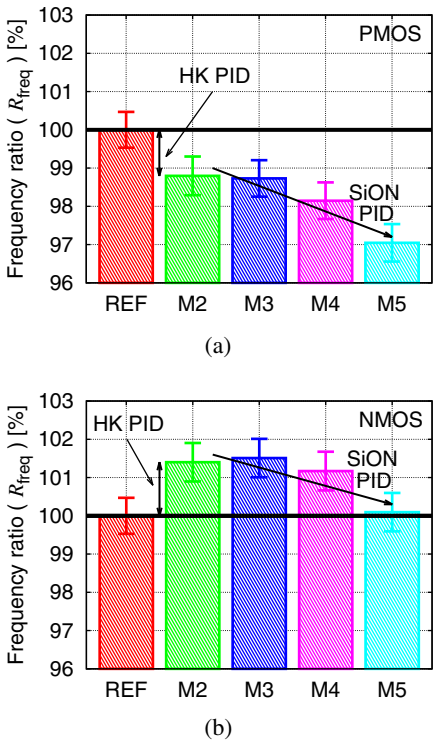


Fig. 7. (Color online) Measured initial frequencies. (a) PMOS type. (b) NMOS type.

PID of M2, all transistors except M2-PID-SW are off in the RO. Only M2-PID-SW is on. Then, the RO oscillates for 28 μs. The measured frequencies in the 70 ROs × 4 chips are averaged. The average frequency fluctuates owing to PID on M2-PID-SW. Frequencies from M3- to M5-PID-SWs are measured similarly. We also measured frequencies in the decreased order from M5. However, the results in the increased order are used because those results in the decreased order are the same as those in the increased order.

The measurements are performed at room temperature and a nominal supply voltage of 1.0 V. Frequency ratio (R_{freq}) is calculated as

$$R_{freq} = \frac{f_{PID}}{f_{REF}}, \tag{1}$$

where f_{REF} and f_{PID} are the frequencies of REF- and PID-SWs, respectively. R_{freq} indicates the amount of degradation in terms of oscillation frequency.

Figure 7 shows the measurement results. R_{freq} in 70 ROs × 4 chips showed a normal (Gaussian) distribution in all antenna layer structures. Error bars are plotted in accordance with the standard error (SE) calculated as

$$SE = \frac{3\sigma}{n}, \tag{2}$$

where σ is the standard deviation in the normal distribution and n is the number of ROs. Initial frequencies of PMOS-SWs with antennas are lower than those of REF-SW as shown in Fig. 7(a). The ROs with M5-PID-SW have the lowest R_{freq}. $|V_{th}|$ increases owing to PID in PMOS with antennas in the upper metal layers. The initial frequency of M5-PID-SW decreases by 3.1% from that of REF-SW. However, the initial frequencies of NMOS-SWs are higher

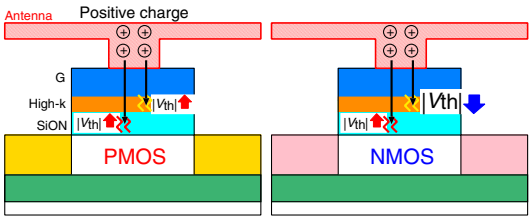


Fig. 8. (Color online) V_{th} fluctuation due to positive charge. $|V_{th}|$ increases in PMOS owing to PID. $|V_{th}|$ decreases owing to positive charge damage in HK in NMOS.

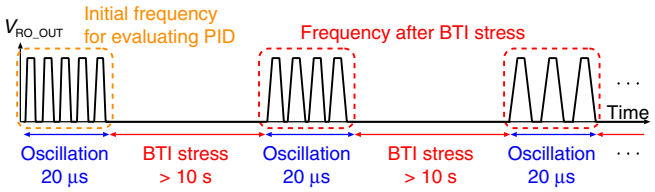


Fig. 9. (Color online) Measurement flow for BTI-induced degradation. Oscillation and BTI stress are repeated. The BTI stress time is more than 10 s to dominate BTI-induced degradation.

than those of REF-SW as shown in Fig. 7(b). $|V_{th}|$ decreases owing to PID in NMOS. This result is explained by positive charge damage in HK dielectrics.[30] The fabricated FDSOI process uses thick SiON and thin HK to control V_{th} through gate work functions. $|V_{th}|$ decreases owing to the positive charge damage in HK. However, if SiON suffers from PID, $|V_{th}|$ increases whether the charge is positive or negative as shown in Fig. 8. $|V_{th}|$ decreases in all metal layers owing to the positive charge damage in HK. From the results in Fig. 7, positive charge damage decreases $|V_{th}|$ equally with antennas in all metal layers. PID on SiON becomes dominant and then $|V_{th}|$ increases in the upper metal layers. Frequency fluctuations are canceled out by PMOS and NMOS in the lower antenna layers in the CMOS structure. However, performance degrades in the upper layers because the $|V_{th}|$ values of both PMOS and NMOS increase.

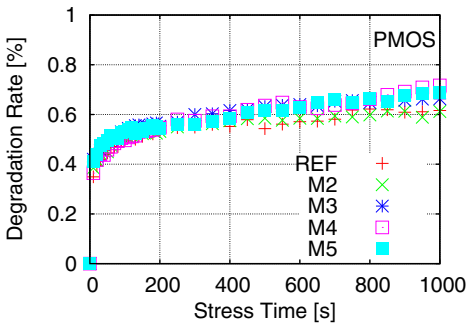
3.2 BTI-induced degradation

Figure 9 shows how to measure BTI-induced degradations. ROs oscillate for 20 µs and stop oscillating for over 10 s after measuring the frequency that dominates BTI-induced degradation. The frequency is measured again after BTI stress. The measured frequency decreases owing to BTI-induced degradation. The oscillation and BTI stress are repeated. The measurements are performed at a temperature of 120 °C and a supply voltage of 2.0 V to accelerate BTI-induced degradation. Degradation rate (D_{rate}) is calculated as

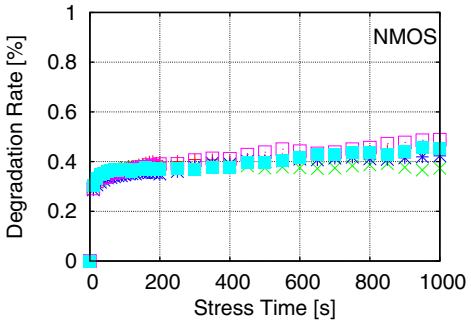
$$D_{rate} = \frac{f_0 - f(t)}{f_0}, \quad (3)$$

where f_0 is the initial frequency at $t = 0$ and $f(t)$ is the measured frequency at time t.

Figure 10 shows the measured BTI-induced degradations. The X-axis shows the BTI stress time and the Y-axis D_{rate}. Dots indicate the average D_{rate} of 70 ROs. The D_{rate} values of both PMOS [Fig. 10(a)] and NMOS [Fig. 10(b)] increase with time. The D_{rate} of PMOS is 1.5 times larger than that of NMOS at 1,000 s. NBTI is more dominant than PBTI, which coincides with previous research results.[19,31] The difference



(a)



(b)

Fig. 10. (Color online) Measured BTI-induced degradations. (a) PMOS type. (b) NMOS type.

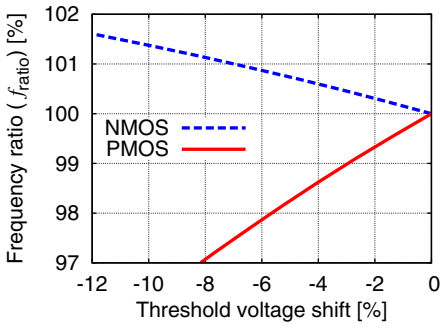


Fig. 11. (Color online) Simulated V_{th} shifts. Frequency ratios are proportional to threshold voltage shift (ΔV_{th}).

in D_{rate} is only less than 0.1% among the antenna layers. The BTI-induced degradation is almost the same in all antenna layers.

4. Degradations converted to V_{th}

We convert frequency fluctuation to V_{th} shift on current-starving switches using circuit simulations. The V_{th} of those switches changes because the switches suffer from PID, but the transistors in ROs do not. The simulated circuits include parasitic capacitance and resistance extracted from layout patterns. Frequency oscillations are simulated by changing the V_{th} of PID-SW. Figure 11 shows the simulation results. The X- and Y-axis show V_{th} shift (ΔV_{th}) and the frequency ratio based on the frequency without degradation, respectively. This results are obtained by changing the V_{th} of M2 PID-SWs. Simulation results are almost the same in all antenna layers because all MOSFET-SWs have almost the same gate, source, and drain areas, and parasitic capacitance and resistance on metal layers. $|V_{th}|$ is increased and

Table I. V_{th} conversion results at time 0 degradation by PID.

	$-\Delta V_{th}$ (%)			
	M2	M3	M4	M5
PMOS	3.8	3.7	5.6	8.4
NMOS	11	11	8.0	0.33

decreased in PMOS and NMOS, respectively, to fit to measured initial frequencies. Frequency ratios of PMOS and NMOS are proportional to ΔV_{th}. Frequency ratios from measurement results are the same as those from simulation results. For example, frequency ratios are 98.7% in PMOS of the M2 antenna layer from both measurement and simulation results, which corresponds to ΔV_{th} of 3.8%. All measured frequency ratios are similarly converted to ΔV_{th}. Table I shows the results of V_{th} conversion. The ΔV_{th} of M5-PID-SW in NMOS is only 0.33%. However, its maximum values are 8.4 and 11% in PMOS and NMOS, respectively. Chip designers should consider V_{th} shifts caused by PID, particularly that depending on the type of antenna layers.

5. Conclusions

We fabricated ROs in the 65 nm FDSOI process to evaluate PID and BTI depending on the type of antenna layer. Current-starved ROs with wires on different antenna layers can separate degradations in PMOS and NMOS, and evaluate those degradations depending on the type of antenna layer. NOR-type current-starved ROs do not suffer from BTI in MOSFETs in ROs themselves but suffers from BTI in current-starved switches. Oscillation frequencies of ROs with antennas are compared with those without antennas. Initial frequencies of PMOS-SWs decrease in upper antenna layers. However, ROs of NMOS-SWs with antennas become faster than those without antennas because high-k dielectrics are damaged by positive charge. BTI-induced degradation in PMOS is 1.5 times larger than that of NMOS. However, BTI-induced degradation is almost the same in all antenna layers. Frequency fluctuations at time 0 caused by PID are converted to V_{th} shifts. V_{th} on both PMOS and NMOS transistors shift by 8.4 and 11%, respectively, in the worst case. V_{th} shifts caused by PID should be considered during chip design.

Acknowledgments

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