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Radiation hardness evaluations of 65 nm fully depleted silicon on insulator and bulk processes by measuring single event transient pulse widths and single event upset rates

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We measure single event transient (SET) pulse widths on inverter chains and single event upset (SEU) rates on flip-flops (FFs) fabricated in 65 nm fully depleted silicon on insulator (FD-SOI) and bulk processes. The layout designs of test chips are strictly identical between their processes besides buried oxide (BOX) layers. Experimental results show that neutron-induced SEU and SET rates in the FD-SOI process are 230× and 450× lower than those in the bulk process, respectively. © 2015 The Japan Society of Applied Physics

1. Introduction

According to process scaling down to nanometers, LSI is more sensitive to radiation effects in space and terrestrial environments. At ground level, single event effects (SEEs) are significant issues for LSI reliability, which is caused by α particles and neutrons. When a charged particle is incident on the LSI, its ionizing effect generates electron–hole pairs in p- and n-wells. Generated charge is collected into a transistor's drain region and its output is temporally flipped, which is called a soft error. If a charged particle is incident on a combinational circuit, it induces a transient pulse, which is named a single event transient (SET). In contrast, if a charged particle is incident on a storage cell such as static random access memories (SRAMs) and flip-flops (FFs), its stored value is flipped. It is called a single event upset (SEU). Soft error rates (SERs) per chip increase according to the process scaling since transistor density exponentially increases yearly.[1] Therefore, a radiation-hardened design is required to achieve high reliability in advanced technologies.

The triple modular redundancy (TMR) FF is the fundamental circuit design for the reliability, which consists of three identical FFs and a majority-voting circuit.[2] The output of the TMR FF is determined by majority voting of three FFs and it remains correct even if a particle is incident on one FF and flips its stored value. The TMR FF has strong radiation resilience while it occupies a huge area and consumes much power. However, the soft error resilience on radiation-hardened FFs is markedly reduced in the 90 nm process and beyond. Jagannathan et al. reported neutron- and α-particle-induced SERs on 40 nm TMR FF and several redundant FFs.[3] TMR FF has only 3.3× higher soft error resilience than non redundant FF owing to multi-node charge collection.[4] A radiation strike can flip several nodes, and these flips are simultaneous flips of stored values.

Fully depleted silicon on insulator (FD-SOI) transistors are one of the most effective solutions for the single event effect.[5–7] In an SOI process, transistors are separated into the p- and n-well by buried oxide (BOX) layers. Almost all of the generated charge cannot be collected into a drain region, when a particle is incident on a chip and generates electron–hole pairs in the p- and n-wells. Therefore, SOI transistors have higher soft error resilience than bulk transistors without area, delay, and power penalties.

In this work, we measure neutron-induced SEU and SET in a 65 nm FD-SOI technology and a 65 nm bulk technology.[8] The layout designs of test chips are strictly identical between FD-SOI and bulk processes except for thin BOX layers. Test chips consist of a shift-register-based flip-flop array and 6 types of inverter chain with a time-to-digital converter in order to measure SEU rates on FFs and SET pulse widths.

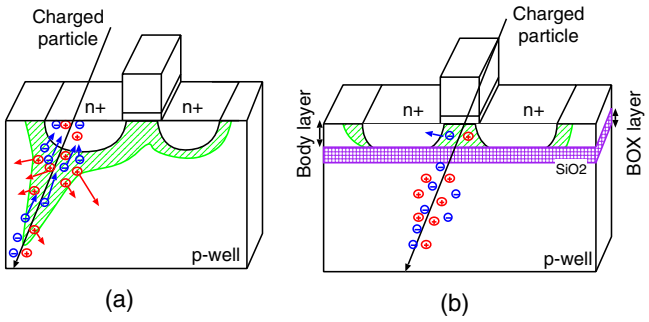

Fig. 1. (Color online) Single event effect on a bulk transistor and on a SOI transistor: (a) bulk process and (b) SOI process.

The paper is organized as follows. In Sect. 2, we explain soft error mechanisms in bulk and FD-SOI processes. In Sect. 3, we explain the test circuit structure. In Sect. 4, we discuss the experimental results. In Sect. 5, we conclude this paper.

2. Soft error mechanism

At ground level, soft errors are caused by α particles emitted from package material and neutrons generated in the atmosphere by cosmic rays.[9] When an α particle is incident on a bulk transistor, electron–hole pairs are generated by its ionizing effect along the particle track, as shown in Fig. 1(a). Generated electrons in the p-well are collected into the drain region of the nMOS transistor by funneling, drift, and diffusion.[10] The drain output can be flipped by collected electrons transiently. Its radiation effect is termed a SEE. In contrast, neutrons do not generate electron–hole pairs directly. Their effects occur through nuclear collisions with Si atoms, which generate secondary particles. Then, they generate electron–hole pairs. When electron–hole pairs are generated in a combinational circuit, they induce a transient voltage pulse on any node in a circuit, which is called a SET. When electron–hole pairs are generated in a sequential element, they may flip the stored value, which is called a SEU.

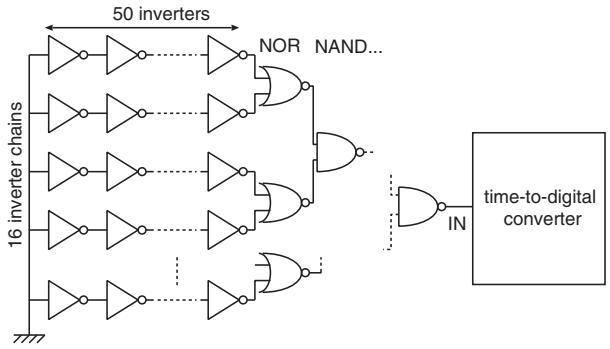

Fig. 2. Schematic circuit diagram of embedded inverter chain and time-to-digital converter.

In an FD-SOI process, transistors are separated from p- and n-wells by BOX layers as shown in Fig. 1(b). Radiation-induced carriers in well regions are not collected into drain regions, and carriers in a body are only collected. In a bulk process, the charge-collection range by funneling is several hundred nanometers, which is used in the depth of sensitive volume for soft error simulation.[11,12] In contrast, the body thickness in fabricated FD-SOI process is 12 nm. Therefore, the amount of collected charge is much smaller in the FD-SOI transistor than in the bulk transistor and FD-SOI transistor achieves a high soft error resilience.[6,13–15]

3. Test circuit structure

To measure the SET pulse width on inverters and SEU on FFs, we implement two test circuits. In this section, we explain them in detail.

3.1 SET pulse width measurement circuit

Inverter chains and time-to-digital converters (TDCs) are embedded to measure SET pulse width distributions. Figure 2 shows the schematic circuit diagram of embedded inverter chains and a TDC. It is connected to a 16-inverter chain through the logic tree of NAND and NOR gates. Each inverter chain consists of 50 inverters. This structure suppresses the propagation-induced effect and measures SET pulse widths accurately.[16,17] The propagation-induced effect implies that injected SET pulses are broadening or shrinking linearly while SET pulses propagate through a logic chain. It is explained by the hysteretic modulation in the threshold voltage by the floating body effect and negative bias temperature instability (NBTI).[18] Some researchers report that the pulse modulation amount is less than 2 ps per inverter.[18–21] We assume that the modulation amount is less than 100 ps even if the SET pulse is injected in the first inverter of the implemented inverter chain.

Figure 3 shows a circuit structure for measuring SET pulse widths. The implemented TDC is based on a ring oscillator and a counter.[22] The SET pulse width is roughly measured by a counter circuit and precisely measured by D-latches. If an SET is injected from the target, the NAND gate is activated and the ring oscillator remains oscillating while the SET pulse is injected, as shown in Fig. 4. The counter detects fall transitions of the ring oscillator and counts its frequency, while the latches hold each output value of the logic gates in the oscillator immediately when the ring oscillator stops. The

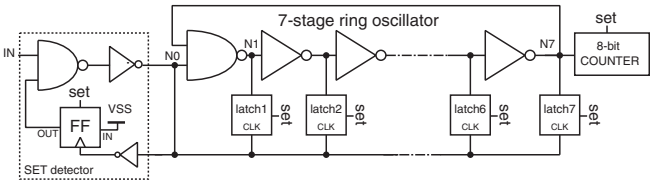

Fig. 3. Time-to-digital converter to measure SET pulse width.

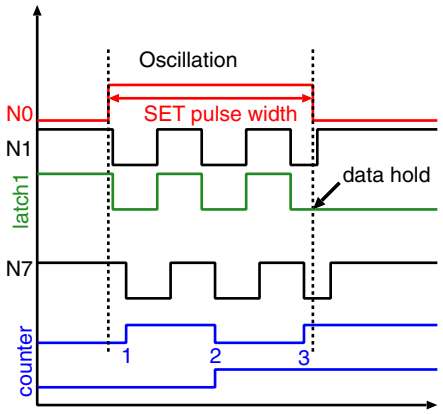

Fig. 4. (Color online) Operating example of time-to-digital converter.

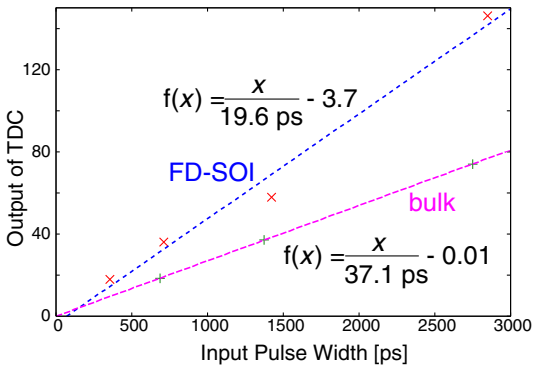

Fig. 5. (Color online) Calibration results of TDC fabricated in 65 nm FD-SOI and bulk processes.

SET pulse width can be computed on the basis of the number of oscillations stored in the counter and the states of the latches. Therefore, it can measure SET pulse widths by the resolution of the delay time of the inverter in the ring oscillator. When two SET pulses are injected in the inverter chain, the counter counts the sum of their widths. One FF and a NAND gate are inserted to detect an SET occurrence and block another SET pulse from the inverter chain. The signals called "set" are external inputs, which are used to initialize stored values of the counter, the D-latches, and the FF.

We implement 7-stage ring oscillators and dividers to generate rectangular pulses. We measure their pulse widths using the TDCs fabricated in 65 nm FD-SOI and bulk processes in order to obtain the resolution of TDCs. Figure 5 shows the calibration results. The resolutions of the TDCs are 19.6 and 37.1 ps, respectively, when the supply voltage is 1.2 V. The FD-SOI transistors have a lower threshold voltage and higher a on-state current than the bulk transistor. The FD-SOI transistors also have a smaller junction capacitance

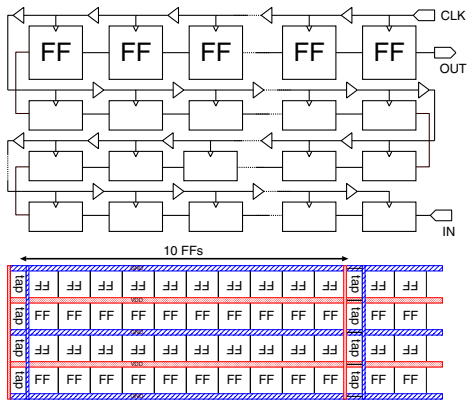

Fig. 6. (Color online) Schematic structure of the FF array.

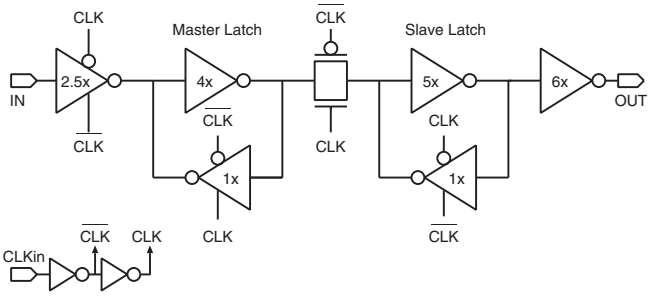

Fig. 7. Schematic structure of the implemented FF.

between the diffusion region and the well region since the thin BOX layer is inserted between them, and the BOX layer is thicker than the depletion region of the bulk transistor. Thus, the resolution is better in the FD-SOI process than in the bulk process. In the circuit-level simulation, delay times of an inverter with fanout 1 are 21.1 ps in the 65 nm bulk process and 13.3 ps in the 65 nm FD-SOI process.

3.2 FF array for measuring SEU rates

To measure SEU rates on FFs, we prepare an FF array on the basis of a shift register, which is constructed using FFs and a clock buffer chain.[23,24] Figure 6 shows the schematic of the FF array and Fig. 7 shows that of the implemented FF. It has no clock tree to simplify the layout structure, and clock buffer chains are used to apply a clock signal. Well contacts are inserted every 10 FFs to stabilize the well potential in the implemented FF array. In accelerated tests, the FF array is initialized using an arbitrary pattern. During irradiation, its clock signal is fixed at "0" or "1" in order to maintain the stored value. All stored values are retrieved after irradiation and compared with the initial pattern. The soft error rate can be calculated from the number of flipped stored values, neutron flux, and the number of implemented FFs.

3.3 Test chip structure

Figure 8 shows the fabricated test chip micrograph with a floor plan and a layout pattern. Test chips were fabricated in the bulk process and the thin BOX FD-SOI process named SOTB. In the SOTB process, the thicknesses of the BOX layer and body layer are 10 and 12 nm, respectively. The layout designs of the test chips are strictly identical between SOTB and bulk processes in order to compare soft error rates.

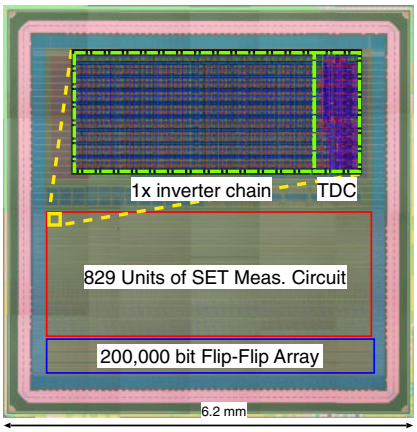

Fig. 8. (Color online) Fabricated test chip micrograph with floor plan and layout pattern.

Table I. The parameters of implemented inverter chains.

Inverter chain	Drive strength	Fanout	Well-contact interval (μm)	Drain area (arb. unit)
1×	1	1	50	1
1×WC	1	1	2	1
1×FO2	1	2	50	1
1×FO4	1	4	50	1
2×	2	1	50	1
4×	4	1	50	2

However, the channel impurity concentrations and the threshold voltage of the SOTB transistors are lower than those of the bulk transistors.[25] The test chip includes 829 units of SET pulse measurement circuits and a 140,000 bit FF array. To measure the dependences of SETs, we implemented 6 different types of inverter chain. The parameters of the implemented inverter chains are summarized in Table I, and Fig. 11 shows their layout structures.

4. Experimental results

4.1 Experimental setup

Accelerated tests were performed by the spallation neutron beam at the research center for nuclear physics (RCNP), Osaka University. Figure 9 shows the neutron beam spectrum in comparison with the terrestrial neutron spectrum at the ground level of New York. The average accelerated factor is 2.9×10^8. We measured 12 FD-SOI test chips and 12 bulk test chips simultaneously using stacked DUT boards, as shown in Fig. 10. Their supply voltages were fixed at 1.2 V. All stored values of the FF array are initialized to "0" or "1". Therefore, the SET pulses on clock buffer chains are negligible since they cannot flip the stored values on FFs. During irradiation, the clock signal is fixed at "1" or "0" to keep the master latches or slave latches in FFs in the hold state. The stored values on the FF array and TDCs are retrieved and initialized every 7 min.

4.2 Comparison of SEU rates and SET rates between the FD-SOI and the bulk processes

Table II shows SEU rates on the FD-SOI and bulk FFs. We

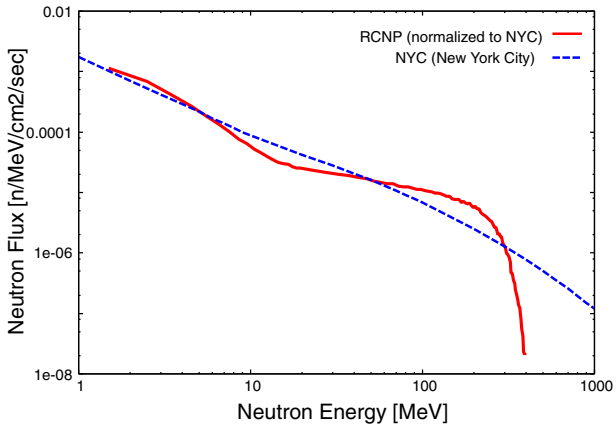

Fig. 9. (Color online) Neutron spectrum at RCNP.

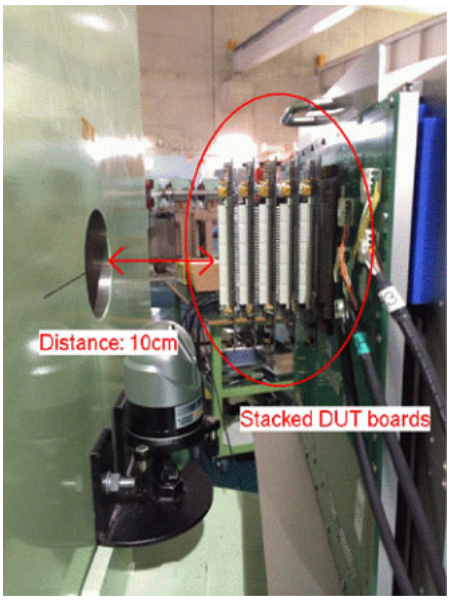

Fig. 10. (Color online) Stacked DUT boards.

Table II. SEU rates on FD-SOI and bulk FFs.

Stored values	FD-SOI	Bulk
	SEU rate (FIT/Mbit)	SEU rate (FIT/Mbit)
ALL1	3.5	620
ALL0	1.6	630

use failure in time (FIT) as the unit of error rate. One FIT equals one failure per billion hours (about 110,000 years). The average SEU rate is 230 times lower on the FD-SOI FFs than on the bulk FFs. This result corresponds to the SEU rate on SRAM cells in the 28 nm thin BOX FD-SOI process.[26] In this measurement, only one SEU is observed in FD-SOI FFs when all stored values are initialized to ALL0. Therefore, the difference between ALL0 and ALL1 in FD-SOI is caused by the measurement error. The enhancement of soft error resilience by the FD-SOI technology is larger than that by radiation-hardened designs such as dual interlocked storage cell (DICE) latches.[27,28] The FD-SOI technology can

Table III. SET rates on FD-SOI and bulk inverter chains.

Inverter	FD-SOI		Bulk	
	SET rates (FIT/Minv.)	Average SET pulse width (ps)	SET rate (FIT/Minv.)	Average SET pulse width (ps)
1×	0.0	N/A	88	185
1×WC	0.0	N/A	58	159
1×FO2	0.0	N/A	46	195
1×FO4	0.0	N/A	26	202
2×	0.0	N/A	40	156
4×	0.4	78	24	180

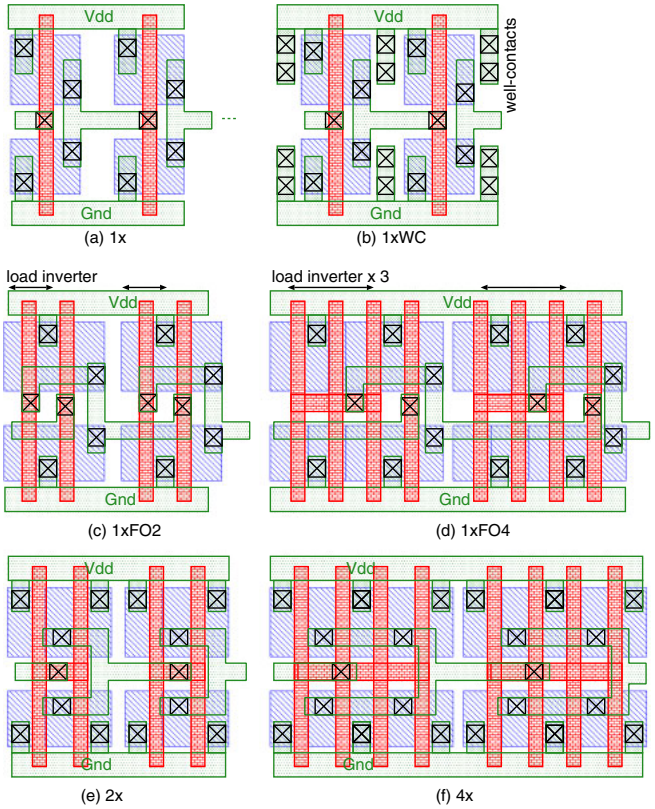

Fig. 11. (Color online) Layout structures of implemented inverter chains. Well-contacts are inserted every 50 μm in all inverter chains except (b).

effectively enhance soft error resilience without area, delay, and power consumption penalties.

Table III shows SET rates on the FD-SOI and bulk inverter chains. Only one SET pulse was injected in the FD-SOI inverter chains in 41 measurements (approximately 5 h of neutron irradiation). Its pulse was observed in the 4× inverter chain. We assume that it is caused on the NAND and NOR tree, as shown in Fig. 2, since their on-current and gate capacitance are smaller than those of 4× inverter and they are more sensitive to SEEs. On average, the FD-SOI inverters are 450× less susceptible than the bulk inverters. In the bulk process, SETs are observed in all inverter chains. The 1× inverter has highest SET rate and other inverters have only 1.5× – 3.5× higher error resilience than the 1× inverter. Therefore, it is difficult to completely eliminate soft errors by resizing the gate widths of transistors and by connecting an extra load capacitance in the bulk process.

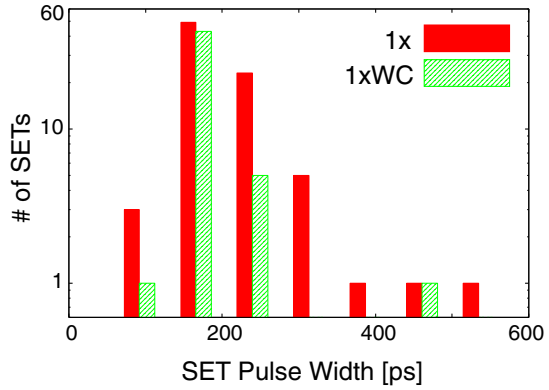

Fig. 12. (Color online) SET pulse width distributions on 1× and 1×WC inverter chains in the 65 nm bulk process. 1× inverter chains have 50 µm well-contact intervals while 1×WC inverter chains have 2 µm well-contact intervals.

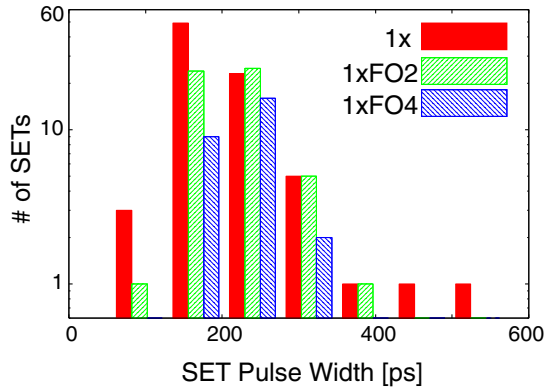

Fig. 13. (Color online) SET pulse width distributions on 1×, 1×FO2, and 1×FO4 inverter chains in the 65 nm bulk process.

4.3 SET pulse width distribution in the 65 nm bulk process

Figure 12 shows SET pulse width distributions on 1× and 1×WC inverter chains in the 65 nm bulk process. 1× inverter chains have 50 µm well-contact intervals while 1×WC inverter chains have 2 µm well-contact intervals. SET pulse widths are roughly exponentially distributed. The average SET pulse width on 1×WC inverters is shorter than that on 1× inverters, and the 1×WC inverter chains have only one SET over the 300 ps pulse width. It is because high-density well-contacts suppress the well-potential perturbation, and parasitic bipolar transistors are not turned on by radiation strikes.[29] These results correspond to heavy-ion-induced SET results[30,31] and our previous results.[21]

Figure 13 shows SET pulse width distributions on 1×, 1×FO2, and 1×FO4 inverter chains and Fig. 14 shows SET pulse width distributions on 1×, 2×, and 4× inverter chains. Although the number of SETs is reduced according to fanout or drive strength, these inverters have almost similar distributions and average SET pulse widths.

The distributions of SET pulse widths in the 65 nm bulk process show that the soft error rate caused by SET pulses can not be reduced markedly by circuit-level mitigation techniques, such as gate-width resizing and by connecting an extra load capacitance. Compared with 1× inverters, 4× inverters have about 1/4 of the SET rate, a similar average

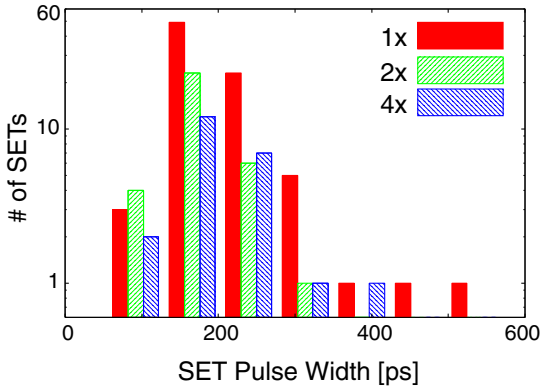

Fig. 14. (Color online) SET pulse width distributions on 1×, 2×, and 4× inverter chains in the 65 nm bulk process.

SET pulse width, and 4/5 maximum SET pulse width in this measurement. In contrast, soft errors by the SET pulse can be reduced markedly by device-level mitigation techniques. FD-SOI inverters are 450× less susceptible than the bulk inverters. When we fabricate an LSI with 450× higher error resilience in the 65 nm bulk process, we need TMR FFs and over 500 ps delay elements to eliminate the SET pulse caused on the combinational circuit. Therefore, the FD-SOI transistor can effectively improve soft error resilience.

5. Conclusions

We fabricated a test circuit with strictly identical layout designs in FD-SOI and bulk processes and measured SEU rates and SET pulse width distributions. Neutron irradiation experimental results show that neutron-induced SEU and SET rates in the FD-SOI process are 230× and 450× lower than those in the bulk process, respectively. As for SET pulse widths in the bulk process, the number of SETs is reduced according to fanout, drive strength or high-density well contacts. However, it is difficult to completely eliminate SETs by their method. The thin-BOX FD-SOI technology can effectively enhance soft error resilience without area, delay and, power consumption penalties.

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