

Structural Dependence of Source and Drain Series Resistance on Saturation Drain Current for Sub-20 nm Metal-Oxide-Semiconductor Field-Effect Transistors

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The structural dependence of series-resistance effects on saturation currents is investigated in sub-20 nm metal-oxide-semiconductor field-effect transistors (MOSFETs). For planar bulk, silicon-on-insulator (SOI), and multigate (MG) MOSFETs, reduction rates of the saturation currents are calculated using an analytical current model in high-performance (HP), low operating power (LOP), and low standby power (LSTP) technologies. In HP technology, the reduction rates are 29.0, 25.3, and 22.1% for bulk, SOI, and MG MOSFETs, respectively. In LOP technology, the reduction rates are 23.8, 21.5 and 20.7% for bulk, SOI, and MG MOSFETs, respectively. In LSTP technology, the reduction rates are about 17% for all devices. In HP technology, the ratio of the series resistance to a channel resistance is the dominant factor for the reduction rate. In LOP, the ratio of the over-drive voltage to the supply voltage is the dominant factor. In LSTP, both the resistance and voltage ratios are the dominant factors.

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1. Introduction

The metal-oxide-semiconductor field-effect transistors (MOSFETs) have been scaled as important parts of integrated circuits to satisfy the demands of higher speed, increased compactness, and improved reliability. The continuous scaling has major problems such as short-channel effects and leakage currents. These problems can be suppressed by structural changes from planer bulk to fully depleted silicon-on-insulator (SOI) and multi gate (MG) MOSFETs such as tri-gate, gate all around MOSFETs, and fin field-effect transistor (FinFET).¹⁻⁴⁾ Actually, tri-gate transistor is used with fully depleted operation as 22 nm logic technology.^{5,6)} Using the tri-gate transistor improves the electrostatic control of the channel in sub-20 nm gate-length regime.⁷⁻⁹⁾ In these advanced MOSFETs, as the fin or channel regions are extremely scaled, tall and narrow extended source and drain regions are formed. The extended regions lead to higher source and drain series resistance.¹⁰⁻¹²⁾ Effects of the series resistance on drain currents increase as supply voltages decrease to reduce the power consumption.^{13,14)} Therefore, the effects of the series resistance on drain currents becomes a non-negligible factor in sub-20 nm gate-length regime.^{15,16)}

The series resistance has been important issues for modeling I - V characteristics of the extremely scaled MOSFETs. Many works¹⁷⁻²⁴⁾ have modeled about the effects of the series resistance on I - V characteristics. Analytical current models are approximated using the Taylor expansion of the series resistance. The models have been researched and analyzed at the saturated current region in the works. However, higher order effects of the series resistance are not mentioned in detail. In the past work,²⁵⁾ we derived a saturation current model including the higher order effects in sub-20 nm MOSFETs and investigated a gate length dependence of the series resistance on the saturation drain current on a bulk substrate. We found that the higher order effects in saturation currents increase as the gate length decreases in sub-20 nm MOSFETs.

In this work, we investigate the structural dependence of source and drain series resistance on the saturation drain current for planer bulk, SOI, and MG MOSFETs in sub-20 nm technology nodes. We briefly review the analytical current model.²⁵⁾ We describe model simulation methods and parameters of sub-20 nm MOSFETs. A reduction rate of the saturation drain current owing to the effect of the series resistance is calculated in complementary metal oxide semiconductor (CMOS) logic technologies. The reduction rates and expansion components of the saturation current are discussed

to clear relationships between physical parameters and the current reduction.

2. Analytical Saturation Drain Current Model

The effect of the series resistance in saturation drain current can be examined by using an equivalent circuit. The equivalent circuit is assumed that a circuit consists of an intrinsic MOSFET, a source resistance, and a drain resistance as the series resistance.²⁶⁾ The drain current flows through the drain resistance, the channel, and the source resistance. At that time, a voltage drop occurs owing to the resistances. The saturation current including the effect of the series resistance I_{Dsat} is used as follows:²⁵⁾

$$I_{\text{Dsat}} = I_{\text{Dsat0}}(1 + a_1 R_S + a_2 R_S^2 + a_3 R_S^3 + a_4 R_S^4 + O(R_S^5)), \quad (1)$$

where I_{Dsat0} is the intrinsic saturation current, R_S is the source resistance as the series resistance, a_N are coefficients of the source resistance, and $O(R_S^5)$ is the sum of the higher-order terms higher than 4th term. The drain resistance (R_D) is not contained in eq. (1), because the intrinsic saturation current is the function of a gate voltage. The saturation current I_{Dsat0} per unit channel width when $R_S = R_D = 0 \text{ } \Omega \cdot \mu\text{m}$ is used as follows:^{27,28)}

$$I_{\text{Dsat0}} = \frac{1}{2} \mu_{\text{eff}} C_{\text{ox}} \frac{(V'_{\text{GS}} - V_{\text{th,on}})^2 E_c}{(V'_{\text{GS}} - V_{\text{th,on}}) + L_{\text{el}} E_c (1 + d)}, \quad (2)$$

$$E_c = 2 \frac{\nu_{\text{sat}}}{\mu_{\text{eff}}}, \quad (3)$$

$$d = \frac{q N_{\text{ch}} \sqrt{2 \varepsilon_s (2 \varphi_{\text{F}} - V_{\text{b}}) / q N_{\text{ch}}}}{2 C_{\text{ox}} (2 \varphi_{\text{F}} - V_{\text{b}})}. \quad (4)$$

In eq. (2), μ_{eff} is the effective mobility, C_{ox} is the gate capacitance per unit area, V'_{GS} is the internal voltage of a gate-source voltage, $V_{\text{th,on}}$ is the threshold voltage at the on-state, E_c is the critical electric field, and L_{el} is the effective channel length. In eq. (3), the electron saturation velocity ν_{sat} is assumed to be a constant ($= 1.1 \times 10^7 \text{ cm/s}$), and the effective mobility is assumed as a function of effective field. In eq. (4), q is the electric charge, N_{ch} is the channel doping concentration, ε_s is the silicon permittivity, φ_{F} is the quasi-Fermi potential in electron volts, and V_{b} is the applied substrate voltage. The coefficients in eq. (1) are used as follows:

$$a_1 R_S = \left(\frac{R_S}{R_{\text{ch}}} \right) \cdot \left(\frac{V_{\text{dd}}}{V_{\text{gt}}} \right) \cdot (\alpha - 2), \quad (5)$$

$$a_2 R_S^2 = \left(\frac{R_S}{R_{ch}} \right)^2 \cdot \left(\frac{V_{dd}}{V_{gt}} \right)^2 \cdot \left(2\alpha^2 - 6\alpha + 5 \right), \quad (6)$$

$$a_3 R_S^3 = \left(\frac{R_S}{R_{ch}} \right)^3 \cdot \left(\frac{V_{dd}}{V_{gt}} \right)^3 \cdot \left(5\alpha^3 - 20\alpha^2 + 28\alpha - 14 \right), \quad (7)$$

$$a_4 R_S^4 = \left(\frac{R_S}{R_{ch}} \right)^4 \cdot \left(\frac{V_{dd}}{V_{gt}} \right)^4 \cdot \left(14\alpha^4 - 70\alpha^3 + 135\alpha^2 - 120\alpha + 42 \right), \quad (8)$$

$$\alpha = \frac{V_{gt}}{V_{gt} + L_{el} E_c (1 + d)}, \quad (9)$$

where R_{ch} is a channel resistance (V_{DD}/I_{Dsat0}). In eqs.(5)-(8), each expansion component of the series-resistance effect has the following physical meaning. The first components are the ratios of the source resistance to the channel resistance. The second components are the ratios of the supply voltage to the overdrive voltage. The third components are the functions of V_{gt} , L_{el} , E_c , and d .

3. Simulation

The saturation current including the effect of the series resistance is compared with the current without the effect to investigate the resistance effect on the saturation current for bulk, SOI, and MG MOSFETs. The reduction rate of the saturation current is defined as follows:

$$\frac{|I_{Dsat} - I_{Dsat0}|}{I_{Dsat0}}, \quad (10)$$

where I_{Dsat0} is the saturation drain current without the resistance effect calculated using eq. (2) and the saturation drain current including the resistance effect I_{Dsat} is calculated using eq. (1). Values of the parameters used in the simulated devices are shown in Table I. L_g and V_{dd} are chosen from the International Technology Roadmap for Semiconductors (ITRS) 2007.²⁹⁾ ITRS publishes annual reports focusing on high-performance (HP), low-operating-power (LOP), and low-standby-power (LSTP) technologies in logical devices. The source resistance per unit gate width is calculated under the assumption that R_S is one-half of R_{SD} . V_{gt} is given by

$$V_{gt} = V_{dd} - V_{th,on}, \quad (11)$$

$$V_{th,on} = V_{t,sat} + \Delta V, \quad (12)$$

where $V_{th,on}$ is the saturated threshold voltage used for on-state current calculation. $V_{th,on}$ is modified by adding a modified model parameter ΔV to a saturated threshold voltage $V_{t,sat}$.³⁰⁾ ΔV is assumed to be 0.03 V. The saturated threshold voltage $V_{t,sat}$ is used for the extrapolation of channel leakage current at $V_{GS} = 0$ and $V_{DS} = V_{dd}$. EOT is the equivalent oxide thickness. L_{el} , μ_{eff} , E_c , d , and EOT are calculated by using the MASTAR³⁰⁾ results. The model for the assessment of CMOS technologies and roadmaps (MASTAR) is an analytical model used in ITRS. C_{ox} is identical to the electronic gate-oxide capacitance $C_{ox,elec}$ in the result of the MASTAR. In the MASTAR, the source and drain resistances R_{SD} were used as the source resistance. However, one-half of the source and drain resistances is used as the source resistance in this work. The reduction rates of the saturation current are calculated for bulk, SOI, and MG MOSFETs in HP, LOP, and LSTP technologies.

A key transistor performance of the requirements is the intrinsic switching frequency ($1/\tau = I/CV$) for device scaling in the ITRS reports. Scaling targets of this parameter are 13 - 17% improvement per year. In HP technology, to scale the device with the improvement, the scaling of the gate oxide thickness is important. However, the gate leakage current due to direct tunneling increases exponentially as the gate oxide thickness decreases above 1.2 nm. Therefore, the gate leakage current density is a critical issue. EOT is set as thin as possible with the tolerable gate leakage current density. As the structure of MOSFETs changes the planner bulk to the SOI or MG MOSFETs, the requirement of EOT increases from 0.55 nm at the planner bulk to 0.60 nm at the SOI or 0.80 nm at the MG MOSFETs because the gate electrodes are performed more than one side. To compensate this loss, the carrier mobilities in channel regions increase 265, 327, 416 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ for the bulk, SOI and MG MOSFETs as the structure changes, respectively. In LOP technology, to scale the device with the low operating power, the lowering of the supply voltage is the most effective way to decrease the dynamic power consumption. In order to keep the reasonable saturation current with the lowest supply voltage ($= 0.7$ V), the threshold voltage has to be reduced as small as possible. The threshold voltage is reduced by the more effective gate control as the structure of MOSFET changes. This merit enhances the overdrive voltage. The overdrive voltages increase from 424 mV at the planner bulk to 452 mV at the SOI or 463 mV at the MG MOSFETs. In LSTP technology, to scale the device with the low standby power, the suppression of the off-state leakage current is important. To achievement the low leakage current needs to increase the threshold voltage. The threshold voltage follows

the supply voltage to gallant the reasonable overdrive voltage. However, the thickest EOT (1.2 - 1.4 nm) influenced by the smallest requirement of the gate leakage current density get worth the device performance. As the structure changes, this demerit can be suppressed by the improvement of the carrier mobility in the channel region.

4. Results

Table II shows the calculated saturation currents and the reduction rates of the current for bulk, SOI, and MG MOSFETs in HP, LOP, and LSTP technologies.

Figure 1 shows the reduction rates of the saturation current influenced by the series resistance for bulk, SOI, and MG MOSFETs in HP, LOP, and LSTP technologies. In HP technology, the reduction rates are 29.0, 25.3, and 22.1% for bulk, SOI, and MG MOSFETs, respectively. In LOP technology, the reduction rates are 23.8, 21.5 and 20.7% for bulk, SOI, and MG MOSFETs, respectively. In LSTP technology, the reduction rates are 17.5, 16.7, and 16.6% for bulk, SOI, and MG MOSFETs, respectively. The reduction rate decreases in all technologies as the structure of MOSFETs is advanced.

Differences of the reduction rates compared with each structure are different for each technology. Figure 2 shows difference of the reduction rates between each structure in HP, LOP, and LSTP technologies. The differences of the reduction rates between bulk-SOI, bulk-MG, and SOI-MG are 3.7, 6.9, and 3.2% in HP technology, respectively. The differences of the reduction rates between bulk-SOI, bulk-MG, and SOI-MG are 2.3, 3.1, and 0.8% in LOP technology, respectively. The differences of the reduction rates between bulk-SOI, bulk-MG, and SOI-MG are 0.8, 0.9, and 0.1% in LSTP technology, respectively. The differences of the reduction rate are largest in HP technology. The differences of the reduction rate between bulk-SOI and bulk-MG are above 2%, that between SOI-MG is below 1% in LOP technology. The differences of the reduction rates are below 1% in LSTP technology. The reduction rate of the saturation drain current depends on the MOSFET structure in HP and LOP technologies. The reduction rate rarely depends on the MOSFET structure in LSTP technology.

5. Discussion

To investigate the physical reasons underlying the reduction rate decrease as the MOSFET structure changes, expansion components of the saturation current influenced by the series resistance are analyzed. The expansion components normalized by bulk MOSFET are compared with the other components of SOI and MG in HP, LOP, and LSTP

technologies. The calculated results of the expansion components are shown in Table III.

Figure 3 shows normalized expansion components of the saturation current including an effect of the series resistance in HP technology. Normalized first components for SOI and MG are 0.88 and 0.74, respectively. Normalized second components for SOI and MG are 0.98 and 1.01, respectively. Normalized third components for SOI and MG are 0.96 and 0.93, respectively. Normalized first components for SOI and MG structures decrease compared with bulk structure. Normalized second and third components for SOI and MG structures are almost constant compared with bulk structure. In HP technology, the ratio of the series resistance to the channel resistance is the dominant factor in the reduction rate of the saturation current. The ratio decreases owing to constant series resistance and increase of the channel resistance ($R_{ch} = V_{dd}/I_{Dsat0}$) as the MOSFET structure changes bulk to SOI and SOI to MG. The saturation current and gate oxide capacitance decrease owing to increase of the gate oxide thickness. Required gate oxide thickness increases as the MOSFET structure changes bulk to SOI and SOI to MG to control the gate leakage current.

Figure 4 shows normalized expansion components of the saturation current including an effect of the series resistance in LOP technology. Normalized first components for SOI and MG are 0.97 and 0.97, respectively. Normalized second components for SOI and MG are 0.94 and 0.92, respectively. Normalized third components for SOI and MG are 0.97 and 0.94, respectively. Normalized second components for SOI and MG structures decrease compared with bulk structure. Normalized first and third components for SOI and MG structures are almost constant compared with bulk structure. In LOP technology, the ratio of the over-drive voltage to the supply voltage is the dominant factor in the reduction rate of the saturation current. The ratio decreases owing to constant supply voltage and increase of the overdrive voltage as the MOSFET structure changes bulk to SOI. The overdrive voltage increases owing to decrease of threshold voltage by enhancement of gate controllability. The ratio of voltages is sensitive because the supply voltage is the smallest compared to other technologies. As the MOSFET structure changes SOI to MG, the ratio of voltages is almost constant owing to the effect of the gate controllability.

Figure 5 shows normalized expansion components of the saturation current including an effect of the series resistance in LSTP technology. Normalized first components for SOI and MG are 1.32 and 1.32, respectively. Normalized second components for SOI and MG are 0.79 and 0.81, respectively. Normalized third components for SOI and MG

are 0.90 and 0.88, respectively. Normalized first components for SOI and MG structures increase compared with bulk structure. Normalized second and third components for SOI and MG structures decrease compared with bulk structure. In LSTP technology, both the ratio of the series resistance to the channel resistance and the ratio of the over-drive voltage to the supply voltage are the dominant factors in the reduction rate of the saturation current. However, the reduction rate depends on the MOSFET structure rarely because the structural dependence is canceled by multiplying each component.

Requirements of the MOSFETs as the structure changes are different in each technology. A key transistor performance of the requirements is the intrinsic switching frequency for device design in Table I. In HP technology, the MOSFETs are focused on the highest switching frequency. The transistors have both the highest device performance and the highest gate leakage current density to improve the channel resistance. The ratio of the series resistance to the channel resistance is the main factor in the saturation current. Therefore, the ratio of the series resistance to the channel resistance is important in the reduction of the saturation current by the series resistance. In LOP technology, the MOSFETs are focused on reducing of the operating power dissipation by controlling the gate leakage current and the operating current. The transistors have lower performance and lower leakage current. To effectively reduce the power dissipation, the supply voltage is minimized. The ratio of the over-drive voltage to the supply voltage is the main factor in the saturation current. Therefore, a ratio of the over-drive voltage to the supply voltage is important in the reduction of the saturation current. In LSTP technology, the MOSFETs are focused on the gate leakage current and the off-state current. The transistors have both the lowest device performance and the lowest gate leakage current of all. The lower voltage and higher resistance ratios are main factors in the saturation current. Therefore, the voltage and resistance ratios are important in the reduction of the saturation current.

6. Conclusions

We investigated the structural dependence of the series-resistance effect on the saturation currents in sub-20 nm MOSFETs. The saturation currents including the resistance effect were calculated using the analytic current model for bulk, SOI, and MG MOSFETs. The calculated saturation currents were compared with the intrinsic saturation currents to calculate reduction rates of the saturation current in HP, LOP, and LSTP technologies.

In HP technology, the reduction rates are 29.0, 25.3, and 22.1% for bulk, SOI, and MG MOSFETs, respectively. In LOP technology, the reduction rates are 23.8, 21.5 and 20.7% for bulk, SOI, and MG MOSFETs, respectively. In LSTP technology, the reduction rates are 17.5, 16.7, and 16.6% for bulk, SOI, and MG MOSFETs, respectively. The reduction rate of the saturation drain current depends on structures of the MOSFETs as the structure of MOSFETs changes. In HP technology, a ratio of the series resistance to the channel resistance is the dominant factor in the reduction rate of the saturation current. In LOP technology, a ratio of the over-drive voltage to the supply voltage is the dominant factor in the reduction rate of the saturation current. In LSTP technology, both the resistance and voltage ratios are dominant factors because the structural dependence is canceled by multiplying the lower third component, the lower voltage and higher resistance ratios.

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Fig. 1. Reduction rate of the saturation current influenced by the series resistance for bulk, SOI, and MG structure in HP, LOP, and LSTP technologies.

Fig. 2. Difference of the reduction rates between each structure in HP, LOP, and LSTP technologies.

Fig. 3. Normalized expansion components of the saturation current including an effect of the series resistance in HP technology.

Fig. 4. Normalized expansion components of the saturation current including an effect of the series resistance in LOP technology.

Fig. 5. Normalized expansion components of the saturation current including an effect of the series resistance in LSTP technology.

Table I. Values of the parameters used for HP, LOP, and LSTP technologies in the simulated devices.

		High Performance			Low Operating Power			Low STandby Power		
		Bulk	SOI	MG	Bulk	SOI	MG	Bulk	SOI	MG
L_g	(nm)	16	16	16	20	20	20	22	22	22
L_{el}	(nm)	12.4	12.4	8.5	15.0	15.0	11.2	17.5	17.2	12.4
EOT	(nm)	0.55	0.60	0.80	0.80	0.90	0.90	1.20	1.30	1.40
V_{dd}	(V)	0.95	1.00	1.00	0.70	0.70	0.70	1.00	0.90	0.85
$V_{th,on}$	(mV)	131	119	145	276	248	237	582	425	410
E_c	(MV/cm)	8.31	6.72	5.29	3.76	3.32	3.17	5.57	3.48	3.37
R_S	($\Omega \cdot \mu\text{m}$)	90	90	90	95	95	95	90	100	105
C_{ox}	(fF/ μm)	42.0	34.5	28.8	30.5	26.5	26.5	22.9	20.3	19.2
μ_{eff}	($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	265	327	416	585	663	656	395	574	594
d		0.190	0.015	0.000	0.217	0.019	0.000	0.343	0.025	0.000
V_{gt}	(mV)	819	881	855	424	452	463	418	475	440
Switching Speed	(GHz)	2326	2778	2941	1333	1449	1449	806	980	980

Table II. Calculated results of the reduction rate on saturation current by the series resistance.

		High Performance			Low Operating Power			Low STandby Power		
		Bulk	SOI	MG	Bulk	SOI	MG	Bulk	SOI	MG
I_{Dsat0}	($\mu A/\mu m$)	3297	3051	2571	1226	1185	1187	800	854	770
I_{Dsat}	($\mu A/\mu m$)	2342	2280	2002	935	931	942	660	711	642
Reduction rate	(%)	29.0	25.3	22.1	23.8	21.5	20.7	17.5	16.7	16.6

Table III. Calculated expansion components of 1st-order terms in HP, LOP, and LSTP technologies.

	High Performance			Low Operating Power			Low STandby Power		
	Bulk	SOI	MG	Bulk	SOI	MG	Bulk	SOI	MG
First component	0.31	0.17	0.07	0.27	0.16	0.09	0.23	0.16	0.10
Second component	1.16	1.65	2.39	1.14	1.55	1.89	1.17	1.51	1.93
Third component	1.13	1.14	1.24	1.09	1.10	1.11	1.05	1.07	1.09

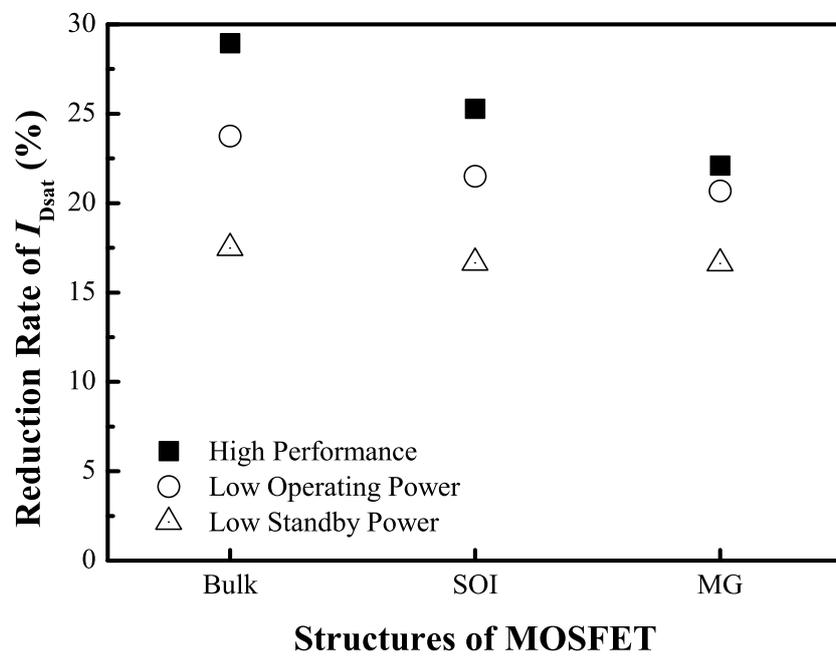


Fig. 1. Reduction rate of the saturation current influenced by the series resistance for bulk, SOI, and MG structure in HP, LOP, and LSTP technologies.

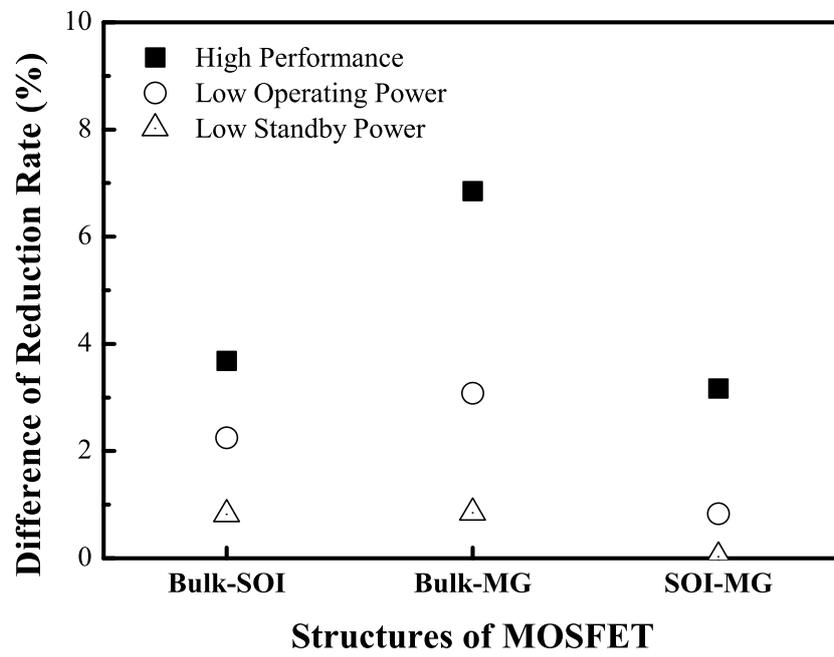


Fig. 2. Difference of the reduction rates between each structure in HP, LOP, and LSTP technologies.

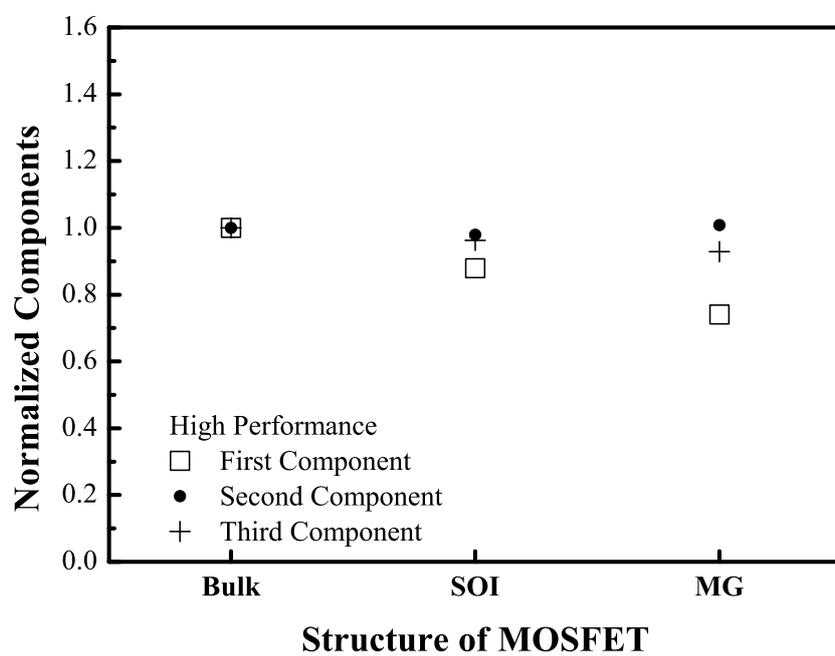


Fig. 3. Normalized expansion components of the saturation current including an effect of the series resistance in HP technology.

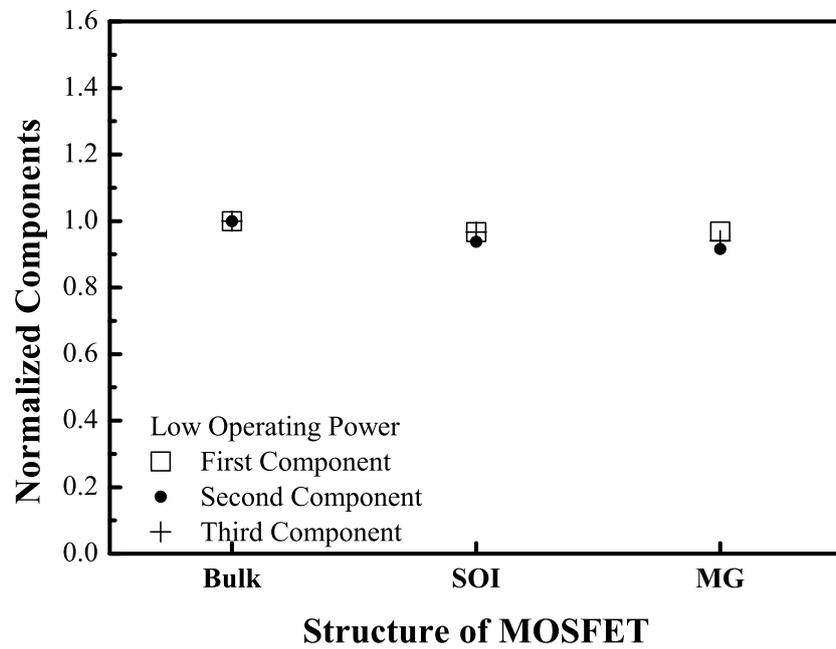


Fig. 4. Normalized expansion components of the saturation current including an effect of the series resistance in LOP technology.

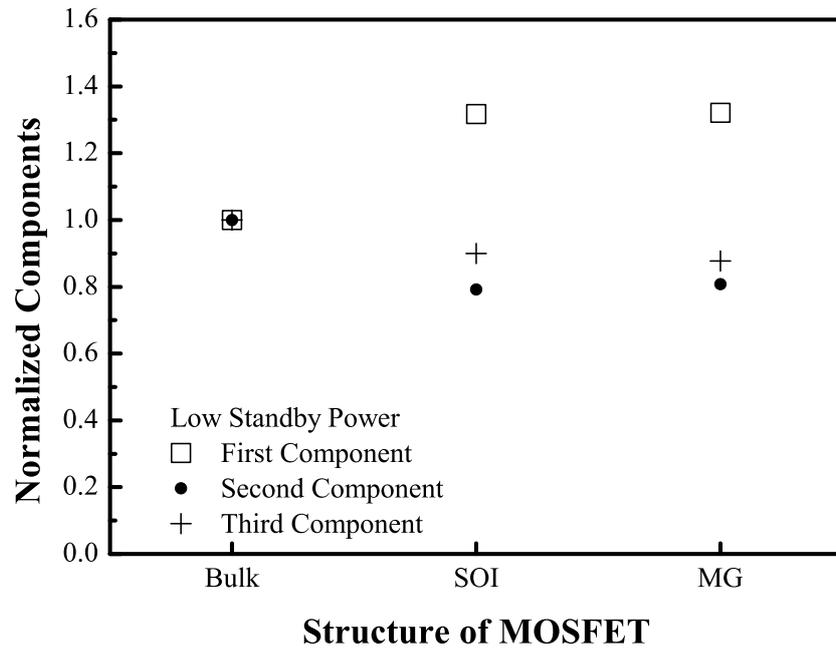


Fig. 5. Normalized expansion components of the saturation current including an effect of the series resistance in LSTP technology.