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Higher-Order Effect of Source–Drain Series Resistance on Saturation Drain Current in Sub-20 nm Metal–Oxide–Semiconductor Field-Effect Transistors

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The saturation drain current including a higher-order effect of series resistance is investigated in sub-20 nm metal–oxide–semiconductor field-effect transistors (MOSFETs). The reduction in current by the resistance is calculated using a derived analytical current model. As a result, the reduction rate increases from 15.8 to 24.0% as the gate length decreases from 32 to 18 nm. Ratios of the *N*th-order term to the sum of all absolute order terms are calculated. As the gate length decreases, the effect of higher-order terms becomes important for analyzing the effect of the series resistance. Normalized expansion components of the higher-order resistance-effect are compared with the reduction rate to determine the physical reasons for the reduction increase. We find that the ratio of the source resistance to the channel resistance is the dominant factor in device design and development for sub-20 nm MOSFETs. © 2012 The Japan Society of Applied Physics

1. Introduction

As the gate length shrinks into sub-20 nm regions, metal–oxide–semiconductor field-effect transistor (MOSFET) structures have been changed from simple planar bulk MOSFETs to fully depleted silicon-on-insulator (FD SOI) and multigate (MG) MOSFETs to control the short-channel effects.[1,2] In the traditional planar bulk MOSFETs, extended source and drain regions with shallow junction and higher doping concentrations have been used to prevent not only the short-channel effects but also the increase in sheet resistance.[3] The extended source and drain series resistance was modeled in an early study of Kim *et al.*[4,5] In the ultra-thin body and buried-oxide FD SOI and MG MOSFETs, the resistance of the extended regions becomes high with the thinning of body regions.[6–8] This problem was discussed by using an analytical resistance model based on understanding[8] of the resistance behavior in advanced MOSFETs.[9] Low series resistance is required for complementary metal oxide semiconductor (CMOS) technology to keep up with downscaling.[10–12] In device design and development for advanced MOSFETs, drain current reduction due to the series resistance becomes a critical issue as CMOS technologies are scaled deeper into the nanoscale regime.[8,9,13,14] As one of the solutions, improving the drain current has been researched by improving the carrier mobility and the gate oxide capacitance. The mobility in the channel region is improved by adopting strained body[15,16] and high-mobility materials.[17,18] Gate oxide capacitance is enhanced by using high-k materials[19] as the gate oxide.

In drain current modeling, analytical current models including the effect of the resistance have some advantages over circuit simulations. The analytical current models explicitly describe the relationships between physical parameters and MOSFET performance. Actually, an analytical current model that incorporated the impact of the series resistance was proposed to evaluate the capability of FD SOI for deep submicron technology.[20] A saturation current model was proposed by the 1st-order Taylor expansion for lightly doped drain (LDD) MOSFETs.[21,22] The improved model includes effects of self-heating and velocity overshoot by Roldán *et al.*[23] For 65 and 32 nm CMOS technologies, a simple semiempirical current model was researched by using several physical parameters.[24] However, no suitable analytical model for sub-20 nm MOSFETs has been researched. The model is necessary to analyze a higher-order effect of the series resistance.

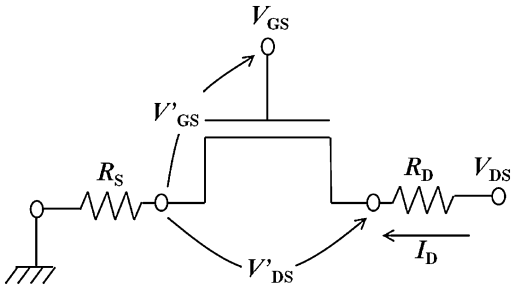

Fig. 1. Equivalent circuit including the intrinsic MOSFET and the series resistance.

In this work, we investigate a reduction in saturation drain current by the source and drain series resistance in the sub-20 nm technology node. An analytical saturation drain current model including an effect of higher-order terms of the series resistance is derived to improve the accuracy of the model and understand the physical meaning of the effect of higher-order terms. We describe model parameters of sub-20 nm MOSFETs and simulation methods. The reduction rate of the saturation drain current owing to the effect of the series resistance is calculated by using the derived analytical current model. An effect of higher-order terms of the saturation drain current and the relationships between physical parameters and the current reduction are discussed.

2. Analytical Saturation Drain Current Model

The effect of the series resistance is examined using an equivalent circuit in Fig. 1. The equivalent circuit consists of an intrinsic MOSFET, a source resistance, and a drain resistance as the series resistance. The drain current flows through the drain resistance, the channel, and the source resistance. At that time, a voltage drop occurs owing to the resistances. Therefore, internal voltages (V'_{GS}, V'_{DS}) are given by[25–27]

$$V'_{GS} = V_{GS} - I_D \cdot R_S, \quad (1)$$

$$V'_{DS} = V_{DS} - I_D \cdot (R_S + R_D), \quad (2)$$

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where R_S and R_D are the source and drain resistances per unit gate width, respectively. When the intrinsic MOSFET operates in the saturation region, the drain current equation is used as follows:[28,29)]

$$I_{Dsat0} = \frac{1}{2}\mu_{eff}C_{ox}\frac{(V'_{GS} - V_{th,on})^2 E_c}{(V'_{GS} - V_{th,on}) + L_{el}E_c(1+d)}, \quad (3)$$

$$E_c = 2\frac{v_{sat}}{\mu_{eff}}, \quad (4)$$

$$d = \frac{qN_{ch}\sqrt{2\varepsilon_s(2\varphi_F - V_b)/qN_{ch}}}{2C_{ox}(2\varphi_F - V_b)}, \quad (5)$$

where I_{Dsat0} is the saturation drain current per unit gate width when $R_S = R_D = 0\,\Omega{\cdot}\mu m$, μ_{eff} is the effective mobility, C_{ox} is the gate capacitance per unit area, $V_{th,on}$ is the threshold voltage at the on-state, E_c is the critical electric field, and L_{el} is the effective channel length. In eq. (4), the electron saturation velocity v_{sat} is assumed to be a constant ($= 1.1 \times 10^7$ cm/s), and the effective mobility is assumed as a function of effective field. The saturation current does not depend on the drain voltage because the effect of channel length modulation is assumed to be negligible. N_{ch} is the channel doping concentration, V_b is the applied substrate voltage, and φ_F is the quasi-Fermi potential in electron volts. From eq. (1), the saturation drain current is reduced by the gate-voltage drop ($I_{Dsat} \cdot R_S$) because of the source resistance. The saturation current equation solved by using the quadratic formula can be expressed as follows:

$$I_{Dsat} = \frac{-B - \sqrt{B^2 - 4AC}}{2A}, \quad (6)$$

$$A = \frac{1}{2}\mu_{eff}C_{ox}E_cR_S^2 + R_S, \quad (7)$$

$$B = -[V_{gt} + L_{el}E_c(1+d) + \mu_{eff}C_{ox}E_cR_SV_{gt}], \quad (8)$$

$$C = \frac{1}{2}\mu_{eff}C_{ox}E_cV_{gt}^2, \quad (9)$$

where V_{gt} is the overdrive voltage ($V_{GS} - V_{th,on}$) and I_{Dsat} is the saturation drain current per unit gate width including the effect of the series resistance. Equation (6) becomes complicated owing to the fact that it contains a root term. To analyze the physical meaning from the complicated form of I_{Dsat}, the Taylor expansion is used. I_{Dsat} including the higher-order terms of R_S can be rewritten as follows:

$$I_{Dsat} = I_{Dsat0}[1 + a_1R_S + a_2R_S^2 + a_3R_S^3 + a_4R_S^4 + O(R_S^5)], \quad (10)$$

$$a_1 = I_{Dsat0}\left(\frac{\alpha - 2}{V_{gt}}\right), \quad (11)$$

$$a_2 = I_{Dsat0}^2\left(\frac{2\alpha^2 - 6\alpha + 5}{V_{gt}^2}\right), \quad (12)$$

$$a_3 = I_{Dsat0}^3\left(\frac{5\alpha^3 - 20\alpha^2 + 28\alpha - 14}{V_{gt}^3}\right), \quad (13)$$

$$a_4 = I_{Dsat0}^4\left(\frac{14\alpha^4 - 70\alpha^3 + 135\alpha^2 - 120\alpha + 42}{V_{gt}^4}\right), \quad (14)$$

$$\alpha = \frac{V_{gt}}{V_{gt} + L_{el}E_c(1+d)}. \quad (15)$$

Equation (10) is the 4th-order approximated analytical current model. A 1st-order approximation of eq. (6) is identical to the semiempirical saturation drain current model equation.[22)] Each term of eq. (10) can be divided into three components by using a channel resistance ($R_{ch} = V_{dd}/I_{Dsat0}$) as follows:

$$a_1R_S = \left(\frac{R_S}{R_{ch}}\right)\cdot\left(\frac{V_{dd}}{V_{gt}}\right)\cdot(\alpha - 2), \quad (16)$$

$$a_2R_S^2 = \left(\frac{R_S}{R_{ch}}\right)^2\cdot\left(\frac{V_{dd}}{V_{gt}}\right)^2\cdot(2\alpha^2 - 6\alpha + 5), \quad (17)$$

$$a_3R_S^3 = \left(\frac{R_S}{R_{ch}}\right)^3\cdot\left(\frac{V_{dd}}{V_{gt}}\right)^3\cdot(5\alpha^3 - 20\alpha^2 + 28\alpha - 14), \quad (18)$$

$$a_4R_S^4 = \left(\frac{R_S}{R_{ch}}\right)^4\cdot\left(\frac{V_{dd}}{V_{gt}}\right)^4\cdot(14\alpha^4 - 70\alpha^3 + 135\alpha^2 - 120\alpha + 42). \quad (19)$$

We investigate the physical meaning of the components. The first components are ratios of the source resistance to the channel resistance. The second components are ratios of the supply voltage to the overdrive voltage. The third components are functions of V_{gt}, L_{el}, E_c, and d. As the degrees of terms increase, the degrees of the first and second components increase. We can obtain the explicit forms of the saturation current model including the effect of the series resistance.

3. Simulation

To investigate the saturation drain current including the effect of the series resistance, the reduction rate of I_{Dsat} is calculated as a function of the gate length. The reduction rate of I_{Dsat} is defined as follows:

$$\frac{|I_{Dsat} - I_{Dsat0}|}{I_{Dsat0}}, \quad (20)$$

where I_{Dsat0} is the saturation drain current without the effect of the series resistance calculated using eq. (3) and the saturation drain current including the resistance effect I_{Dsat} is calculated using eq. (6). Values of the parameters used in the simulated devices are shown in Table I. L_g and V_{dd} are chosen from the International Technology Roadmap for Semiconductors (ITRS) 2007.[30)] ITRS publishes annual reports focusing on various technologies, such as high-performance (HP) technology, low-standby-power (LSTP) technology, and low-operating-power (LOP) technology in the logical device technology. The supply voltages are 1.1, 1.0, and 0.8 V in HP, LSTP, and LOP technologies, respectively. In the LOP technology, the focus is on reduc-

Table I. Values of the parameters used in the simulated devices.

L_g	(nm)	32	28	25	22	20	18
L_{el}	(nm)	21.6	19.2	17.5	16.4	15.1	13.4
R_S	($\Omega{\cdot}\mu$m)	95	95	95	95	95	95
C_{ox}	(fF/μm)	18.8	23.9	25.9	27.9	30.6	30.8
μ_{eff}	($cm^2\,V^{-1}\,s^{-1}$)	491	581	557	607	585	582
E_c	(MV/cm)	4.48	3.79	3.94	3.62	3.76	3.78
V_{dd}	(V)	0.8	0.8	0.8	0.7	0.7	0.7
$V_{th,on}$	(V)	0.294	0.296	0.289	0.259	0.246	0.249
V_{gt}	(V)	0.506	0.504	0.511	0.441	0.454	0.456
d		0.334	0.245	0.241	0.224	0.217	0.242

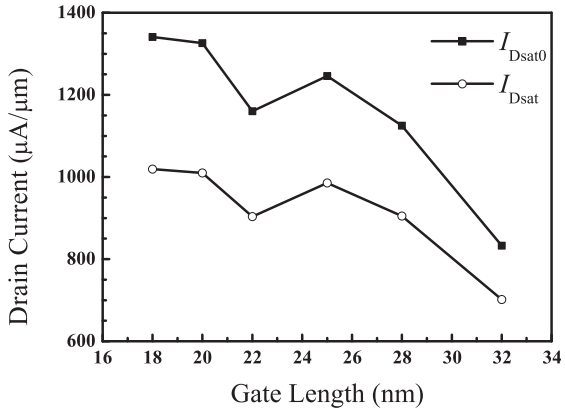

Fig. 2. Saturation drain current without the effect of the series resistance (squares) and saturation drain current including the effect (circles) as a function of the gate length.

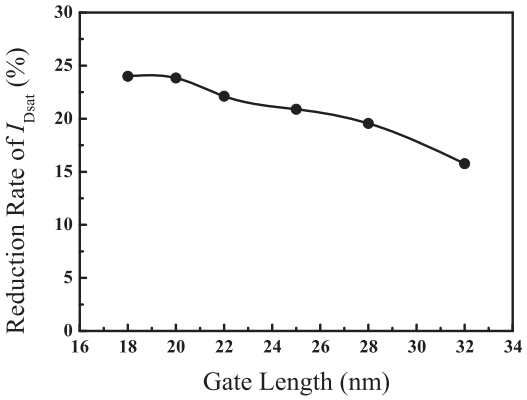

Fig. 3. Reduction rate by considering source–drain series resistance of I_{Dsat} as a function of the gate length.

ing operating power dissipation. To effectively reduce the power dissipation, the supply voltage is minimized. By decreasing the supply voltage, an increase in spreading resistance is induced.[31] The LOP technology is chosen in this simulation according to the minimum supply voltage. The source resistance per unit gate width is calculated under the assumption that R_S is one-half of R_{SD}. V_{gt} is given by

$$V_{gt} = V_{dd} - V_{th,on}, \tag{21}$$

$$V_{th,on} = V_{t,sat} + 0.03, \tag{22}$$

where $V_{th,on}$ is the saturated threshold voltage used for on-state current calculation. $V_{th,on}$ is modified by adding 0.03 V to a saturated threshold voltage $V_{t,sat}$.[32] The saturated threshold voltage $V_{t,sat}$ is used for the extrapolation of channel leakage current for $V_{GS} = 0$ and $V_{DS} = V_{dd}$. L_{el}, μ_{eff}, E_c, and d are calculated by using the MASTAR[32] results. The model for the assessment of CMOS technologies and roadmaps (MASTAR) is an analytical model used in ITRS. C_{ox} is identical to the electronic gate-oxide capacitance C_{ox_elec} in the result of the MASTAR.

4. Results

Figure 2 shows the results of I_{Dsat0} and I_{Dsat} calculated using eqs. (3) and (6) as a function of the gate length, respectively. Differences between I_{Dsat0} and I_{Dsat} increase from 131 to 332 μA/μm as the gate length decreases from 32 to 18 nm. As the gate length decreases, both saturation drain currents increase except for the 22 nm MOSFET. The drain current of the 22 nm MOSFET decreases since the supply voltage changes from 0.8 to 0.7 V.

Figure 3 shows the reduction rate of I_{Dsat} described by eq. (20) as a function of the gate length. The reduction rate increases from 15.8 to 24.0% as the gate length decreases from 32 to 18 nm. As the gate length decreases from 32 to 28 nm, the reduction rate increases from 15.8 to 19.6%. The largest gap of the rates between generations is between 32 and 28 nm generations. For 18 and 20 nm MOSFETs, the rates are 24.0 and 23.8%, respectively. The rates are almost constant below 20 nm. The gate voltage drop depends on I_{Dsat} and R_S, as shown by eq. (1). R_S is 95 Ω·μm in the 18–32 nm gate length range. Thus, the gate voltage drop and the reduction rate depend on I_{Dsat}. The reduction rate should also decrease for the 22 nm MOSFET. By comparing Fig. 2 with Fig. 3, the current drop does not depend on only I_{Dsat} and R_S.

Table II. Calculated results of absolute Nth-order terms ($a_N R_S^N$).

L_g	(nm)	32	28	25	22	20	18
$a_1 R_S$	($\times 10^{-1}$)	1.88	2.44	2.65	2.85	3.14	3.17
$a_2 R_S^2$	($\times 10^{-2}$)	3.64	6.07	7.14	8.26	10.0	10.2
$a_3 R_S^3$	($\times 10^{-2}$)	0.709	1.51	1.93	2.40	3.20	3.26
$a_4 R_S^4$	($\times 10^{-3}$)	1.39	3.78	5.22	6.99	10.2	10.5

To investigate the effect of higher-order terms, we calculated the absolute Nth-order terms using eqs. (16)–(19). The results of the Nth-order term are shown in Table II as a function of the gate length. The 1st- and 3rd-order terms have negative values. Using Table II, we calculated the ratio of the Nth-order term to the sum of all absolute order terms. The ratio is defined as

$$\frac{|a_N R_S^N|}{\sum_{i=1}^{4} |a_i R_S^i|}. \tag{23}$$

Figure 4 shows results of the ratio as a function of the gate length. The ratios of 1st-order terms decrease from 80.7 to 68.6% as the gate length decreases from 32 to 18 nm. The ratios of 2nd-order terms increase from 15.6 to 22.0% as the gate length decreases. The ratios of 3rd-order terms increase from 3.0 to 7.1% as the gate length decreases. In particular, for 2nd-order terms, the ratios are over 20% for 22 nm and below MOSFETs. As the gate length decreases, any effect of higher-order terms becomes important for analyzing the effect of the series resistance.

5. Discussion

To investigate the physical reasons underlying the reduction rate increase, expansion components of the Nth-order term are compared with the reduction rates. Table III shows the calculated expansion components of the Nth-order terms ($a_N R_S^N$). Figure 5 shows the expansion components of the 1st-order term and the reduction rates as a function of the gate length. The expansion components are normalized by that of the 32 nm MOSFET. The normalized first component

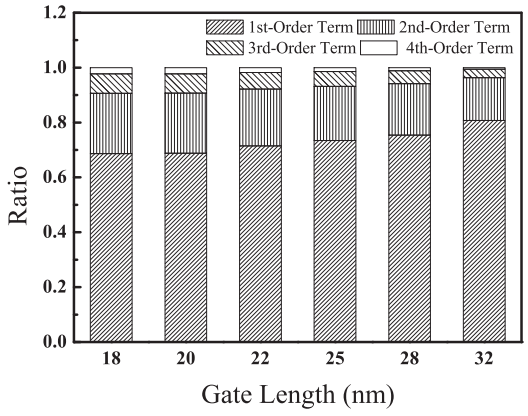

Fig. 4. Ratio of *N*th-order term to the sum of all absolute order terms as a function of the gate length.

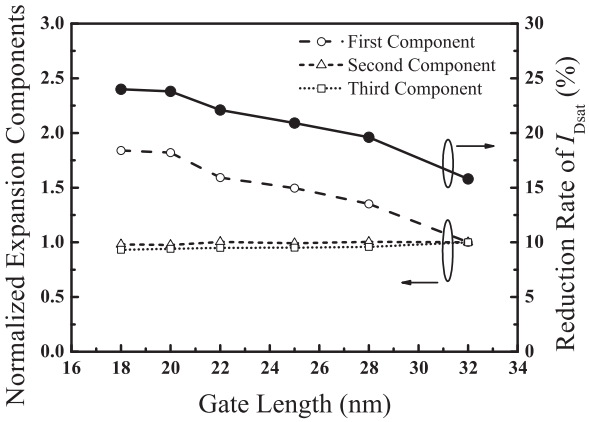

Fig. 5. Normalized expansion components (dashed lines) of 1st-order term and the reduction rates (solid line) of I_{Dsat} as a function of the gate length.

Table III. Calculated expansion components of *N*th-order terms ($a_N R_S^N$).

			L_g (nm)					
			32	28	25	22	20	18
	First component		0.989	1.34	1.48	1.57	1.80	1.82
$a_1 R_S$	Second component	($\times 10^{-1}$)	1.58	1.59	1.57	1.59	1.54	1.55
	Third component		1.20	1.15	1.14	1.14	1.13	1.12
	First component		0.978	1.78	2.19	2.48	3.24	3.31
$a_2 R_S^2$	Second component	($\times 10^{-2}$)	2.50	2.52	2.45	2.52	2.38	2.40
	Third component		1.49	1.35	1.33	1.32	1.30	1.28
	First component		0.968	2.38	3.24	3.90	5.83	6.03
$a_3 R_S^3$	Second component	($\times 10^{-3}$)	3.95	3.99	3.85	4.00	3.67	3.73
	Third component		1.86	1.59	1.55	1.54	1.50	1.45
	First component		0.957	3.19	4.79	6.14	10.5	11.0
$a_4 R_S^4$	Second component	($\times 10^{-4}$)	6.24	6.33	6.02	6.34	5.66	5.78
	Third component		2.32	1.87	1.81	1.79	1.72	1.66

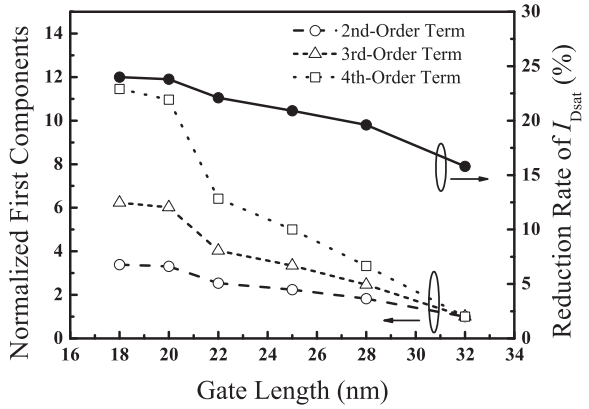

Fig. 6. Normalized first components (dashed lines) of 2nd-, 3rd-, and 4th-order terms and the reduction rate (solid line) of I_{Dsat} as a function of the gate length.

increases from 1 to 1.84 as the gate length decreases from 32 to 18 nm. As the gate length decreases from 32 to 28 nm, the first component increases from 1 to 1.35. For 18 and 20 nm MOSFETs, the first components are 1.84 and 1.82, respectively. The first components are almost constant below 20 nm. The increases in first components follows that in reduction rate. The second and third normalized components are about 1 at all gate lengths. There is no dependence on the gate length in the second and third components. The second component is the ratio of the supply voltage to the overdrive voltage. In other words, the supply voltage and the overdrive voltage are well scaled in these gate length regions. Below 32 nm MOSFETs, the first component is a dominant factor in the reduction in I_{Dsat}.

Figure 6 shows normalized first components of higher-order terms and the reduction rates as a function of the gate length. The first components increase as the gate length decreases. The increases in first components follow that in reduction rate, as in the case of the 1st-order terms. The second and third components are almost constant as a function of the gate length, as in the case of the 1st-order terms. The difference in first component between 32 and 18 nm increases from 0.84 to 2.39 for the 1st- and 2nd-order terms such an increase grows as the order increases. As the degree of the order term increases from 1 to 4, the values of the higher-order terms decrease since the unnormalized values of the first components decrease, as shown in Table III.

As shown in Fig. 5, the increases in first components follow that in reduction rate. The first component is the ratio of the source resistance to the channel resistance. Since it is assumed that the source resistance is constant in this work, the reduction in saturation drain current is inversely proportional to the channel resistance. The channel resistance is proportional to I_{Dsat0} owing to the fact that the supply voltages are 0.7 and 0.8 V. In eq. (3), I_{Dsat0} is a function of μ_{eff}, C_{ox}, V_{gt}, E_c, and L_{el}. The effect of $L_g \cdot E_c$ is insignificant, since $E_c \cdot L_{el}$ is sufficiently small to ignore. The overdrive voltage drops by 0.05 V below 22 nm MOSFETs. The gate capacitance and the effective mobility are the most effective parameters in the saturation drain current (I_{Dsat0}). As shown in Fig. 3, the largest gap of the rates between 32 and 28 nm generations can be explained by the fact that high-*k* dielectric materials are available as the gate insulator. Below 20 nm, problems of interface properties and compatibility of the high-*k* materials limit the decrease in equivalent oxide thickness (EOT) < 0.7 nm.

6. Conclusions

We investigate the saturation drain current reduction by the source and drain series resistance in sub-20 nm MOSFETs. The current reduction is calculated by using the derived analytical current model including the higher-order terms of the series resistance. As a result, the reduction rate increases from 15.8 to 24.0% as the gate length decreases from 32 to 18 nm. The ratios of 1st- and 2nd-order terms change from 80.7 to 68.6% and from 15.6 to 22.0% as the gate length decreases from 32 to 18 nm, respectively. We find that the higher order terms are important for analyzing the effect of the series resistance as the gate length decreases. From the analysis of the normalized expansion components, the increase in the ratio of the source resistance to the channel resistance leads to that in reduction rate. This implies that the resistance ratio of the source resistance to the channel resistance is a dominant factor in device design and development for sub-20 nm MOSFETs.

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