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Multicore Large-Scale Integration Lifetime Extension by Negative Bias Temperature Instability Recovery-Based Self-Healing

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We propose a multicore large-scale integration (LSI) lifetime extension method, which is based on negative bias temperature instability (NBTI) recovery-based self-healing and circuit parallelization. NBTI recovery is characterized by the recently proposed NBTI sensor with 400 ns measurement delay that measures the off-leak current of p-channel metal–oxide–semiconductor (PMOS) transistors. The circuit is fabricated in a commercial 65 nm complementary MOS (CMOS) technology. It is found that the recoverable component of the LSI performance characterized by the off-leak current remains almost constant after repeatedly adding NBTI stress. The NBTI stress corresponds to circuit operation for several years at room temperature and a nominal operating voltage. It is also found that the amount of NBTI recovery can be tuned by the relaxation time in a real application, and it follows log t from 400 ns to 3000 s. It is shown that for multicore LSI, by recovering one of the $n+1$ cores, the n-core LSI system does not stop and the lifetime can be extended by NBTI recovery. For the first time, transforming silicon area into LSI reliability is shown to be a promising and realistic concept for the ever-shrinking CMOS technology.

1. Introduction

Designing reliable systems has become more difficult in recent years. In addition to conventional problems such as transistor leakage, the degradation and variation of transistor performance have a severe impact on the dependability of very large scale integration (VLSI) systems.[1–3] Negative bias temperature instability (NBTI) is one of the strongest reliability concerns for complementary metal–oxide–semiconductor (CMOS) circuits.[4–15] A remarkable phenomenon regarding NBTI is that the degraded performance of a p-channel metal–oxide–semiconductor (PMOS) transistor recovers when the bias temperature stress applied to the gate oxide is removed or relaxed.[6] In this paper, we describe a multicore LSI lifetime extension method. In the following, it is shown that LSI lifetime is extended by combining NBTI recovery and circuit parallelization. It is a crucial step for this lifetime extension method to clarify the amount of NBTI recovery. Thus, we characterize NBTI using an NBTI sensor with a very short measurement delay (400 ns).[16] It is generally believed that the measurement delay is set as short as 1 μs to prevent NBTI recovery for a correct NBTI characterization.[7] It is also shown for the first time that transforming silicon area into LSI reliability is a promising and realistic concept for the ever-shrinking CMOS technology.[17]

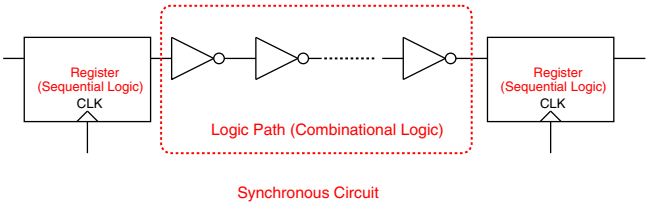

Fig. 1. (Color online) Typical synchronous circuit structure.

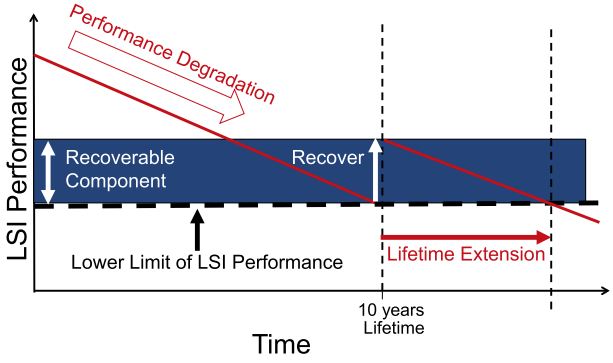

Fig. 2. (Color online) Degraded LSI performance can be recovered by NBTI recovery that leads to LSI lifetime extension.

2. Lifetime Extension by NBTI Recovery

Figure 1 shows a typical synchronous circuit structure where a logic path exists between two registers. The impact of the reliability of transistors that construct the synchronous circuit has increased in recent years. NBTI is one of the major concerns for the recent transistor reliability that is related to a physical property of a very thin gate oxide insulator. When transistors degrade owing to NBTI, the propagation delay of combinational logic increases. The correct operation of a register may not be guaranteed. Furthermore, the timing of registers that is generated by a clock tree may be skewed. As a result, owing to NBTI degradation, the circuit does not operate correctly or does not reach the lower limit of LSI performance. Figure 2 shows that LSI performance degrades with time and finally reaches its lifetime, for example, 10 years, which is defined by the lower limit of LSI performance. If LSI performance is recovered by NBTI recovery, its lifetime can be further extended, as shown in Fig. 2. As shown in §4, NBTI degradation under normal operating conditions is a gradual process, whereas NBTI recovery is a fast process. Thus, the recovery time is very short in Fig. 2. As a result, it is a crucial step for this lifetime extension method with NBTI recovery to clarify the amount of the NBTI recoverable component shown in Fig. 2. The nature of the recoverable component is clarified with measurement results in §4.

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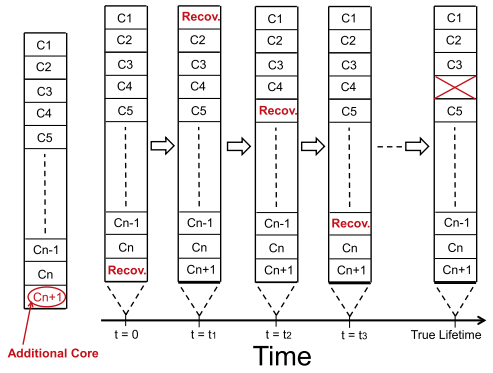

Fig. 3. (Color online) An example of $(n+1)$-core LSI ($C_1 - C_{n+1}$) operation is shown. Shortly before C_1 reaches its lifetime at $t = t_1$, C_1 becomes the recovery mode, and C_{n+1} becomes the active mode. By recovering one of the $n+1$ cores, the n-core LSI system does not stop and the lifetime can be extended by NBTI recovery.

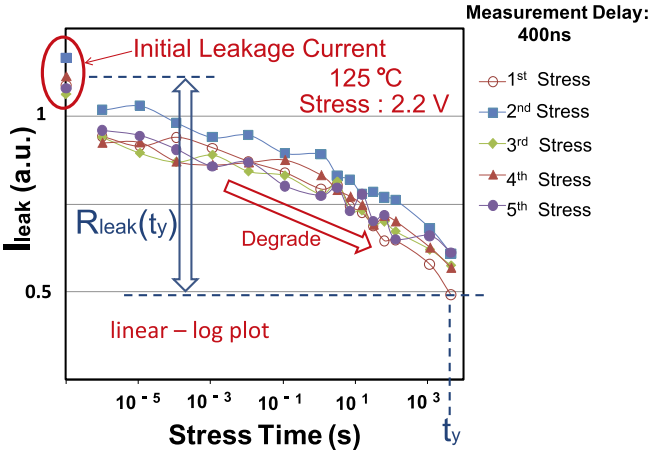

Fig. 4. (Color online) The off-leak current decreases with stress time compared with its initial value. The recoverable component shown in Fig. 1 measured using the off-leak current remains almost constant after repeatedly adding NBTI stress. The amount of the recoverable component is denoted by $R_{\mathrm{leak}}(t_y)$ for the stress time t_y.

3. Multicore LSI Lifetime Extension

The recent scaling of the CMOS device leads to circuit parallelization or multicore architecture in many applications.[18] Conventionally, yield is improved, power is decreased, and the hot spot on a die is decreased by circuit parallelization. For example, it is described that with the continuing trend of the denser technology through scaling, a new degree of freedom in architectural design has been made possible, in which silicon area can be traded off against power consumption.[19]

In this paper, we describe for the first time that transforming silicon area into LSI reliability is a promising and realistic concept for the ever-shrinking CMOS technology. Figure 3 shows the $(n+1)$-core LSI ($C_1 - C_{n+1}$). It is a homogeneous $(n+1)$-core LSI, and one core is always set to the sleep mode (or NBTI recovery mode). It is assumed that each core reaches its lifetime at a different time because of the process variation and different workload. When one core reaches its lifetime faster than any other cores, this core is set to the sleep mode instead of the previously recovered core, and the previously recovered core is set to the active mode. For example, shortly before C_1 reaches its lifetime at $t = t_1$, C_1 becomes the recovery mode, and C_{n+1} becomes the active mode. Thus, this LSI keeps n-core circuits active. As a result, by recovering one of the $n+1$ cores, the n-core LSI system does not stop and the lifetime can be extended to the "true lifetime" in Fig. 3 by NBTI recovery [originally, the lifetime is only t_1 for n-core ($C_1 - C_n$) LSI]. The recovery time is at most 1 h, as shown in §4. Furthermore, both C_1 and C_{n+1} operate under the same workload for a short time (around $t = t_1$) so as not to stop LSI operation when cores are exchanged.

4. NBTI Characterization Results

Quantitatively clarifying the amount of the recoverable component shown in Fig. 2 is a crucial step for lifetime extension. Recently, we have proposed an NBTI sensor that can characterize NBTI with 400 ns measurement delay.[16] NBTI is characterized by the off-leak current of PMOS transistors. Because this circuit contains 2160 PMOS transistors under NBTI stress, an averaged nature of NBTI is obtained. This circuit was fabricated in a commercial 65 nm CMOS technology. In this section, NBTI degradation and recovery measurement results obtained with this circuit are described. Figure 4 shows that the off-leak current decreases with stress time compared with its initial value that is also plotted in the same figure. The biases of 2160 PMOS transistors during the stress phase are $V_{\mathrm{gs}} = -2.2\,\mathrm{V}$, $V_{\mathrm{ds}} = 0\,\mathrm{V}$, and $V_{\mathrm{sub}} = V_{\mathrm{s}}$, and the biases during the measurement phase are $V_{\mathrm{gs}} = 0\,\mathrm{V}$, $V_{\mathrm{ds}} = -2.2\,\mathrm{V}$, and $V_{\mathrm{sub}} = V_{\mathrm{s}}$. The stress temperature is 125 °C. The NBTI degradation rate of a one-year order nominal operating condition generally roughly corresponds to the order of 1%. When PMOS is stressed at $V_{\mathrm{gs}} = -2.2\,\mathrm{V}$ and 125 °C as in Fig. 4, the stress time of 2000 s generally roughly corresponds to one-year order circuit operation at room temperature and a nominal operating voltage. After adding this 2000 s NBTI stress to a DUT, the off-leak current decreases to about half of its fresh value. After sufficient recovery, the off-leak current of the same DUT is again measured, and it is found that the off-leak current almost recovers to its fresh value, as shown in Fig. 4. This DUT is further repeatedly stressed under the same stress condition, and it is found that the initial off-leak current always recovers to its fresh value, as shown in Fig. 4. This means that the recoverable component shown in Fig. 2 measured using the off-leak current remains almost constant after repeatedly adding NBTI stress. The amount of the recoverable component is denoted by $R_{\mathrm{leak}}(t_y)$ for the stress time t_y. In a real application, there may not be sufficient time to recover. Figure 5(b) shows that NBTI recovery clearly follows log t from 400 ns to 3000 s. This is because the time constants of positively charged defects are log-uniformly distributed in PMOS devices.[20] More details are described in ref. 16. By modeling the recovery behavior shown in Fig. 5(b), the amount of NBTI recovery can be tuned by the relaxation time in a real application. Figure 5(a) shows the NBTI degradation measurement result, and we can predict the degradation on the basis of the power law behavior. Figure 6 shows the proposed LSI lifetime extension method by utilizing the recoverable component measured as in Fig. 4. In Fig. 6, $R(t)$ is the recoverable component and $P(t)$

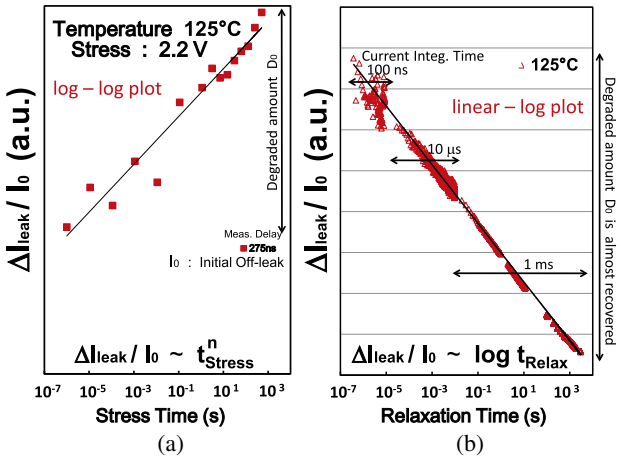

Fig. 5. (Color online) (a) The measurement result of NBTI degradation follows power law. (b) The measurement result of NBTI recovery follows $\log t$. In the case of nominal operation, the relaxation speed is much higher than the degradation speed. Owing to this asymmetrical nature of NBTI, lifetime extension by NBTI recovery is a very effective method.

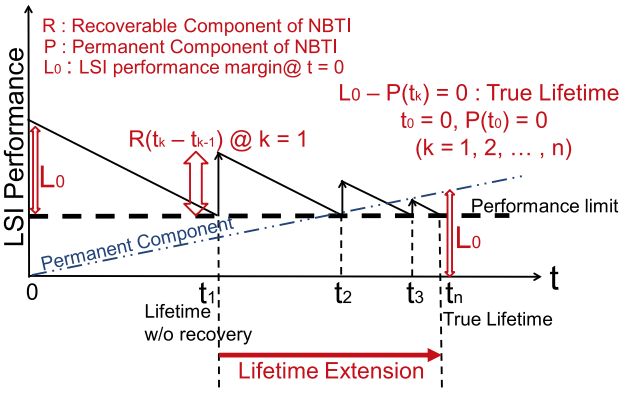

Fig. 6. (Color online) Concept of circuit operation to extend its lifetime. LSI performance can be repeatedly recovered until $L_0 = P(t)$.

is the permanent degradation of NBTI at the (stress) time t. L_0 is the LSI performance margin at $t = 0$. The permanent component $P(t)$ increases gradually with stress time t (conceptually shown in Fig. 6), and LSI performance can be recovered by $R(t_k - t_{k-1})$ at $t = t_k$. Shortly before LSI reaches its lifetime at $t = t_1$, LSI performance can be recovered by $R(t_1)$. LSI performance can be repeatedly recovered until $L_0 = P(t)$. The amount of $L_0 - P(t)$ gradually decreases because $P(t)$ gradually increases with time. When the power supply (VDD) decreases, the true lifetime can be further extended. NBTI degradation at a nominal operating voltage is a gradual process compared with the NBTI recovery that follows $\log t$ with a very fast component, as shown in Fig. 5(b). Owing to this asymmetrical nature of NBTI, lifetime extension by NBTI recovery is a very effective method. When process variation is considered, the performance margin defined in Fig. 6 decreases as the process becomes slow. Figure 5 shows that about 50% can be recovered for the recovery time of 1 ms. For the recovery time of 1 h, the degradation measured using the off-leak current is almost recovered. The degradation under nominal operation for 1 h can be ignored. As a result, more than two cores that reach their lifetime simultaneously can be detected at least 1 h before their lifetime. In the case of using one additional core for recovery, the time to set the core to the recovery mode must be carefully tuned so that another core does not reach its lifetime during the recovery mode. In the case of multicore LSI at a given workload, NBTI-recovery-based self-healing by the additional core works effectively when the degradation speed of the slow process corner core is reduced.

5. Conclusions

It is shown that LSI lifetime can be extended by combining NBTI recovery and circuit parallelization. NBTI recovery is characterized by the recently proposed NBTI sensor with 400 ns measurement delay that is fabricated in a commercial 65 nm CMOS technology. Measurement results show that the recoverable component measured using the off-leak current remains almost constant after repeatedly adding NBTI stress. It is also shown that the amount of NBTI recovery can be tuned by the relaxation time in a real application, and it follows $\log t$ from 400 ns to 3000 s. As a result, multicore LSI lifetime extension can be achieved. For the first time, transforming silicon area into LSI reliability is shown to be a promising and realistic concept for the ever-shrinking CMOS technology.

Acknowledgment

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