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A 65 nm Complementary Metal–Oxide–Semiconductor 400 ns Measurement Delay Negative-Bias-Temperature-Instability Recovery Sensor with Minimum Assist Circuit

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We propose a negative bias temperature instability (NBTI) recovery sensor with a 400 ns measurement delay. The measurement delay is about 30 ms when the leakage current of a small single transistor is measured by the conventional method. This sensor contains many unit cells. One unit cell includes 10 p-channel metal–oxide–semiconductor (PMOS) Device-under-tests (DUTs) and two assist n-channel metal–oxide–semiconductor (NMOS) devices. Parallelizing many unit cells can amplify the leakage current and the assist circuit can reduce the rush current to the ammeter, which keeps the measurement range of the ammeter constant during measurement. A short measurement delay is achieved by these two factors. It is confirmed that from 50 to 125 °C, NBTI recovery follows log t from 400 ns to 3000 s. By stressing and recovering thousands of PMOS transistors at the same time, we can observe that the time constants of positively charged defects, which are related to NBTI, are log-uniformly distributed in the PMOS devices. Also, this circuit has the highest fidelity to NBTI recovery measurement because off-leak current is used for NBTI recovery characterization and stress is not added during measurement.

1. Introduction

Designing reliable systems has become more difficult in recent years. Besides conventional problems such as transistor leakage, the degradation and variation of transistor performance have a severe impact on the dependability of very-large-scale integration (VLSI) systems.[1–3] In this paper, we deal with negative bias temperature instability (NBTI), which is one of the strongest reliability concerns for digital and analog complementary metal–oxide–semiconductor (CMOS) circuits.[4–14] In particular, we focus on a sensor circuit design that has high fidelity to NBTI recovery monitoring. In the following, first, we clarify the limitation of NBTI recovery measurement by a single p-channel metal–oxide–semiconductor (PMOS) transistor. Then, we describe an NBTI-recovery sensor with a minimum assist circuit achieving a 400 ns measurement delay.[18]

2. NBTI-Recovery Measurement by a Single PMOS

Figure 1 shows that the drain-to-source off-leak current (Leak) has a much higher (16 times higher) sensitivity than the saturation current (Ion) under the same amount of deviation in the threshold voltage ΔV_{th} according to a circuit-level simulation. Therefore, we use the off-leak current to characterize NBTI recovery with high resolution. Figure 2 shows the typical NBTI recovery measurement result obtained by the off-leak current of a single PMOS transistor. The transistor size used in Figs. 1 and 2 is identical and a small device is used. The bias during the stress phase is $V_{gs} = -2.0$ V, $V_{ds} = 0$ V, and $V_{sub} = V_s$, and the bias during the measurement phase is $V_{gs} = 0$ V, $V_{ds} = -1.2$ V, and $V_{sub} = V_s$. This measurement is done using an up-to-date semiconductor parameter analyzer[15] and 30 ms is the fastest initial measurement time in the case of off-leak current measurement. The current integration time is about 30 ms and this limits the measurement delay of 30 ms. A triaxial cable of 3 m length is used to connect the analyzer and the probe card.

We see clear step-like recovery behavior. Such step-like behavior is due to the individual recovery of positively charged defects.[11] Recovery starts immediately (generally, at least 1 μs) after stress is removed or relaxed.[6] Thus, the minimum measurement delay of 30 ms is too slow to measure NBTI recovery just after stress is released. As a result, there is an unknown region, as shown in Fig. 2, and

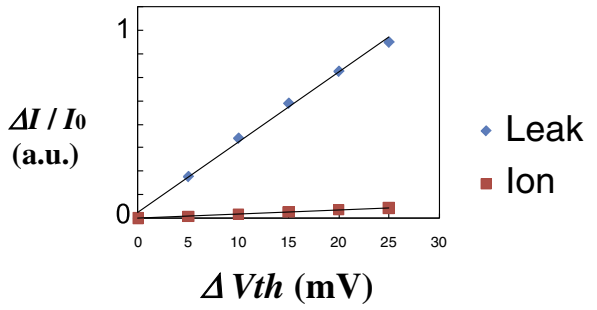

Fig. 1. (Color online) Drain to source off-leak current (Leak) has a much higher (16 times higher) sensitivity than the saturation current (Ion) under the same amount of deviation in the threshold voltage ΔV_{th} according to a circuit-level simulation.

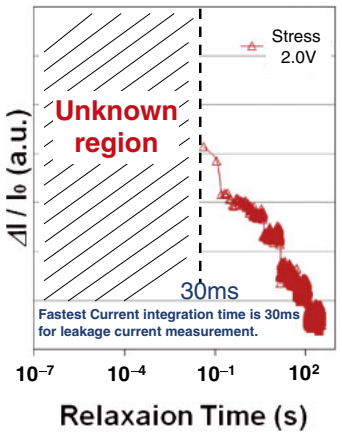

Fig. 2. (Color online) NBTI recovery measurement result by off-leak current of a single PMOS transistor for gate stress bias of 2.0 V. The fastest measurement delay is 30 ms.

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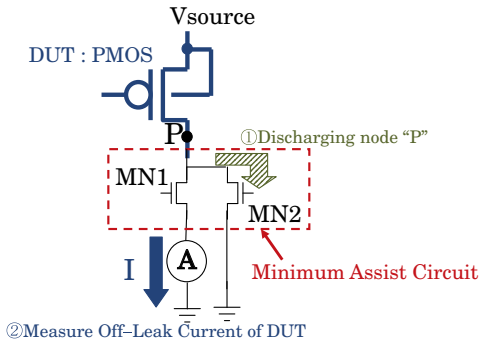

Fig. 3. (Color online) Concept of unit cell circuit design is shown. Unit cell circuit is constructed from a PMOS DUT and two assist NMOSes. Unit cell contains 10 DUTs in parallel in the real circuit.

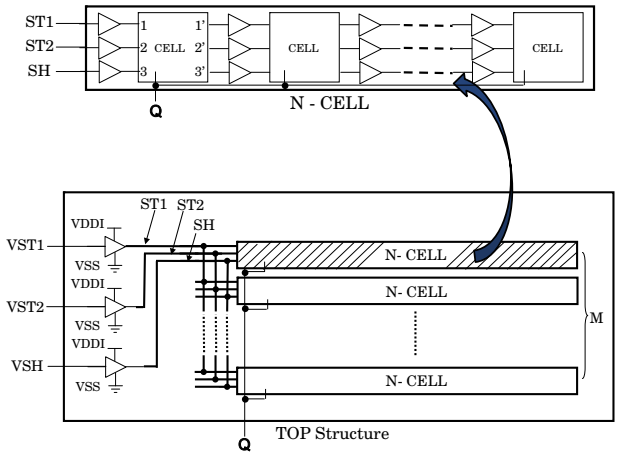

Fig. 4. (Color online) Entire measurement circuit ($M \times 10N$ DUTs).

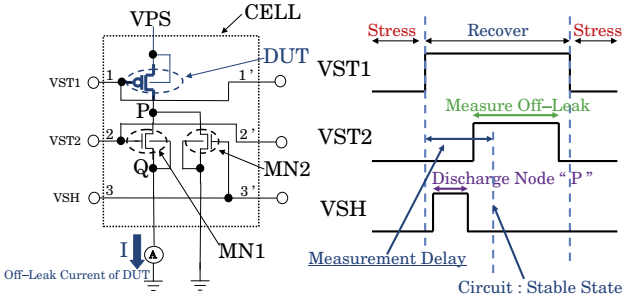

Fig. 5. (Color online) Timing chart of the proposed measurement circuit.

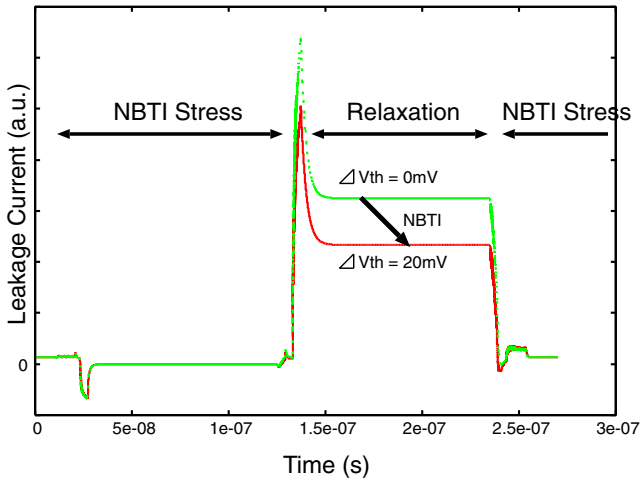

Fig. 6. (Color online) Simulation result of current at node Q in Fig. 5. $\Delta V_{th} = 0$ mV line means the fresh sample case and $\Delta V_{th} = 20$ mV line means the degraded case.

clarifying the recovery behavior in this region is very important for NBTI recovery modeling. In the next section, we propose an NBTI-recovery measurement circuit that can measure the recovery behavior with as short as a 400 ns delay.

3. NBTI Sensor by Minimum Assist Circuit

Parallelizing many PMOS devices can amplify the off-leak current while achieving high resolution. However, a large amount of charge is stored at the drain node of a DUT PMOS during the NBTI stress phase. As a result, the measurement range of the analyzer changes owing to this large injection current, which makes the measurement speed slower. To avoid this problem, we proposed a circuit that has two assist NMOS devices (MN1 and MN2 in Fig. 3), added to the PMOS DUT. Figure 3 shows the concept of the proposed circuit. This unit cell contains 10 DUTs in parallel and the transistor size of one DUT PMOS is identical to the case in Figs. 1 and 2. Immediately after the NBTI stress is removed, the charge at node P (drain of DUT) is discharged by MN2 for about 30 ns. Then, the off-leak current of the DUT is measured by opening MN1. These two NMOS devices achieves a 400 ns measurement delay as shown in the next section. Figure 4 shows the top structure of the proposed circuit. $M \times N$ cells in Fig. 3 are connected and the sum of the off-leak current of all these cells is measured. Because there are buffers between unit cells, the time when the leakage current begins to be measured in each cell is delayed slightly. As a result, the peak current that rushes to the ammeter immediately after MN1 is turned on becomes smaller and the measurement delay becomes faster. This enables a 400 ns measurement delay, which is much shorter than that in the single PMOS case (30 ms). Figure 5 shows the unit cell shown in Fig. 3 and the timing chart of the circuit of Fig. 4. The input voltage, VST1, determines whether the DUT is in a stress or recovery mode. Immediately after the DUT enters the recovery mode, VSH becomes "high" for a very short time (about 30 ns) to discharge node P in Fig. 5. Owing to this discharge, the large amount of charge at node P stored during stress mode is not injected to the ammeter, enabling the 400 ns measurement delay.

VST2 determines the PMOS leakage measurement duration. As shown in Fig. 5, the measurement delay of the circuit depends on the time until the circuit stays in a stable state after VST1 becomes "high". Figure 6 shows the simulation result of the current at node Q in Fig. 5. The line labeled as $\Delta V_{th} = 0$ mV corresponds to a fresh sample case and the line labeled as $\Delta V_{th} = 20$ mV represents a degraded case. Owing to the NBTI degradation, the off-leak current decreases, as shown in Fig. 6. Soon after the NBTI stress is removed, there appears a peak current, as shown in Fig. 6. Then, this current becomes stable and we can determine the

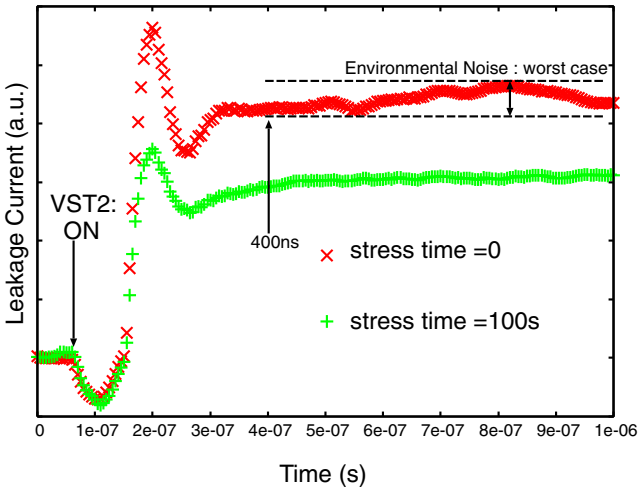

Fig. 7. (Color online) Measurement result of the current at node Q is shown. The measurement delay is 400 ns in the case of $M = 4$ and $N = 54$.

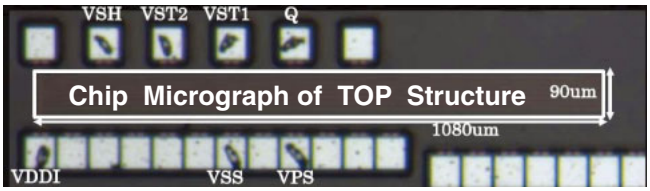

Fig. 8. (Color online) Chip micrograph fabricated in a 65 nm CMOS.

measurement delay (about 20 ns). Figure 7 shows the measurement result of the current at node Q. The current is measured using a fast current measurement unit.[16] The measurement delay is defined as 400 ns in the case of $M = 4$ and $N = 54$ as shown in the initial measurement curve (no degradation) of Fig. 7.

In the simulation result of Fig. 6, an ideal power source is used for the node VPS in Fig. 5. On the other hand, DC bias is provided by the SMU of the semiconductor parameter analyser.[15] This SMU needs a few μs time for the worst case to provide a stable output after the current starts to flow from this SMU. The ratio of this current to the current range of the SMU determines the time until the SMU output becomes stable. In our leakage current case (the number of DUTs is 2160), it is 400 ns and it limits the measurement delay to 400 ns. When the number of DUTs is increased from 2160 to 10000, the measurement delay also monotonically increases and it is a few μs for the case of 10000 DUTs. The measurement sequence in Fig. 5 can avoid channel hot carrier injection (HCI) because all the DUTs are in the off state during stress and measurement. Figure 8 shows a chip micrograph. The physical gate oxide thickness is 1.7 nm, W/L (drawn) of DUT is 11.75, and the minimum L is 50 nm (physical). It was fabricated in a commercial 65 nm CMOS technology.

4. Measurement Results of Proposed Circuit

Figure 9 shows the measurement results of NBTI recovery with 2160 PMOS DUTs ($M = 4$ and $N = 54$) after a 1000 s stress. The horizontal axis is the log scale and the vertical axis is the linear scale. The bias during the stress phase is

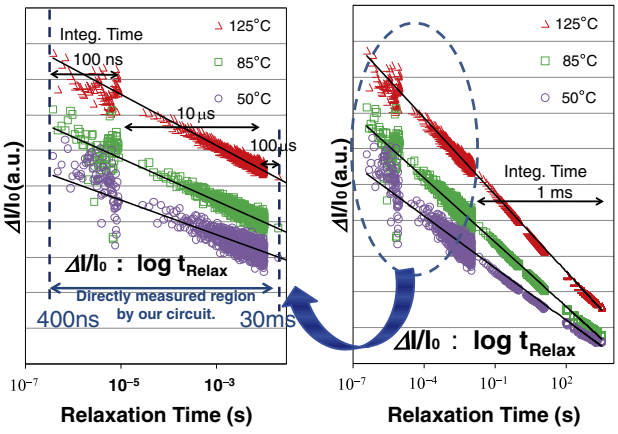

Fig. 9. (Color online) NBTI recovery measurement by the proposed circuit. NBTI recovery follows log t from 400 ns for all temperatures. Fitting lines (log t) to the experimental data are also shown.

$V_{gs} = -2.2$ V, $V_{ds} = 0$ V, and $V_{sub} = V_s$, and the bias during the measurement phase is $V_{gs} = 0$ V, $V_{ds} = -2.2$ V, and $V_{sub} = V_s$. The current integration time is also shown and the integration time is set to the optimal value corresponding to the relaxation time. When the current integration time is below 100 μs, the measurement points have some variation owing to environmental noise that is as large as the environmental noise shown in Fig. 7 for the worst case. After one sample is stressed at one temperature for 1000 s, it is recovered for 3000 s at the same temperature. The temperature is varied from 50 to 125 °C. The measurement delay as defined in Fig. 5 is 400 ns. Proposed circuit can measure the unknown region in Fig. 2. NBTI recovery clearly follows log t from 400 ns to 3000 s for all temperatures. This is because the time constants of positively charged defects are log-uniformly distributed in the PMOS devices.[17] What we observe in Fig. 9 is the averaged recovery behavior of 2160 PMOS transistors connected in parallel. We can observe such a log t behavior without measuring many single transistors individually. When a DUT is in the recovery mode, it is in the off state. Thus, there is no perturbation to the gate bias of DUTs. This enables high-fidelity NBTI recovery measurement, and other conventional methods do not have such a high fidelity.

5. Conclusions

We have proposed an NBTI-recovery sensor with a 400 ns measurement delay that includes many unit cells of ten PMOS DUTs and two assist NMOS devices. It is confirmed that NBTI recovery follows log t from 400 ns to 3000 s. By degrading and recovering thousands of PMOS transistors at the same time, we can observe that the time constants of positively charged defects, which are related to NBTI, are log-uniformly distributed in the PMOS devices. Also, this circuit has the highest fidelity to NBTI recovery measurement.

Acknowledgment

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1) S. Borkar: IEEE Micro **25** [6] (2005) 10.
2) M. Alam: Microelectron. Reliab. **48** (2008) 1114.
3) H. Onodera: IEDM Tech. Dig., 2008, p. 701.
4) D. K. Schroder and J. A. Babcock: J. Appl. Phys. **94** (2003) 1.
5) J. H. Sthathis and S. Zafar: Microelectron. Reliab. **46** (2006) 270.
6) H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder: Proc. IRPS, 2006, p. 448.
7) C. Shen, M. F. Li, C. E. Foo, T. Yang, D. M. Huang, A. Yap, G. S. Samudra, and Y. C. Yeo: IEDM Tech. Dig., 2006, p. 333.
8) Z. Q. Teo, D. S. Ang, and G. A. Du: Proc. IRPS, 2009, p. 1002.
9) T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel: Proc. IRPS, 2009, p. 33.
10) A. E. Islam, S. Mahapatra, S. Deora, V. D. Maheta, and M. A. Alam: IEDM Tech. Dig., 2009, p. 733.
11) H. Reisinger, T. Grasser, W. Gustin, and C. Schlunder: Proc. IRPS, 2010, p. 7.
12) T. Grasser, H. Reisinger, P. J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer: Proc. IRPS, 2010, p. 16.
13) B. Kaczer, T. Grasser, Ph. J. Roussel, J. Franco, R. Degraeve, L. A. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger: Proc. IRPS, 2010, p. 26.
14) V. Huard: Proc. IRPS, 2010, p. 33.
15) Agilent B1500A User's Guide.
16) Agilent B1530A User's Guide.
17) T. Aichinger, M. Nelhiebel, and T. Grasser: Proc. IRPS, 2009, p. 2.
18) T. Matsumoto, H. Makino, K. Kobayashi, and H. Onodera: Ext. Abstr. Solid State Devices and Materials, 2010, p. 806.