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PAPER Special Section on Low-Power and High-Speed Chips

A Perpetuum Mobile 32bit CPU on 65nm SOTB CMOS Technology with Reverse-Body-Bias Assisted Sleep Mode

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SUMMARY A 32bit CPU, which can operate more than 15 years with 220mAH Li battery, or eternally operate with an energy harvester of in-door light is presented. The CPU was fabricated by using 65nm SOTB CMOS technology (Silicon on Thin Buried oxide) where gate length is 60nm and BOX layer thickness is 10nm. The threshold voltage was designed to be as low as 0.19V so that the CPU operates at over threshold region, even at lower supply voltages down to 0.22V. Large reverse body bias up to −2.5V can be applied to bodies of SOTB devices without increasing gate induced drain leak current to reduce the sleep current of the CPU. It operated at 14MHz and 0.35V with the lowest energy of 13.4 pJ/cycle. The sleep current of 0.14μA at 0.35V with the body bias voltage of −2.5V was obtained. These characteristics are suitable for such new applications as energy harvesting sensor network systems, and long lasting wearable computers.

key words: *microprocessor, low power design*

1. Introduction

Perpetuum mobile computing is one of the key technologies to achieve trillion sensor universe, in which sensors along with super low power micro-controller unit (MCU) operate with harvesting energy or small coin batteries without maintenance. The super low power MCU should consume very tiny energy not only in operation mode but in sleep mode. When the average power of the MCU is less than the average harvesting power, the sensor nodes can operate eternally. This paper describes the first CPU which attains the conditions above by using the key technology called silicon on thin buried oxide (SOTB). As a step forward from the previous papers on the SOTB technology itself [1]–[3], [9], [10], this paper focuses on 32bit CPU implemented with the SOTB. The contribution of this paper is summarized as follows.

(1) This paper shows the first practical CPU implementation with the SOTB technology. Additional evaluation results, a comparison to other competitors and discussion for perpetuum mobile computing are added to the extended abstract paper [4] which is the basis of the paper.

(2) This paper also shows the chip with practical size of logic gates and memory cells. Although some specialized chips with practical size (an FPGA [11] and an accelerator [12]) with the SOTB were reported, no report has been done for common chips with logic gates and memory cells.

This paper is organized as follows. Section 2 describes the structure of 65nm SOTB devices for the fabrication of the CPU. Then in Sect. 3, we will introduce the structure and circuits of the CPU. Characteristics of the fabricated CPU are evaluated in Sect. 4 followed by the discussion in Sect. 5, and Sect. 6 concludes this paper.

2. SOTB Structure and Advantage for Low Power Micro Controller Unit (MCU)

The CPU was fabricated by using the 65nm SOTB CMOS technology.

The technology consists of two kinds of devices, one is SOTB devices whose gate length is 60nm for core logic and SRAM (Fig. 1 (a)), and the other is bulk devices (Fig. 1 (b)) whose gate length is 400nm for IO circuits. In the structures of 65nm SOTB as shown in Fig. 1 (a), the SOTB devices has an SOI layer thickness of 12 nm [1]. The specification of each region is summarized in Table 1. The BOX layer and gate oxide thicknesses are 10-and 2.0 nm, respectively. The body biases for NMOS "VBN" and PMOS "VBP" are applied from the Pwell and Nwell, respectively. Since Pwell and Nwell have neither source nor drain junctions due to dielectric isolation by the BOX layer, we can apply large reverse body bias up to −2.5V, which corresponds to the limitations on junctions between the Pwell and the Nwell. The original threshold voltage at body bias of 0V can be decreased to 0.20V for NMOS and 0.19V for PMOS to attain low voltage and fast operation of the CPU.

Thanks to the thin BOX layer, the body bias coefficients γ of the SOTB devices are so large [2]. We can apply large reverse body bias (RBB) to both NMOS and PMOS devices, as shown in the equation below.

$$\mathrm{VBB} = \mathrm{VBN} = \mathrm{VDD} - \mathrm{VBP}, \quad (1)$$

where VBN is body bias of NMOS and VBP is that of PMOS transistors. The value "γ" is defined in the following equation.

$$\gamma = \Delta\mathrm{Vth}/|\Delta\mathrm{VBB}| \quad (2)$$

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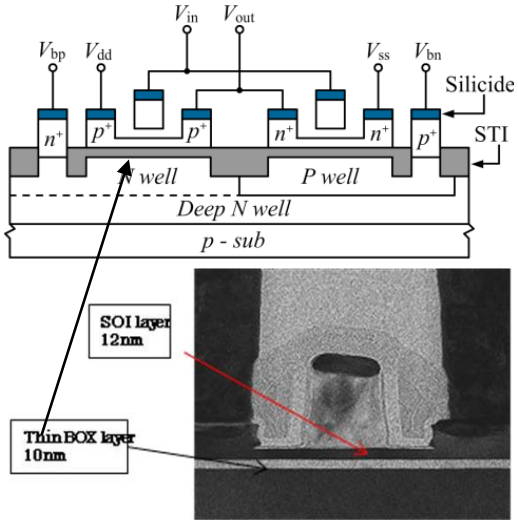
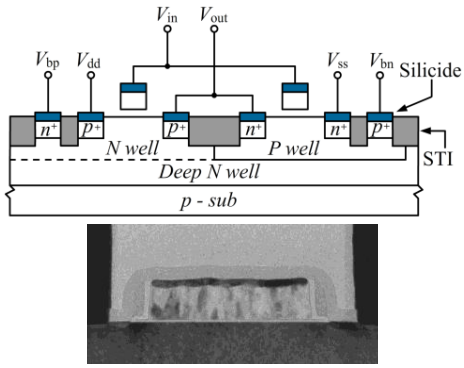


(a) Cross-sectional view of Core and SRAM regions of 65nm SOTB technology



(b) IO Cross-sectional view of Bulk Region

Fig. 1 Structures of devices and photomicrographs of the IO Region and Core and SRAM regions of 65nm SOTB technology.

Table 1 Specification of IO and Core Region.

IO Region(Bulk)	3.3V Lg=400nm, Tsion=7.5nm, Twin Well
Core Region (SOTB)	0.2-1.2V Lg=60nm, Tsion=2.0nm, TSOI=12nm, TBOX=10nm, Triple Well VTP/VTN(VBB=0)=0.20V/0.19V(Logic) =0.24V/0.22V(Memory)
Metal Layers	7 metal(5 fine, 2 Semiglobal), 1 AL

The value can be increased to 150 mV/V, which is almost three times higher than bulk devices at the same technology node.

Leakage which flows on an F.O 4 25-stage ring oscillator of inverters was measured as shown in Fig. 2 [3]. When we applied RBB, the leakage monotonically decreased without increasing GIDL (Gate Induced Drain Leakage) except for the shaded region. The GIDL current was smaller than the bulk devices of the same 65-nm technology. The GIDL current reduction for SOTB is easier than bulk because of its simple doping profile, that is, no halo implants is necessary [14]. The I_{ds}-V_{gs} characteristics of SOTB transistor at $V_{bb} = -2$ V (not shown) indicate that the subthreshold current dominates at $V_{ds} = 0.4$ V or lower whereas GIDL dominates the off-current at $V_{ds} = 1.2$ V. We can thus decrease the leakage down to 10pA at a supply voltage of 0.3V and VBB of −2V on the 100 -inverter ring oscillator.

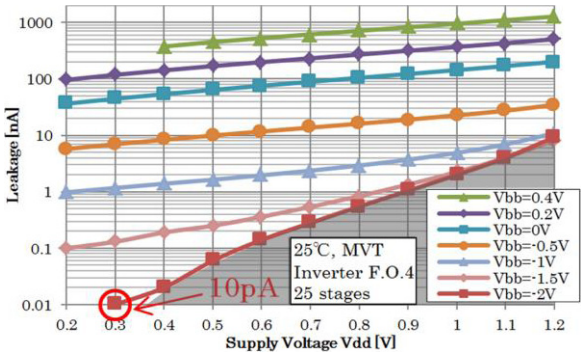


Fig. 2 Measured leakage of a ring oscillator on SOTB devices. The ring oscillator consists of 25-stage FO4 inverters. The shadow region shows the area where influence of GIDL current appears.

3. Structure and Circuit for 32 bit CPU

3.1 V850EStar CPU

A 32 bit microcontroller with a core compatible to the V850Estar [13] for signal processing, car electronics and digital servo motor control was implemented. It has RISC instruction set including operations for multiplies, saturation calculations, and bit manipulations. 5-stage standard in-order pipeline can execute most of instructions in a clock cycle. Here, instead of using the cache memory, local data memory was provided, and instructions are fetched from the memory outside the chip.

Structure of power lines, FF circuits, and power line operating waveforms of CPU are shown in Fig. 3. The power lines for CPU logic and SRAM were separated [4]. As for the CPU logic, VDD and VSS are power lines, and VBN and VBP are body biases for NMOS and PMOS, respectively. The VBB for logic was tuned to −0.5 V and that for SRAM was tuned to −1.0 V so as to attain minimum energy per cycle value. As for the SRAM memory array, supply voltage of SRAM, VDDM, was 0.1V higher than VDD to attain stable operation of SRAMs. In order to prevent leakage on the boundary between SRAM array and CPU logic, memory IO circuits that consist of NAND gates were introduced. Clocked CMOS input type DFF was introduced to attain low voltage operations of logic circuits.

We confirmed the data retention in SRAM fabricated by our SOTB technology under reverse body bias condition at V_{dd} less than 0.4 V [1]. The data stored in the DFF is thus not gone in standby mode when the large body bias is applied. This means that we need neither extra back up latch [5] nor retention FF [6] to restore the data during standby. As soon as the mode of the CPU changes from sleep to operation mode, the CPU can resume operation by using data stored in the FF latch. This is an advantage of the body bias techniques from the viewpoints of compatibility

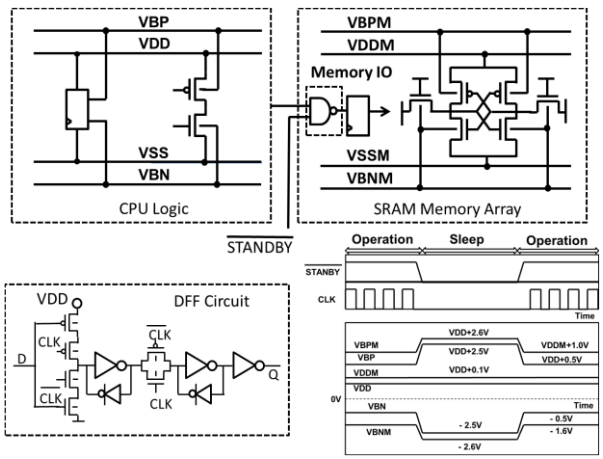


Fig. 3 Structure of power lines of CPU, circuit of DFF, and schematic operating waveforms of CPU.

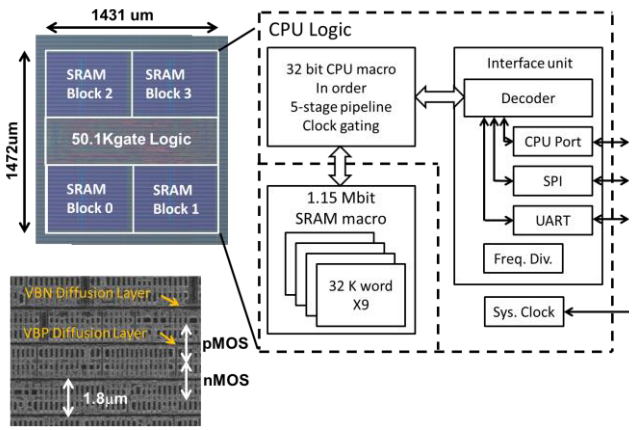


Fig. 4 CPU chip photomicrograph, CPU structure, and SEM photomicrograph of the region where primitive logic cells are paved.

with legacy design and area overhead.

A photomicrograph of the CPU core and the chip architecture are shown in Fig. 4. The CPU core consists of in-order 5-stage pipeline, and 4 blocks of 32Kword X 9 data memory. Instructions are fed from an instruction memory out of the chip through the IO circuits. The CPU core consists of 50.1K gate logic and 1.15 Mbit 6T SRAM arrays, and occupies 2.1 mm^2. The CPU chips were also fabricated by 65nm bulk-only CMOS using the same mask pattern to compare characteristics of CPUs for SOTB and Bulk devices.

Layout pattern of the region where primitive cells are located is also shown in Fig. 4. The cell height is 9 grids of 200nm M1 pitch, which corresponds to 1.8 μm height. We use silicided diffusion layers for VBN and VBP wires. Since the diffusion layers run horizontally without any gap, noise occurred in the primitive cells in operation mode can be reduced, thereby obtaining stable operations of the circuits, even applying RBB in operation mode.

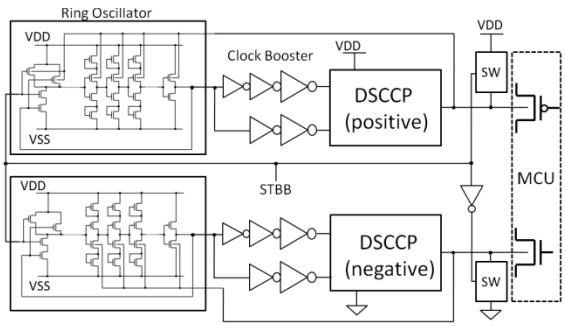


Fig. 5 Block diagram of the VBBGEN

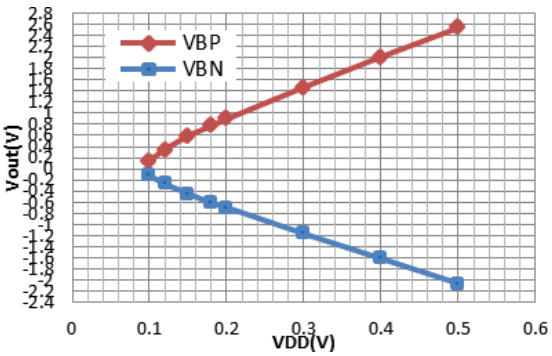


Fig. 6 Simulated output voltage of VBBGEN

3.2 Low Power Body Bias Generator

Low power body bias generator is necessary to reduce the standby current of the CPU, so that a large body bias voltage should be generated from the low supply voltages. Also the power consumption of the body bias generator itself must be low.

We have proposed body bias generator (VBBGEN), where body bias is generated by using Dynamic Substrate Controlled Charge Pump (DSCCP) [15]. The block diagram of the VBBGEN is shown in Fig. 5. The VBBGEN consists of Ring Oscillator, Clock Booster, and DSCCP. The outputs of the DSCCPs correspond to the body bias voltages (VBN and VBP) where VBN and VBP are connected to bodies of NMOS and PMOS in the Ring Oscillators so that the Ring Oscillators run and drive the DSCCP until the VBN and VBP reached to the predetermined voltages. As shown in Fig. 6, large |VBN| and VBP-VDD voltages of around 2.1V were obtained by the VBBGEN at a supply voltage of 0.5V by simulation.

Simulated current consumption of the VBBGEN was 361nA at a load current of 10 nA. Since load current of SOTB devices are extremely low due to the BOX insulation, the current consumption of the VBBGEN can be further reduced to sub 100 nA level.

3.3 Bias Control

Another issue is how to find optimal VDD, VDDM, VBB

and VBBM. There are a lot of researches to find the supply voltage and Vth for the smallest energy consumption [16]. In the CPU built with SOTB, *Vth* can be controlled by VBB/VBBM. By applying expressions in [17], we can find the optimal ones. However, from the viewpoint of practical usage of CPUs, a certain performance is needed. Thus, the optimal VDD, VDDM, VDD and VBBM must achieve the smallest energy consumption with a required clock frequency. Su and his colleague evaluated it for an accelerator using SOTB [12], and the same approach is useful to find such optimal parameters for CPUs.

The method of controlling both the optimum VBB and VBBM includes mainly these two points: (1) memory stability and (2) leakage/delay optimization.

Regarding the memory stability, we can control VBBM of both p-type (load) and n-type (access and driver) transistors independently against temperature and process variation. We demonstrated that the SRAM stability at 0.32 V is secured against the temperature variation by the back biasing [1].

Regarding the leakage/delay optimization, balancing the p- and n-type transistors by independent (VBP and VBN) back-bias voltage control is important. It is also essential for the SRAM stability. We demonstrated that the delay can be controlled over the temperature variation by the back biasing [18]. The leakage can be controlled because V_{th} can be controlled to be nearly constant over the temperature variation although a slight increase can be observed due to increasing the S factor at elevated temperatures.

4. Evaluation of the 32 bit CPU

Recently low power and low voltage operation of CPU is attained by lowering the supply voltage below threshold voltages of MOSFETs [7]. However, the CPU cannot operate fast due to sub threshold operation of logic circuits. The threshold voltages of CPU on SOTB can be decreased so that the CPU operates at over-threshold region, thereby operating at fast speed even at lower supply voltages.

Fmax of 32bit CPU core which was fabricated by bulk and SOTB processes are shown in Fig. 7. A simple test program to check the CPU functions including ADD instruction and the data memory read/write operations was carried out for the measurements. While instructions were supplied from the ROM outside the chip, data were stored in the data memory inside the chip. CPU on bulk CMOS operated down to 0.5V however the Fmax was only 1MHz. The maximum operating frequency of CPU on SOTB changed depending on VBB. At the optimized VBB condition, where VBB was −0.5V and VBBM was −1.0V, the CPU operated down to 0.22V and 1MHz. This is the lowest supply voltage of CPU ever reported [5]. The CPU on SOTB also operated at 14MHz at 0.35V and 46MHz at 0.5V. The CPU on SOTB operated at lower supply voltage than bulk by 0.28V, and operated faster by a factor of X46 at a supply voltage of 0.5V.

The power consumption of synchronous logic circuit is

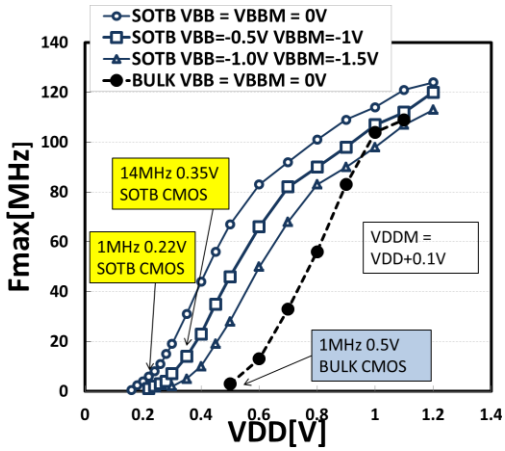


Fig. 7 Maximum operating frequency of CPUs by bulk and SOTB, where VBB is parameterized for SOTB.

expressed as Eq. (3).

$$P = P_{AC} + P_{DC} = 1/2AnCV^2f + nI_LV \quad (3)$$

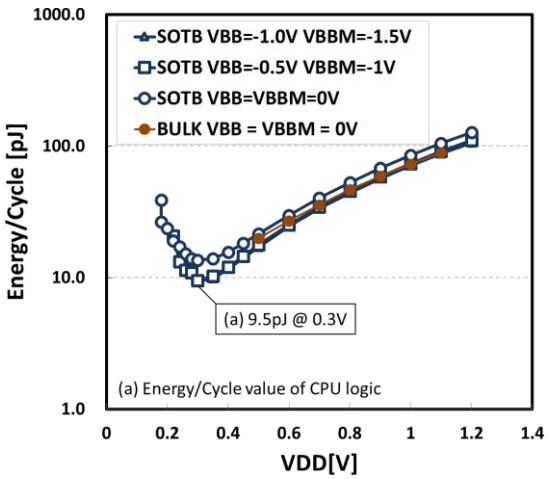
Where A is activity ratio of the circuit, n is number of logic gates, C is average capacitance of each gate, V is supply voltage, f is operating frequency, and I_L is leakage of each gate. When we divide the power by cycle frequency, we can obtain energy per cycle value as shown as Eq. (4)

$$E = E_{AC} + E_{DC} = 1/2AnCV^2 + nI_LV/f \quad (4)$$

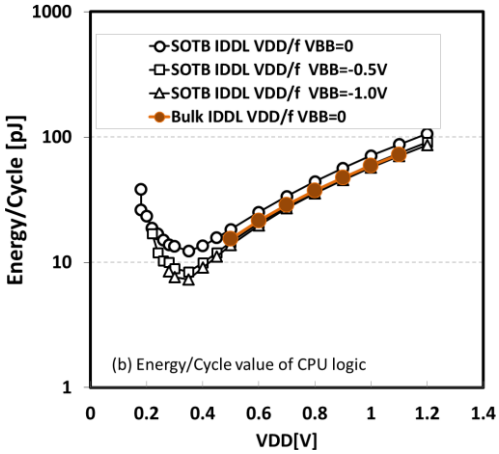
The energy per cycle value consists of AC energy and DC energy. AC energy can be reduced as supply voltage is reduced, however, the DC energy will increase because frequency reduces rapidly. The energy per cycle value normally has a minimum value called as Emin [19], [20].

Measured energy per cycle of the 32bit CPU is shown in Fig. 8. The body biases, VBN, VBP, VBNM, and VBPM were externally applied. The leakage currents of these terminals were measured and they were less than the resolution of the measurement instrument, which is less than 20 nA. The values do not affect the total energy per cycle values. Figure 8 (a) shows the energy/cycle value of CPU logic, while Fig. 8 (b) shows the leakage energy/cycle value of CPU logic. Here, cycle means clock cycle used in the CPU. Figure 8 (c) shows the energy/cycle value of SRAM array, while Fig. 8 (d) shows the leakage energy/cycle value of SRAM array. The total energy/cycle value is shown in Fig. 8 (e).

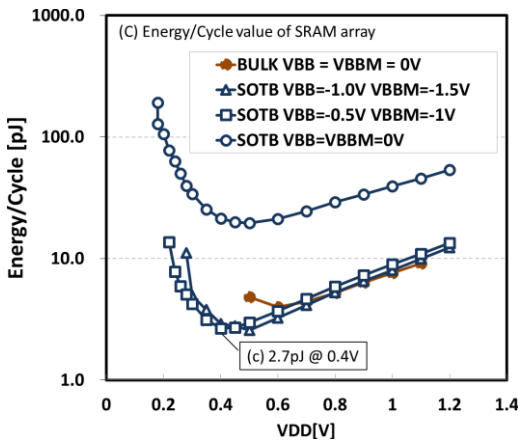
Since leakage increases exponentially as drain voltage increases as shown in Fig. 2, and original threshold voltage of SOTB is quite low, the leakage energy becomes dominant factor even at higher supply voltages. As shown in Fig. 8 (b) and Fig. 8 (d), Leakage-energy/cycle value shown in the 2nd factor in Eq. (4) exhibits minimum values, and it dominates the total energy/cycle values of the CPU. The supply voltages which give Emin appeared to be almost the same at different VBB conditions, and it comes from that leakage energy becomes dominant factors.



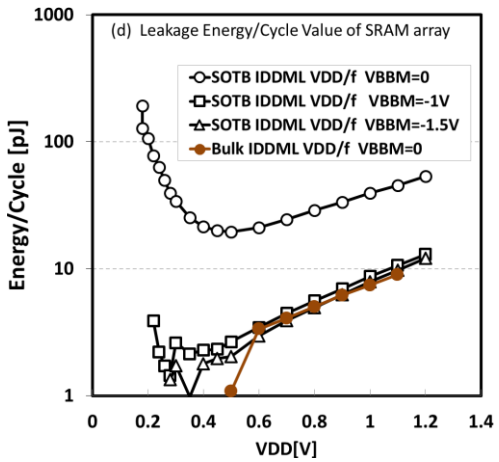
(a) Measured Energy per cycle values of CPU logic for Bulk devices and SOTB devices.



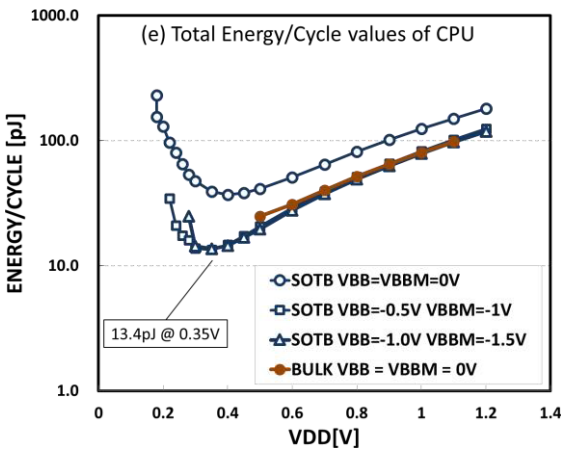
(b) Measured Leakage-energy per cycle values of CPU logic for Bulk devices and SOTB devices. Clock is stopped during the measurement.



(c) Measured Energy per cycle values of SRAM array for Bulk devices and SOTB devices.



(d) Measured Leakage-energy per cycle values of SRAM array for Bulk devices and SOTB devices. Clock is stopped during the measurement.

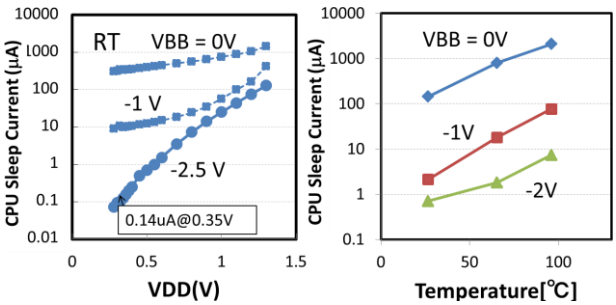


(e) Measured Total energy per cycle values of CPU for Bulk devices and SOTB devices.

Fig. 8 Measured Total energy per cycle valves.

The lowest Emin of 9.5pJ/cycle was obtained at a supply voltage of 0.3V and VBB of −1.0V as for the CPU logic in Fig. 8 (a).

As for the SRAM shown in Fig. 8 (d), DC energy was more dominant at VBB = 0V even at high supply voltages. Therefore larger body bias should be added to reduce energy/cycle value. The lowest value of 2.7pJ/cycle was obtained at VBBM of −1.5V and a supply voltage of 0.5V as



(a) vs. VDD (b) vs. Temperature

Fig. 9 Measured sleep current of CPU on SOTB

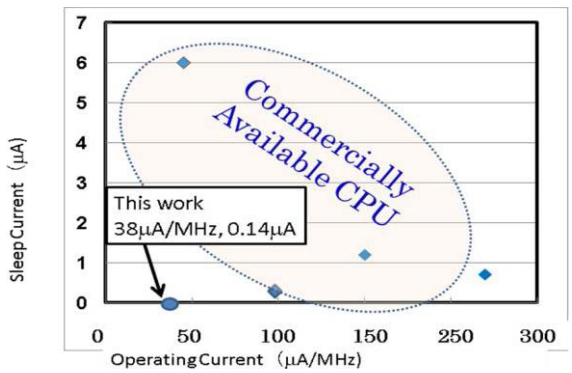


Fig. 10 Mapping for sleep current vs operating current

shown in Fig. 8 (c).

The Emin of CPU was obtained when VDD was 0.35V at VBB of −1.0V and VDDM was 0.45V at VBBM of −1.5V. It reached to 13.4pJ/cycle. Even when the CPU operated with Emin at 0.35V, it operated at high frequency of 14MHz, while CPU in the paper [7] operated at only 73KHz at the Emin condition. Therefore, the CPU on SOTB can achieve high performance with the smallest energy per cycle value.

Sleep current of the 32bit CPU under large reverse VBB is shown in Fig. 9 (a). We reduced the sleep current by more than three orders of magnitude when the VBB of −2.5V was applied. The sleep current of 0.14 μA was obtained at a supply voltage of 0.35V. The sleep current reduction was effective even when the temperature increased as shown in Fig. 9 (b). Therefore, we can prevent thermal runaway which is caused by positive feedback of leakage and temperature rise due to Joule heating.

The operating and sleep current of CPU are normally the trade-off on MCUs. Figure 10 shows a comparison of sleep current and operating current of commercially available MCU and the proposed CPU. Table 3 shows the specification of CPUs under comparison. The proposed CPU can reduce both sleep current and operating current simultaneously, and it can reach 38μA/MHz operating current and 0.14μA sleep current.

Table 2 Conditions for obtaining Perpetuum mobile CPU

Operation time/ Sleep Time	Average Current (μA)	220mAH Battery Life	Capable Harvest Power (cm-2)
100ms/30s	1.66	15 Year	Ambient Linght In door (10μW)
100ms/3s	13.1	1.9 Year	Thermal Energy (30μW)
100ms/300ms	127	72 day	Vibration (100μW)
Always in operation	380	24 day	Ambient light Out door (10000μW)

@ 380μA active current at 10MHz, 0.14μA sleep current
1%/Year battery self discharge

Table 3 Comparison with related work

	This work	Ref [8]	Ref[7]
Technology	65nm SOTB CMOS	32nm CMOS	0.18um CMOS
IP	32bit CPU, 50Kgate	IA-32 processor	32bit M3
VDD range	0.22V(Vmin) – 1.2V	0.28V – 1.2V	0.35V – 0.75V
SRAM	1.15 Mbit Data memory 6T High density [1] VDD + 0.1V	8KByte Code $ 8KByte Data $ 10T 0.55V operation	24Kbit (Retention) 10T
Energy/Cycle	13.4pJ 0.35V	170pJ 0.45V	28.9 pJ 0.4V
Frequency	1MHz 0.22V 4MHz 0.28V 14MHz 0.35V	3MHz 0.28V 915MHz 1.2V	73kHz 0.4V /1MHz 0.5V
Sleep Current, Leakage	0.14 μA	-	100pW/460pW

5. Discussion on Perpetuum Computing

We have estimated average current and battery life when the CPU is used with a 220 mAH battery (equivalent to CR2032 Li coin battery), and compatible energy harvesters as shown in Table 2. When the CPU becomes sleep mode for 30s after it operates for 100ms periodically on SOTB, the estimated life of the battery becomes 15 years. This life is longer than that uses commercially available CPUs at any operation-sleep time ratio. The CPU operates at average current of 1.66 μA, and it eternally continues to operate even with the ambient light energy harvesters that generate 10μA/cm^2 indoors. Therefore, the proposed CPU can realize the Perpetuum mobile computing.

In order to make sure the operation of the Perpetuum computing, we made a demonstration system as shown in Fig. 11. The system has a small Si solar cell of 3cm by 6cm for the supply of the chip including CPU, SRAMs, and IOs. The acceleration sensor detected the motion of a horse doll and the CPU could operate with the power from indoor light intensity. So the demo system proves that the CPU can operate eternally as long as indoor light ists.

6. Conclusions

A 32bit CPU which can operate eternally with an energy

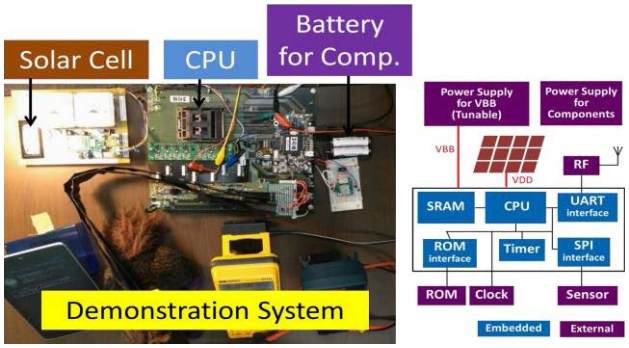


Fig. 11 A picture and block diagram of the demonstration system.

harvester was demonstrated. The CPU was fabricated by using 65nm SOTB CMOS technology. Large reverse body bias up to −2.5V can be applied to bodies of SOTB in sleep mode. It operated at 14MHz and 0.35V with the lowest energy of 13.4 pJ/cycle. The sleep current of 0.14μA at 0.35V with VBB of −2.5V was obtained. These characteristics are suitable for such new applications as energy harvesting sensor network systems, and long lasting wearable computers.

Acknowledgments

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