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Impact of Cell Distance and Well-contact Density on Neutron-induced Multiple Cell Upsets

Jun FURUTA[†a)], **Kazutoshi KOBAYASHI**[†], ***Members***, ***and*** **Hidetoshi ONODERA**[††], ***Fellow***

SUMMARY We measure neutron-induced Single Event Upsets (SEUs) and Multiple Cell Upsets (MCUs) on Flip-Flops (FFs) in a 65-nm bulk CMOS process in order to evaluate dependence of MCUs on cell distance and well-contact density using four different shift registers. Measurement results by accelerated tests show that MCU/SEU is up to 23.4% and it is exponentially decreased by the distance between latches on FFs. MCU rates can be drastically reduced by inserting well-contact arrays between FFs. The number of MCUs is reduced from 110 to 1 by inserting well-contact arrays under power and ground rails.

key words: *Neutron-induced Soft Error, Multiple Cell Upset (MCU), cell distance, well-contact density, Flip-Flop*

1. Introduction

Radiation-induced effects are significant issues for LSI reliability in space and terrestrial environments. In the ground level, α particles and neutrons can flip stored value on storage cells and it induces a temporal error on LSIs, which is called a soft error. When radiation hits on the LSI, its ionizing effect generates electron-hole pairs in p-well or n-well. Generated charge is collected to transistor's drain region and its output is temporally flipped. Soft error rates (SERs) per chip increase according to the process scaling since transistor density exponentially increases. Therefore, radiation hardened design is required to achieve high reliability in advanced technologies.

The Triple Modular Redundancy (TMR) FF is the fundamental circuit design for the reliability, which consists of three identical FFs and a majority-voting circuit. Output of the TMR FF is determined by majority voting of three FFs and it keeps correct even if a particle hits on one FF and flips its stored value. The TMR FF has strong radiation resilience while it takes huge area and power overheads. For less area and power penalty, various redundant FFs are proposed – for example, Dual Interlocked Storage CEll (DICE) [1], Built-In Soft Error Resilience (BISER) [2] and Hysteresis FF [3].

In 90–40 nm process, soft error resilience on radiation-hardened FFs are drastically reduced. P. Hazucha reported neutron-induced SERs on 90-nm DICE latches and they have more than 10x higher soft error resilience than non-redundant latch [4]. In contrast, S. Jagannathan reported that DICE-FF has only ~ 1.4x soft error resilience in 40-nm process due to multi-node charge collection [5]. Multi-node charge collection can flip output values of multiple nodes and cause simultaneous flips of stored values, which is called a multiple cell upset (MCU) or a multiple bit upset (MBU). Since MCU is multiple flips caused by a particle strike, the TMR FF and almost all radiation-hardened FFs are vulnerable to an MCU and their SERs highly depends on the MCU rate. It depends on cell distance and well-contact density [6], [7]. Cell distance is exponentially decreased by process scaling, the MCU rate on SRAMs is drastically increased [8]. Therefore, MCU-hardened layout methodology is also required for all redundant FFs to improve radiation hardness.

In this paper, we show measurement results of neutron-induced MCUs on D-FFs by using 4 different shift registers to estimate soft error rates on redundant-FFs and to measure the dependence of MCUs on the cell distance and well-contact density [9]. Test chips were fabricated in a 65-nm bulk CMOS process and neutron irradiation tests were carried out at Research Center for Nuclear Physics (RCNP). We discuss MCU/SEU dependency on the cell distance, the well-contact density and the technology scaling by experimental results on a 65-nm bulk process.

This paper is organized as follows. Section 3 explains the test circuit structure in detail. Section 4 shows our neutron-beam experimental setups in RCNP, followed by Section 5 which discusses experimental results. Section 6 concludes this paper.

2. Soft Error Mechanism

In the ground level, soft errors are caused by α particles emitted from package material and neutron generated in the atmosphere by cosmic ray [10]. When an α particle incidents on a silicon device, electron-hole pairs are generated by its ionizing effect along the particle track as shown in Fig. 1. Generated minority carriers, electrons in p-well are collected into the drain region of the nMOS transistor by funneling, drift and diffusion. The drain output can be flipped by collected electrons transiently. Its radiation effect is termed a single event effect (SEE). In contrast, neutrons do not generate electron-hole pairs directly. Their effects occur through nuclear collisions with Si atoms, which generates secondary particles. Then, secondary particles generate electron-hole pairs. When electron-hole pairs are generated in a sequential element, they may flip the stored value. It is

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[†]The authors are Graduate School of Science and Technology, Kyoto Institute of Technology, Japan.
[††]The author is Department of Communications and Computer Engineering, Kyoto University, Japan.
a) E-mail: furuta@kit.ac.jp
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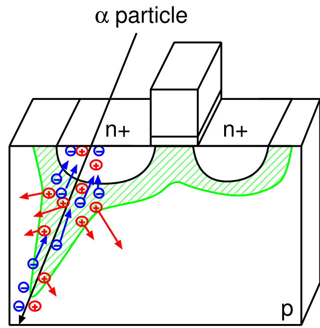

Fig. 1 Single event effect on a silicon device.

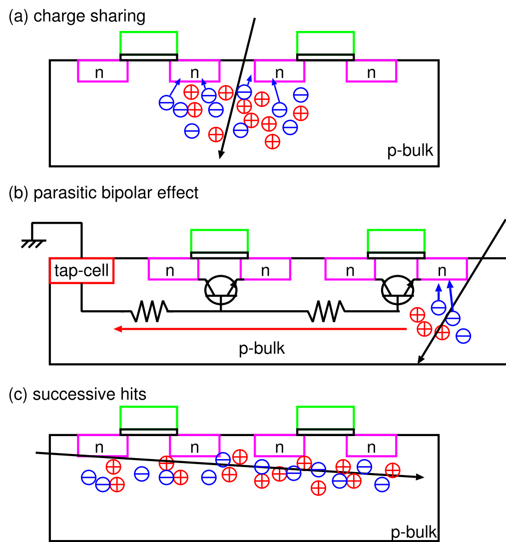

Fig. 2 Mechanisms of multiple errors.

called a single event upset (SEU). The SEU rate on silicon devices increases according to process scaling since gate capacitance of a transistor is reduced by process scaling and output is flipped more easily.

Radiation-induced multiple errors, however, are not caused by charge collection only. They are caused by several mechanisms – charge sharing, the parasitic bipolar effect and successive hits as shown in Fig. 2 [11]–[13]. Charge sharing denotes collection of charge by multiple transistors. The parasitic bipolar effect is induced by arising well-potential caused by radiation incidence, which turns on parasitic bipolar transistors. Therefore, it depends on the well-contact density and distance. Successive hits mentions that one particle penetrates multiple transistors. Successive hits depend on the angle of particle incidence. MCU rate are increased by process scaling in any mechanism because the cell distance is shorter in advanced technologies.

3. Test Chip Structure

We fabricated a test chip in 65-nm bulk CMOS process to measure soft error by the spallation neutron beam at RCNP. The purposes of the test chip are as follows.

- To estimate neutron-induced soft error rates on redundant FFs and compare them with SEU rates on non-redundant FFs.
- To evaluate cell-distance dependence of MCUs for effective layout design methods of redundant FFs.
- To evaluate dependence of MCUs on well-contact density (well-contact distance). If MCU rates strongly depend on it, MCUs are mainly caused by the parasitic bipolar effect. It is because parasitic bipolar transistors turn on by raising well-potential [12].

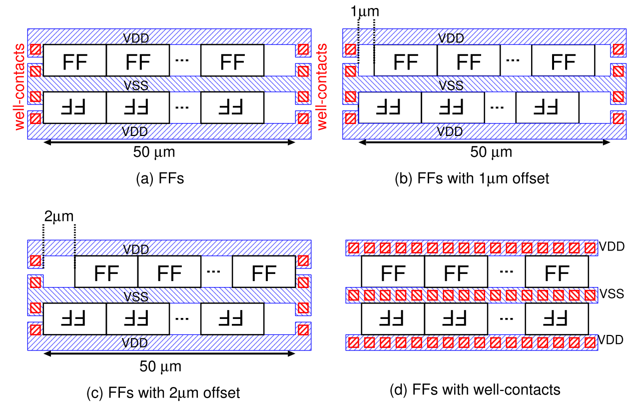

Fig. 3 Conceptual Layout structures of four different shift registers. Clock buffer chains are omitted in this figure.

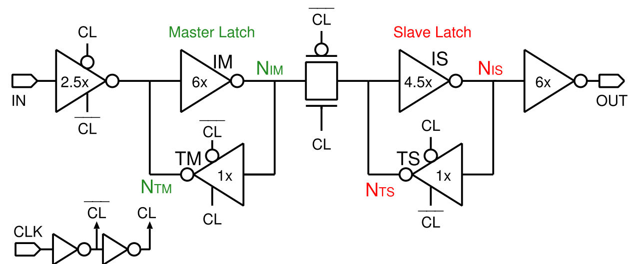

Fig. 4 Schematic diagram of implemented FFs. The values show normalizing drive strengths.

To estimate soft error rates on redundant-FFs, we implement four different types of shift registers as shown in Fig. 3. They are implemented with conventional non-redundant FFs. We assume that MCU rates on FFs are equivalent to the SEU rate on redundant FFs which consist of non-redundant FFs. All shift registers are constructed by FFs and clock buffer chains [14]. Implemented FFs have the same layout structure except well-contacts. Figure 4 shows the schematic diagram. The master and slave latches are constructed by inverters and tri-state inverters.

Shift registers (a)–(c) in Fig. 3 have $0\,\mu$m, $1\,\mu$m and $2\,\mu$m horizontal offsets between odd rows and even rows in order to measure MCU rates by changing the distance between latches in FFs. When the clock is "1", master latches are in the hold state. We can obtain 6 kinds of MCU rate simultaneously from observed MCU patterns as shown in Fig. 5. In addition, shift registers have different distances between slave latches and between master latches as shown in the upper left of Fig. 5. Therefore, we obtain 12 kinds of MCU rate with 0.5–4.6$\,\mu$m by alternating the clock signal.

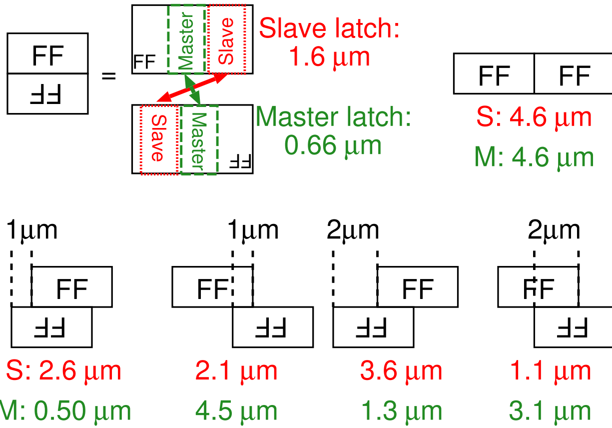

Fig. 5 Distance between master latches or salve latches on shift register (a)–(c) in Fig. 3.

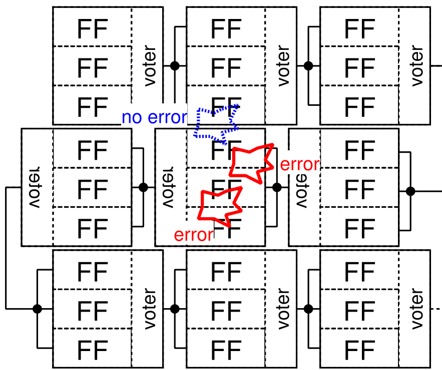

Fig. 6 MCU-induced soft errors on aligned TMR FFs.

We can measure distance-dependence of MCUs using these three simple shift registers.

Shift registers (a)–(c) have isolated well-contacts which are inserted every 50 μm (every 10 FFs). In contrast, the shift register of Fig. 3(d) has well-contact arrays under its power and ground rails. It has 60x higher well-contact density than the other shift registers (a)–(c). We obtain dependence of them on well-contact density by comparing MCU rates between the shift registers (a) and (d) which have same cell offsets. Each shift register is constructed by 10,000 FFs.

To estimate soft error rates on a TMR FF from measurement results of implemented shift registers, we suppose that a 10,000 bit shift register is constructed by TMR FFs and all FFs are aligned as shown in Fig. 6. When an MCU occurs on FFs which construct a TMR FF, it causes a soft error. In the shift register constructed by aligned TMR FFs, 2/3 of MCUs are caused on adjacent FFs in one TMR FF and 1/3 of MCUs are caused on adjacent FFs in two adjacent TMR FF as shown in Fig. 6. The soft error rate of the 10,000 bit TMR FFs constructed by 30,000 bit FFs is twice ($2/3 \times 3$) as high as MCU rate of 10,000 bit non-redundant FFs.

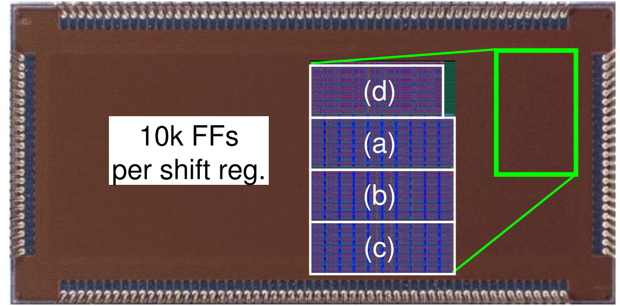

Fig. 7 Chip micrograph with floorplan.

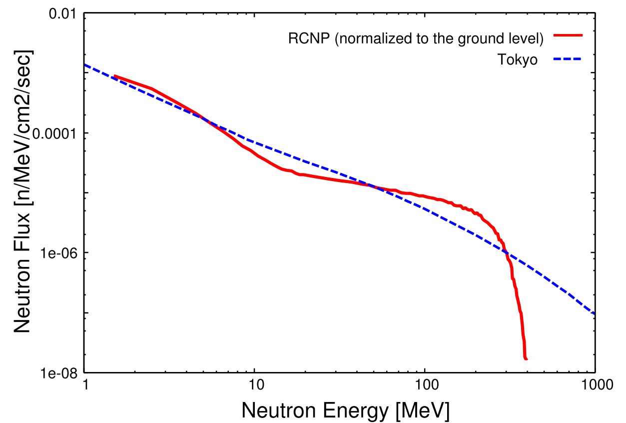

Fig. 8 Neutron spectrum at RCNP.

4. Experimental Setup

Figure 7 shows a test chip micrograph fabricated in a 65-nm bulk CMOS process. It has twin-well structure and its supply voltage is 1.2 V. Each shift register includes 10 k FFs. The total area of four shift registers is 0.5×0.8 mm^2 on a 2×4 mm^2 die.

Accelerated tests were carried out by spallation neutron irradiation at RCNP. Figure 8 shows the neutron beam spectrum compared with the terrestrial neutron spectrum at the ground level of Tokyo. The average acceleration factor is 3.8×10^8. In order to increase error counts, we measured 24 chips at the same time using stacked DUT boards. An engineering LSI tester is used to control DUTs and collect shifted error data.

All stored values of the shift registers were initialized to “ALL0” or “ALL1”. Therefore, SET pulses on clock buffer chains are negligible since they cannot flip stored values on FFs. During irradiation, clock signal is fixed to “1” or “0” to keep master latches or slave latches in FFs in the hold state. All stored values are retrieved every 5 min. The expected value of SEUs on FFs is less than 3 SEU/(chip $\cdot$ 5 min). Since each test chip has 40 k FFs, adjacent FFs are rarely flipped by 2 SEUs. Thus, when adjacent FFs are flipped simultaneously, we expect that these flips are caused by MCUs.

Table 1 The number of SEUs and MCUs by neutron irradiation when stored value is “ALL0” and clock signal is “1” (Master latches are in hold state).

Shift Register	Min. cell distance	# of SEU	# of MCU	MCU ratio [%]
(a) FFs	0.66 μm	617	110	17.8
(b) FFs w/1 μm	0.5 μm	631	148	23.4
(c) FFs w/2 μm	1.3 μm	654	91	13.9
(d) FFs w/well-con.	0.66 μm	498	1	0.2

Table 2 The number of SEU and MCU rates by neutron irradiation when stored value is “ALL0” and clock signal is “0” (Slave latches are in hold state).

Stored values	Shift Register	SEU rate [n/Mbit/h]	MCU rate [n/Mbit/h]
ALL0 (N_{TS} = 0)	(a)	60	0
	(b)	78	0
	(c)	79	0
	(d)	91	0
ALL1 (N_{TS} = 1)	(a)	254	15
	(b)	283	10
	(c)	259	33
	(d)	165	0

5. Experimental Results

In this section, we show experimental results by neutron irradiation. Note that the number of SEUs includes that of MCUs. MCU/SEU becomes 100% when all flips are MCUs.

Table 1 shows the number of SEUs and MCUs of the shift registers as shown in Fig. 3 when stored values are “ALL0” and the clock signal is “1” (master latches are in the hold state). The MCU/SEU is up to 23.4% which is close to that on 65-nm SRAM cells [8]. These results clearly show that soft-error rate on TMR FFs caused by MCUs is only 46.8% of that on FFs. In contrast, the shift register (d) has a very low MCU rate and only one MCU is observed on it. The number of MCUs is reduced from 110 to 1 by inserting well-contact arrays under supply and ground rails of FFs. Therefore, we can improve soft-error resilience of the redundant FFs without delay overhead by inserting well-contacts between latches. It also shows that almost all MCUs are caused by the parasitic bipolar effect since it is caused by well-potential perturbation [12]. In the shift register (a)–(c), we observe more than 3-bit MCUs as shown in Fig. 9. We assume that 5 to 8-bit MCUs are caused by successive hits by one secondary ion because they spread in line [13].

Table 2 shows SEU and MCU rates on shift register (a) and (d) when the clock signal is “0” (slave latches are in the hold state). All shift registers have higher SEU rates when stored values are “ALL1” and the output node of the tri-state inverter in the slave latch (N_{TS}) in Fig. 4 is “1”. The tri-state inverters have smaller critical charge than the inverters since the tri-state inverters have weaker drive strength. It suggests that nMOS transistors are weak to SEUs. N_{TS} in Fig. 4 is flipped to “0” when a particle hits on the nMOS transistor in the tri-state inverter. In the fabricated structure, no MCU is observed at N_{TS} = 0 as shown in Table 2 and 96% of MCUs are on FFs whose p-bulk are shared, which is consistent with the results of [6]. It shows that almost all MCUs are induced when a particle hits on nMOS transistors constructing the tri-state inverter.

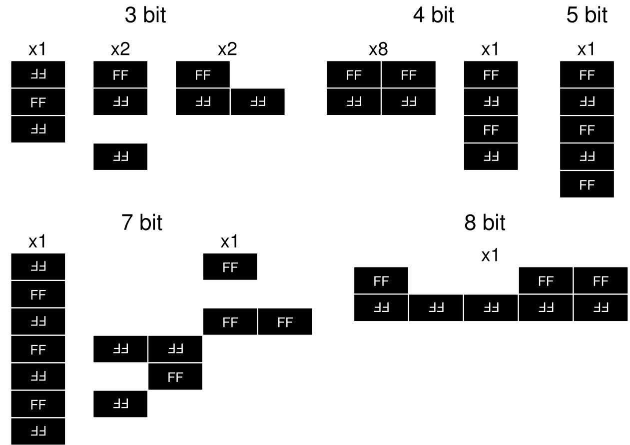

Fig. 9 MCU patterns with more than 3 bits flipped.

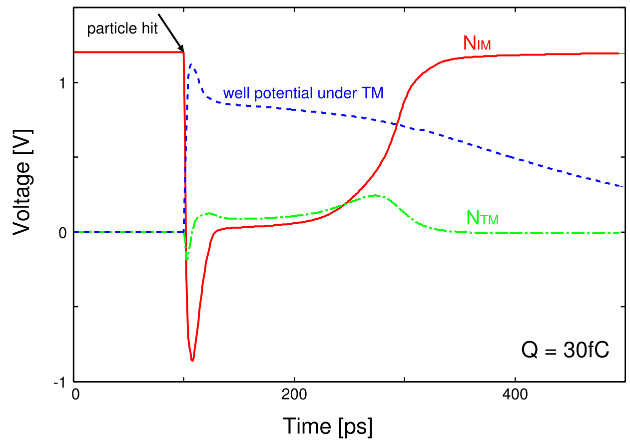

Fig. 10 The parasitic bipolar effect keeps FFs from be flipped, which is calculated from circuit-level simulation [16].

Compared with SEU rates on shift registers, shift register (d) has the highest SEU rate at N_{IS} = 0. It is because the parasitic bipolar effect prevents FFs from being flipped at N_{TS} = 0 [15].

We explain its phenomena using the circuit level simulation result as shown in Fig. 10 in the case that a neutron hits on the inverter (IS) [16].

1. A neutron hits on the inverter (IS) in FF at N_{TS} = 0.
2. N_{IS} turns to “0” by generated electrons and p-well potential is elevated by generated holes.
3. When there are a lot of generated holes, N_{TS} does not turn to “1”. The parasitic bipolar transistors of nMOS transistors turn on by p-well potential perturbation.
4. After p-well potential returns to 0, N_{TS} and N_{IS} rise to “1” simultaneously.
5. As a result, N_{IS} return to “1” and N_{TS} keeps “0” since IS has about 4 times bigger drive strength as

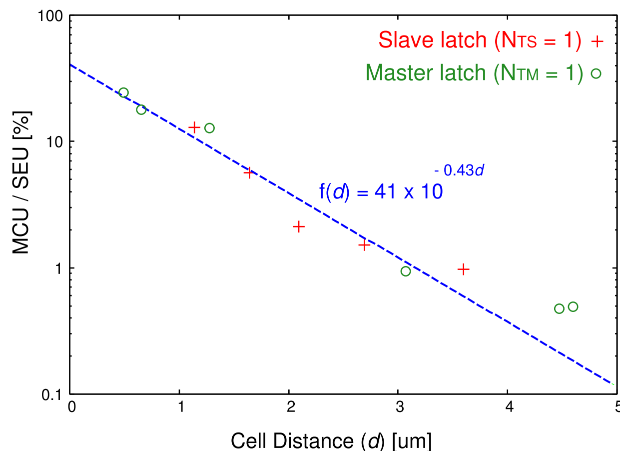

Fig. 11 Distance-dependence of MCUs.

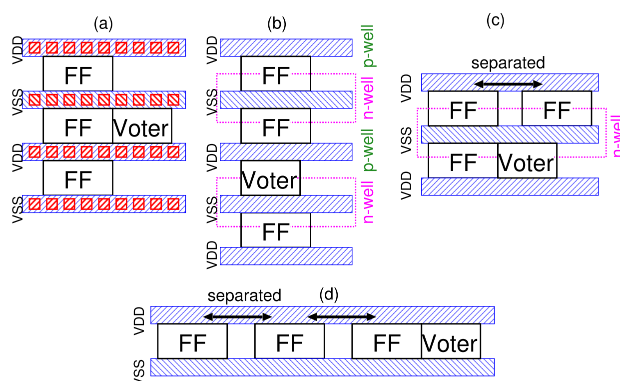

Fig. 12 Placement of triple modular redundant FFs for effective soft-error resilience.

shown in Fig. 4 and its output, N_{IS} rises to "1" more quickly than N_{TS}.

Stored values are not flipped by the parasitic bipolar effect. It is consistent with no MCU at $N_{TS} = 0$.

Figure 11 shows the distance-dependence of MCU/SEU on FFs which is obtained from the shift registers (a)–(c). The MCU/SEU (y-axis) is calculated from measurement results at $N_{TM} = 1$ or at $N_{TS} = 1$. In Fig. 11, MCU/SEU includes less than 4 bit MCUs since 5–8 bit MCUs occur with over 5 μm cell-distance and each MCU is observed only once.

The MCU/SEU is exponentially decreased according to $10^{-0.43d}$ (d is the distance between two latches) and is consistent with the MCU/SEU on 45 nm SRAMs and error rates on redundant FFs [17]. This result is also consistent with our device simulation results [18]. As shown in Fig. 4, master and slave latches in the FF have different structure. However, measurement results of MCU/SEU are distributed along the same straight line. Therefore, the MCU/SEU does not depend on the drive strength and load capacitance. As mentioned above, almost all MCUs are caused by the parasitic bipolar effect. Thus, we assume that a coefficient of fitting line highly depends on the well structure, well-contact distance, impurity density and current amplification coefficient and does not depend on technology nodes directly. G. Gasiot shows experimental neutron MCU rates on SRAMs as a function of technology feature size. MCU rates are exponentially increased when the technology nodes scale down [8]. Suppose that technologies scale down is correlated with the cell distance, MCU/SEU does not depend on the technology node but depends on the cell distance. To achieve same error rates on TMR FF fabricated in different technology nodes, required cell distances are almost equivalent even if technology nodes are different. Compared with the cell size, the required cell distance and area overhead are relatively increased in advanced technology nodes.

For higher LSI reliability, when we implement TMR FFs, we should separate FFs which compose a TMR FF from each other and keep them apart as much as possible in order to reduce MCU rate and achieve higher error resilience. However, it consumes huge area or complicated design procedures. There are trade-off between LSI reliability and area overhead.

In the fabricated technology, we suggest the placement of redundant FFs as follows and as in Fig. 12 for effective soft-error resilience.

1. Insert well-contacts between their FFs (Fig. 12 (a)).
2. Implement each FF on different p-well regions (Fig. 12(b)).
3. Implement p-well-sharing FFs in a horizontal line for separating their FFs from each other (Fig. 12 (c) and (d)).

6. Conclusion

We measured neutron-induced MCUs on FFs in a 65-nm bulk CMOS process in order to evaluate their dependencies on the distance of FFs and well-contact density. Accelerated neutron test results show that the MCU/SEU is up to 23.4% and it is exponentially decreased by the distance of latches. The MCU is an urgent issue for redundant FFs and the MCU mitigation design is required in 65-nm and less technologies nodes. The measurement results also show that MCU rates can drastically be reduced by inserting well-contact arrays between FFs. The number of MCUs is reduced from 110 to 1 by inserting well-contact arrays under supply and ground rails. We can improve soft-error resilience without delay overhead by inserting well contacts between latches on rad-hard FFs.

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Mentor Graphics Corporation, STARC, e-Shuttle, Inc., and Fujitsu Ltd.

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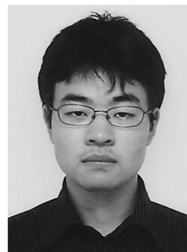

Jun Furuta received B.E. degree in Electrical and Electronic Engineering and M.E. and D. degrees in Informatics from Kyoto University, Kyoto, Japan, in 2009, 2011, 2014, respectively. He is currently a project assistant professor at Kyoto Institute of Technology.

Kazutoshi Kobayashi received his B.E., M.E. and Ph. D. in Electronic Engineering from Kyoto University, Japan in 1991, 1993, 1999, respectively. Starting as an Assistant Professor in 1993, he was promoted to associate professor in the Graduate School of Informatics, Kyoto University, and stayed in that position until 2009. For two years during this time, he acted as associate professor of VLSI Design and Education Center (VDEC) at the University of Tokyo. Since 2009, he has been a professor at Kyoto Institute of Technology.
While in the past he focused on reconfigurable architectures utilizing device variations, his current research interest is in improving the reliability (Soft Errors and Bias Temperature Instability) of current and future VLSIs.
He was the recipient of the IEICE best paper award in 2009 and the IRPS best poster award in 2013.

Hidetoshi Onodera received the B.E., and M.E., and Dr. Eng. degrees in Electronic Engineering from Kyoto University, Kyoto, Japan, in 1978, 1980, 1984, respectively. He joined the Department of Electronics, Kyoto University, in 1983, and currently a Professor in the Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University. His research interests include design technologies for Digital, Analog, and RF LSIs, with particular emphasis on high-speed and low-power design, design and analysis for manufacturability, and SoC architectures.
Dr. Onodera served as the Program Chair and General Chair of ICCAD and ASP-DAC. He was the Chairman of the Technical Group on VLSI Design Technologies, IEICE, Japan, and the Chairman of the IEEE Kansai SSCS Chapter, and the Chairman of the SIG-SLDM (System LSI Design Methodology), IPSJ, Japan. He is currently the Chairman of the IEEE Kansai CASS Chapter. He served as the Editor-in-Chief of IEICE Transactions on Electronics, and currently he is serving as the Editor-in-Chief of IPSJ Transactions on System LSI Design methodology.