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A Radiation-Hard Redundant Flip-Flop to Suppress Multiple Cell Upset by Utilizing the Parasitic Bipolar Effect

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SUMMARY According to the process scaling, radiation-hard devices are becoming sensitive to soft errors caused by Multiple Cell Upset (MCUs). In this paper, the parasitic bipolar effects are utilized to suppress MCUs of the radiation-hard dual-modular flip-flops. Device simulations reveal that a simultaneous flip of redundant latches is suppressed by storing opposite values instead of storing the same value due to its asymmetrical structure. The state of latches becomes a specific value after a particle hit due to the bipolar effects. Spallation neutron irradiation proves that MCUs are effectively suppressed in the D-FF arrays in which adjacent two latches in different FFs store opposite values. The redundant latch structure storing the opposite values is robust to the simultaneous flip.

key words: *DMR, soft error, MCU, device simulation*

1. Introduction

Process scaling makes LSIs less reliable to temporal and permanent failures. Temporal failures flip a stored value on SRAMs or flip flops. A radiation particle hit is one of main sources of temporal failures, which is called a "soft error." Soft errors are classified into Single Event Upset (SEU) and Single Event Transient (SET). SEU is caused by a particle hit on sequential elements, and SET is caused by a particle hit on combinational circuits. Recently, parasitic bipolar effects have been reported to be a source of multiple cell upset (MCUs). Seifert et al. [1] reveals that the probability of MCUs compared with SEUs is 10% in a 65 nm process. MCUs are one of critical issues to diminish soft-error resiliency of radiation designs.

Various redundant flip-flop structures are proposed such as TMR, DICE [2] and BISER [3] to mitigate soft errors, However, aggressive process scaling makes the probability of MCUs greater. MCUs are one of critical issues to diminish soft-error resilience of radiation-hard designs because these designs are very sensitive to simultaneous flips. The parasitic bipolar effect plays an important role on soft errors in a current deep-submicron process [4]. If a particle hit on a transistor, adjacent transistors are affected by the parasitic bipolar effects, which results in an MCU of redundant components. In this paper, shows the parasitic bipolar effects to have a significant impact on MCUs. We show that two latches storing opposite values can suppress the simultaneous flip due to the parasitic bipolar effect [5]. All simulation models are constructed by using a 65-nm process.

This paper is organized as follows. Sections 2 and 3 explains the relationship between latch and the parasitic bipolar effects. In Sect. 4, device-level simulations investigate the simultaneous flip and error rate of redundant latches in detail. Section 5 shows the experimental results by spallation neutron irradiation of a D-FF array. Finally, we conclude this paper in Sect. 6.

2. Relationship between the Parasitic Bipolar Effects and SEU

When a neutron hits to a Si atom, the electron-hole pairs are generated. The electrons can be collected at the drain-well or well-substrate junction. However, the holes are left in the p-well, which reduces the source-well potential barrier due to the increase in the potential of the p-well. Thus, the source injects electrons into the channel which can be collected at the drain. This effect is called the parasitic bipolar effect because the source-well-drain of the NMOS transistor acts as a n-p-n bipolar transistor. It will turn on the parasitic bipolar transistor. SRAMs in the triple-well structure have 3.5x higher probability of MCUs compared to twin-well in a 65-nm process by neutron irradiation [6]. Due to these bipolar effects, adjacent transistors are affected, which results in simultaneous upsets of latches. These simultaneous upsets diminish the error resilience of redundant latches. But it is possible to eliminate simultaneous upsets from soft errors by enhancing circuit structures which utilizes the parasitic bipolar effects.

Figure 1 is a conventional latch structure and its layout. Figure 2 shows two circuit level simulations results [7] when generated charge (Q) is 10 fC and 20 fC respectively. A particle hit on the NMOS transistor of I0 in Fig. 1 (red

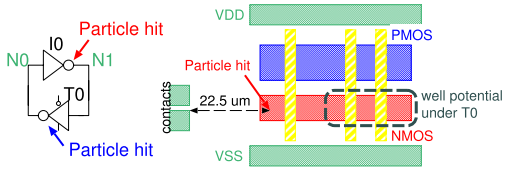

Fig. 1 Schematic (left) and layout (right) of conventional latch.

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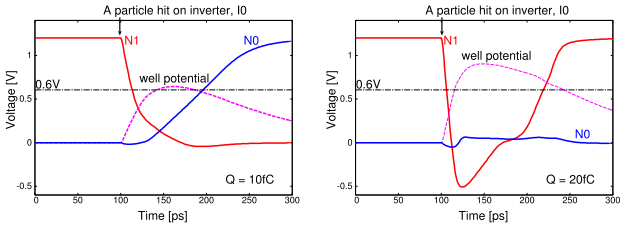
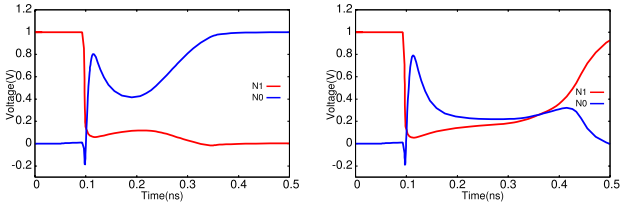


(a) (b)

Fig. 2 Circuit-level transient simulation by a particle hit on I0 in Fig. 1 with Q=10 fC (a) and Q=20 fC (b).

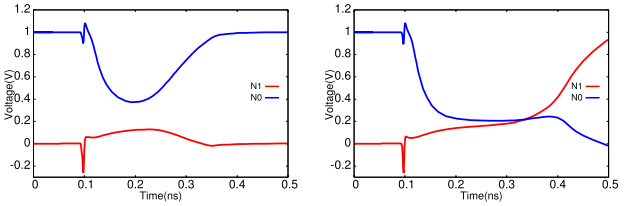


(a) Q=30 fC (b) Q=80 fC

Fig. 3 Transient waveform of N1 and N0 by a perpendicular particle hit on T1 according to the charge "Q" (N1=1, N0=0).

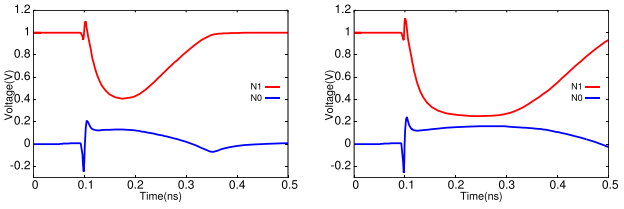
line). Well contacts are placed at 22.5 μm far away from the particle hit. If generated charge is more than the critical charge (Q_{crit}), the latch is upset as in Fig. 2(a). Thus the latch is always upset by a particle hit with higher energy without considering parasitic bipolar effects. On the other hand, if generated charge is large enough to elevate well potential under T0 above a certain level, the latch is stable with considering the parasitic bipolar effect as in Fig. 2(b). In this case, the output values of the inverter becomes around 0 after a particle hit. Due to the high particle energy, the bipolar transistor under the tristate inverter is turned on. Thus, the output values of these two components keep 0 for a while at the same time. When the well potential falls to a certain level at which the bipolar transistors turn off, the output of the inverter always goes back to its original state. It is because the delay time of the inverter is faster than the tristate inverter. The variation may influence the delay time. By the circuit-level simulations, the tristate inverter is never faster than the inverter even if variations influence delay. Note that we assume that variations influences the transistor parameters by 2σ since these two inverters are placed very closely. Thus, by utilizing the parasitic bipolar effects, it is possible to enforce redundant flip-flops to MCUs and soft errors.

There are two device simulation results as shown in Figs. 3(a) and (b). They are the similar to the results of circuit simulations in Fig. 2 when a particle hit (red line) on the NMOS I0 of the conventional latch. Figures 4(a) and (b) show other device simulation results when N0=1, N1=0. In this case, the latch is not stable even if the parasitic bipolar transistor turns on. Due to the parasitic bipolar effect, the outputs of the inverter and the tristate inverter keep "0". After the bipolar transistor turns off, the inverter always goes to "1" before the tristate inverter. Thus the latch is upset when Qcrit is large in this case.



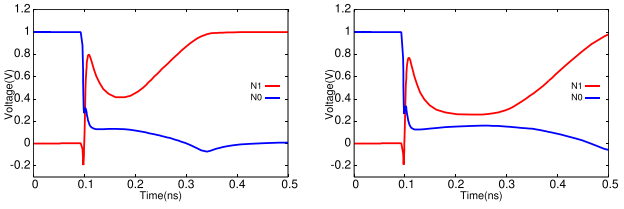
(a) Q=30 fC (b) Q=80 fC

Fig. 4 Transient waveform of N1 and N0 by a perpendicular particle hit on T1 according to the charge "Q" (N1=0, N0=1).



(a) Q=30 fC (b) Q=80 fC

Fig. 5 Transient waveform of N1 and N0 by a perpendicular particle hit on T0 according to the charge "Q" (N1=0, N0=1).



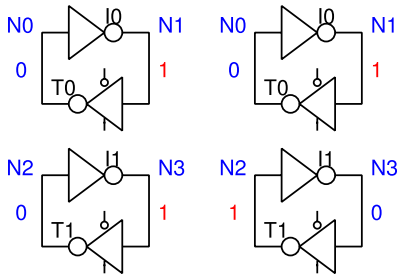
(a) Q=30 fC (b) Q=80 fC

Fig. 6 Transient waveform of N1 and N0 by a perpendicular particle hit on T0 according to the charge "Q" (N1=0, N0=1).

There are other two simulations results as shown in Figs. 5(a) and (b) when a particle hit (blue line) on the tristate inverter T0. The latch is always stable (Fig. 5) when N0=0, N1=1, because the parasitic bipolar transistor under the tristate inverter is always "ON" by a particle hit. The tristate inverter always keeps "0". Then, the inverter goes back to its initial state quickly when the bipolar transistors turn off. In contrast the latch is always upset (Fig. 6) when N0=1, N1=0. In this case, the parasitic bipolar effects keep the outputs of tristate inverter and inverter "0" at the same time. However, the inverter always goes to "1" firstly.

3. Redundant Latch Structure to Suppress MCUs

Figure 7(a) shows a pair of redundant latches which store the same value in conventional redundant FFs such as TMR or BISER, while Fig. 7(b) shows of those storing the opposite values in the BCDMR FF [8] as shown in Fig. 8. In the BCDMR FF, two latches (ML0+ML1 or SL0+SL1) and a keeper (KM or KS) construct a triple-modular redundancy (TMR). In BISER or BCDMR, the output of FFs is stable even if one of two redundant latches is flipped. In order to eliminate a simultaneous flip among these TMR compo-



(a) Store the same value (b) Store opposite values

Fig. 7 Two redundant latch structures.

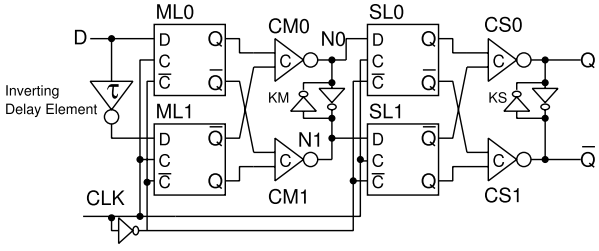


Fig. 8 BCDMR FF.

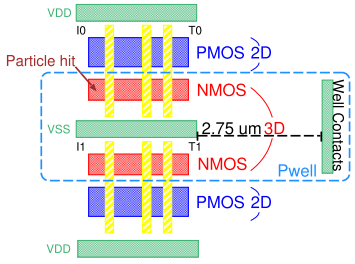


Fig. 9 Two latches placed in two rows (DHC).

nents, these two latches are placed in two rows as shown in Fig. 9, which structure is called the double-height cell structure [9]. The keeper is in the same row as one of two latches but it is placed as far apart as possible [10] from the latch. If both redundant latches stores the same value as in Fig. 7(a), they can be upset at the same time by a particle hit. It is because the parasitic bipolar effects change the latches to the same value. However, if both latches store the opposite values, a particle hit with large amount of charge may change the latches to the same value. At least one of two latches is stable in the original state when they store opposite values. As a result, the output of the redundant FF is not flipped. The possibility of the simultaneous flip can be drastically reduced when both latches store opposite values.

4. Device-Level Simulations

In this section, we use device simulations to show that MCUs are suppressed by the parasitic bipolar effects.

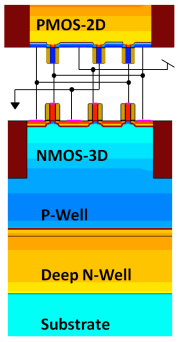


Fig. 10 Mixed-mode model.

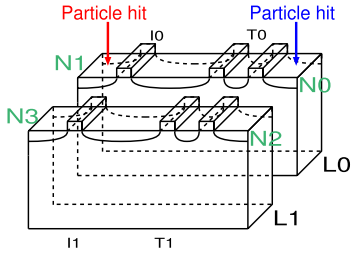


Fig. 11 Perpendicular particle hit on NMOS of I0 or T0.

4.1 Device-Level Simulation Setup

Figure 9 shows the layout structure of two latches placed in two rows sharing the NMOS region in the p-well. The double-height cell structure sharing PMOS regions is more robust to soft errors than sharing the NMOS regions, since the mobility of holes is slower than that of electrons. For showing the results clearly, we constructed the device models sharing the NMOS regions. As the full 3D device-level model prolong simulation time, the mixed-mode device-simulation is used in which the 2D PMOS and 3D NMOS device-level models are connected by wires in the circuit-level as shown in Fig. 10. The well contact is placed at 2.75 μm from T0 and T1. The distance between I0 (T0) and I1 (T1) is 0.3 μm. The area of the p-well is 10 μm $\times$ 10 μm. As we mentioned in the Sect. 2, MCUs are very likely to occur in the triple well structure. Thus all device-level structures are constructed in the triple-well. The device model is constructed according to the 65-nm device structures and parameters in [11].

According the results of device simulations, there are MCUs in both structure in which two latches store the same or opposite values. However, the MCU rates of the structure in which two lathes store opposite values are much lower. We explain details in the following sections.

4.2 Perpendicular Particle Hit Case

When a particle hit on the NMOS transistor of I0 perpendicularly as drawing with the red line in Fig. 11, the upper latch (L0) is affected by the collected charge and the bipolar effect

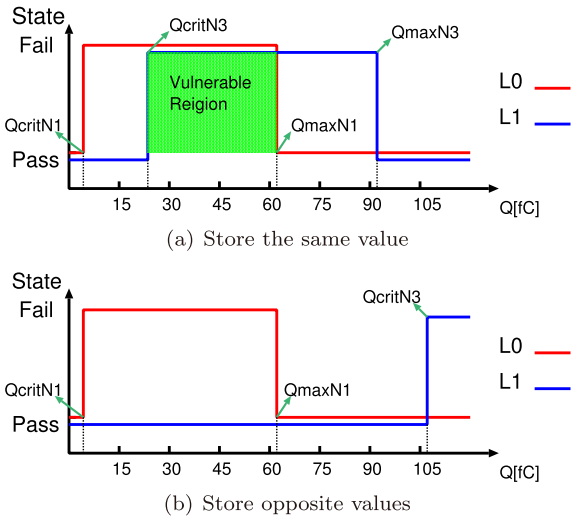


Fig. 12 States of N1 and N3 by a perpendicular particle hit according to the charge "Q".

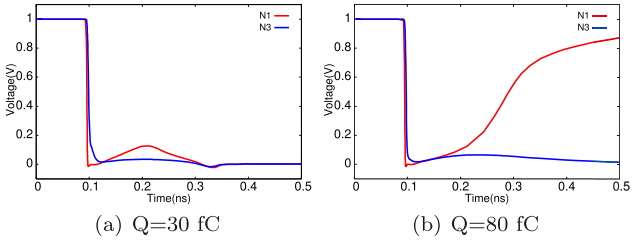


Fig. 13 State of N1 and N3 vs. Q when two latches store the same value (N1=1,N3=1).

while the lower latch (L1) is mainly affected by the bipolar effect.

Figures 12(a) and (b) represent the states of the pair of two latches according to the charge collected to the node N1 and N3 as in Fig. 7. We set "1" as the original value of N1. The results when latches stores the same value (N3=1) and opposite values (N3=0) are shown in Figs. 7(a) and (b), respectively. The values of "Q", $Q_{\mathrm{crit}N_x}$, $Q_{\mathrm{max}N_x}$ denote the collected charge when a latch is flipped and goes back to its original state by the parasitic bipolar effect, respectively.

When two redundant latches store the same value, they are flipped at the same time by charge between $Q_{\mathrm{crit}N_3}$ and $Q_{\mathrm{max}N_1}$ as shown in Fig. 2(a). We call the green region in Fig. 12(a) as the vulnerable region in which both redundant latches flip. The inverter I0 is stable at its original state and the tristate inverter T0 does not flip at the charge above $Q_{\mathrm{max}N_x}$ by the parasitic bipolar effect as shown in Fig. 2(b). A vulnerable region exists between 22.5fC and 62 fC as in Fig. 12(a) when latches store the same value. When they store the opposite values, however, they are not flipped at the same time as shown in Fig. 12(b). In this case, T1 is vulnerable, but the required charge is much more than I0 because of its poor drivability. Therefore, there is no vulnerable region in which both redundant latches are flipped at the same time. Figures 13(a) and (b) show transient voltage

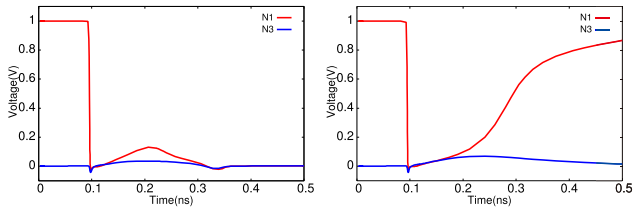


Fig. 14 State of N1 and N3 vs. Q when two latches store opposite values (N1=1, N3=0).

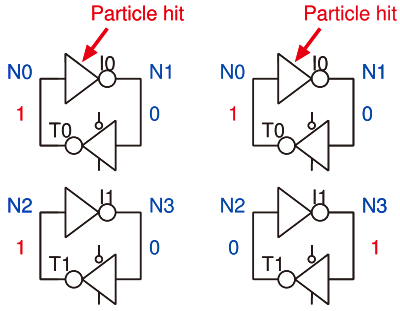
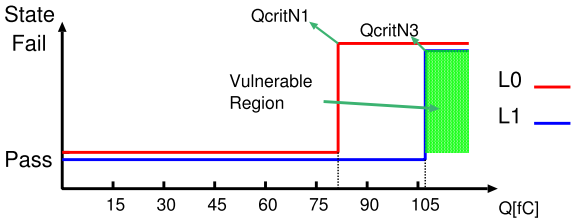


Fig. 15 Circuit structure of two latches which set "0" to node N1.

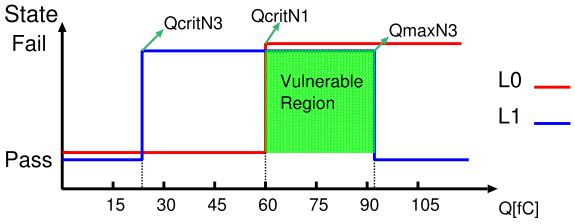
waveforms obtained from device-level simulations of particle hits with collected charge Q=30 fC and 80 fC in which the latches store the same value. The original value of N1 is "1". The node N1 flips at Q=30 fC but goes back to its original state at Q=80 fC, while the node N3 flips in both cases. In contrast, Figs. 14(a) and (b) show transient voltage waveforms when the collected charge Q=30 fC and 80 fC in which the latches store the opposite values. The node N3 does not flip in both cases. No simultaneous flips are observed.

When we set "0" as the original value of N1 as in Figs. 15(a) and (b), the results of these two situations in which two redundant latches store the same value and opposite values are shown in Figs. 16(a) and (b) respectively. In the former case, they are flipped at the same time when the collected charge is bigger than 107fC as in Fig. 16(a). In the latter case, they are also flipped at the same time by the collected charge between 60 fC and 92 fC as in Fig. 16(b). The MCU tolerance when storing the opposite value is much stronger when storing the same value as in Fig. 12(a).

Figure 17 shows other two results of device simulations in which a particle hit on NMOS of the tristate inverter T0 when N1=N3=0 (Fig. 11 (blue line)). When N1=0, both latches are flipped at the same time as shown in Fig. 17(a) when both latches store the same value. Only one latch is flipped when the two lathes store opposite values as in Fig. 17(b). Thus, there is no vulnerable region when two lathes store opposite values in this case. In contrast, there is no MCU occurrence in both of redundant FFs when N1=1.

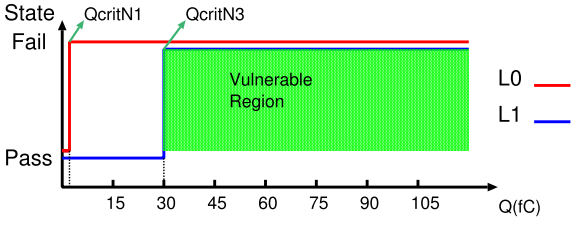


(a) two latches storing the same value

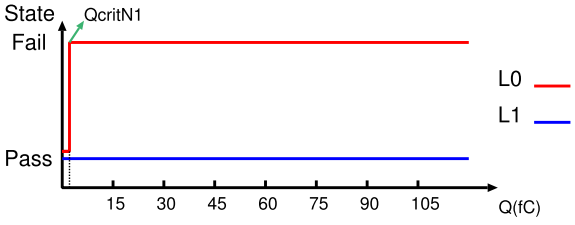


(b) two latches storing opposite values

Fig. 16 State of N1 and N3 vs. Q (N1=0).



(a) two latches store the same value (N1=N3=0)



(b) two latches store opposite values (N1=0, N3=1)

Fig. 17 State of N1 and N3 vs. Q (particle hit on the tristate inverter).

4.3 Diagonal Particle Hit Case

On the perpendicular particle hit in the previous section, one of two latches is affected by collected charge and the bipolar effect, while the other is mainly affected by the bipolar effect. We investigate the vulnerability of two redundant latches by changing the angles of particle hits as in Fig. 18.

The angles of particle hits are set to 30 degree in all three cases. Figures 19(a)–(c) show the results when the two latches store the same value (N1=1). In the case of I0 to I1, the vulnerable region becomes wider mainly due to lower Q_{critN3}. The critical charge of N3 Q_{critN3} becomes lower since the diagonal hits promote the parasitic bipolar effect on I1. This is the weakest case when storing the same value. However, the vulnerable region becomes narrower when a particle passes from I0 to T1. It is mainly due to lower Q_{maxN1}. The bipolar transistor on T0 turns on by a

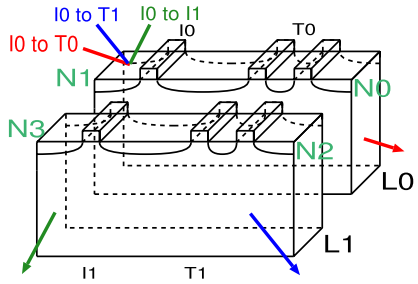
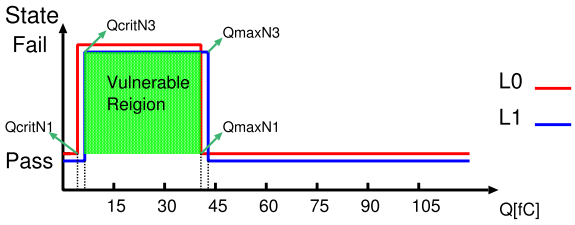
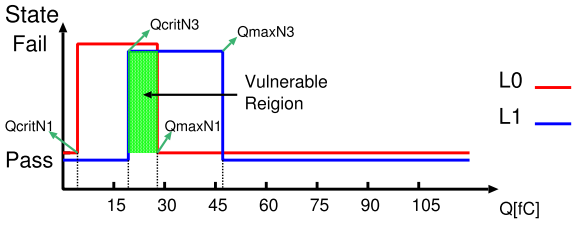


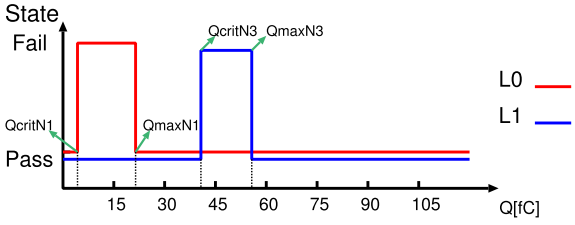
Fig. 18 Diagonal particle hits on I0 to I1, T1 and T0.



(a) I0 to I1 case



(b) I0 to T1 case



(c) I0 to T0 case

Fig. 19 State of N1 and N3 according to collected charge "Q" when a particle hit diagonally on two latches which store the same value.

Table 1 Collected charge "Q" (fC) in the latches which store the same value (Diagonal particle hit case).

	Q_{critN1}	Q_{maxN1}	Q_{critN3}	Q_{maxN3}
I0 to I1	5.2	41.8	5.5	44.0
I0 to T1	5.2	29.0	18.4	46.6
I0 to T0	5.2	22.6	40.8	53.0

lower-energy particle because it passes much closer to T0. When a particle passes I0 to T0, there is no vulnerable region because of lower Q_{maxN1} and higher Q_{critN3}. In contrast, there is no vulnerable region in the structure storing the opposite values in any particle direction. Tables 1 and 2 summarise the collected charge of N1 and N3 in both cases of the perpendicular and diagonal particle hits.

Table 2 Collected charge "Q" (fC) in the latches which store opposite values (Diagonal particle hit case).

	Q_{critN1}	Q_{maxN1}	Q_{critN3}
I0 to I1	5.2	41.8	57.5
I0 to T1	5.2	29.0	69.7
I0 to T0	5.2	22.6	79.5

Table 3 Parameters for SER estimation.

F ($\mathrm{cm}^{-2}\mathrm{s}^{-1}$)	5.65e-3
Q_s (fC)	5.72
K	2.2e-5

Table 4 Qcrit and MCU rates from device simulations.

Latch state (N1/N3)	Q_{crit}	SER
Store the same value (1/1)	22.5 fC	1.48 FIT/Mbit
Store opposite values (1/0)	60.2 fC	2.10e-3 FIT/Mbit

Table 5 Qcrit and SEU rates from device simulations.

Particle hit on	Q_{crit}	SER
Inverter	5.2 fC	30.5 FIT/Mbit
Tristate inverter	4.2 fC	36.3 FIT/Mbit

4.4 Soft Error Rate Calculation

Equation (1) [12] is used to calculate SER in FIT (Failure In Time, error number/$10^1$0 s).

$$N_{\mathrm{SER}}(Q_{\mathrm{crit}}) = F \times A \times K \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_s}\right) \quad (1)$$

where F is the high-energy neutron flux and A is the drain area of transistors related to soft errors. K is a fitting parameter. Q_s is called "charge collection efficiency" that is correspond to the sensitivity of the critical charge. Q_s strongly depends on doping and supply voltage [13]. We use the parameter values as in Table 3 that are scaled from 100 nm [12] to 65 nm.

MCU rates are calculated by the minimum charge which two latches flipped at the same time as shown in Table 4. SEU rates are calculated by the minimum value of "Q" at which only one latch is flipped. The SEU rates of the inverter and the tristate inverter are shown in the Table 5. Note that the device simulations results in which perpendicular particle hit on the latches is used to calculate the error rates. MCU rates of the structure in which two latches store opposite values are roughly 1,000 times lower than those of the same values.

5. Experimental Results by Neutron Irradiation

A test chip was fabricated in a 65 nm bulk CMOS process including a general D-FF array to show vulnerabilities of FFs by the parasitic bipolar effect. Figure 20 show the layout structure of the FF array [14] which consists of a D-FF in Fig. 21. Spallation neutron-beam irradiation was carried out at RCNP of Osaka University. Clock is fixed to 0 or 1

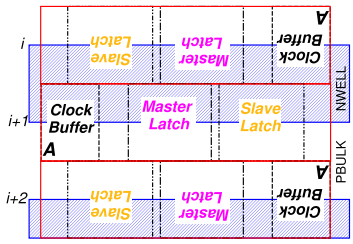


Fig. 20 Floorplan of the general D-FF array to measure MCUs/SEUs rates.

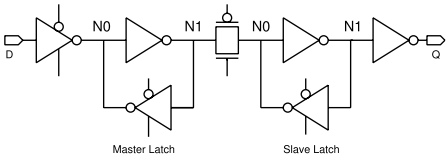


Fig. 21 Schematic of D-FF.

Table 6 The numbers of SEUs and MCUs from experimental results.

Latch state (N1/N3)	N_{SEU}	N_{MCU}
Store the same value (1/1)	483	155
Store opposite values (1/0)	138	1

Table 7 MCUs/SEUs ratio from experimental results and device simulations.

States of two latches (N1/N3)	Experimental	Device Simulation
Store the same value (1/1)	0.3	0.05
Store opposite values (1/0)	0.7e-2	6.5e-5

to keep master or slave latches in the latch state. Table 6 show the numbers of SEUs and MCUs when both latches store the same value and opposite values, respectively. Table 7 show the MCUs/SEUs ratio according to the states of two lathes. Accrding to the results of device simulations, the MCU rates of the structure in which two latches store opposite values are roughly 1,000 times lower than those of the same values. The MCUs/SEUs ratio of the experimental results is 10x bigger that of the device simulations.

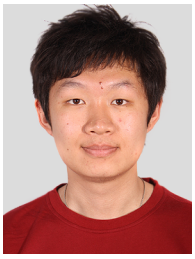
6. Conclusion

We show that two redundant latches store opposite values suppress a simultaneous flip by a particle hit effectively due to the parasitic bipolar effect. In contrast, redundant latches store the same value are very sensitive to MCUs. From device-level simulations, both latches store the same value are flipped between a certain range of generated charge which is called a vulnerable region. Because of the asymmetric structure of latches, they become a specific state when the parasitic bipolar transistors turn on by a particle hit. When storing opposite values in two latches, both latches become the same state by a particle hit. But it does not change the output of the redundant FFs because one of these two latches stores the correct value. Even if there is also MCU occurrence in the latter, the probability is very low. Experimental results on a D-FF array fabricated in

a 65 nm CMOS prove that the error rates of MCU is about 1,000 times lower when latches store opposite values. The ratio of MCUs/SEUs from the device simulations is lower than the results of experiments. However, the MCU rates of the structure in which two latches store opposite much lower in device simulations and experimental results. The parasitic bipolar effect is one of dominant factors of MCUs to decrease the reliability of redundant FFs. But the simple circuit-level technique to store the opposite values enhances the tolerance to MCUs without any area, power and delay overhead.

References

[1] N. Seifert, P. Slankard, M. Kirsch, B. Narasimham, V. Zia, C. Brookreson, A. Vo, S. Mitra, B. Gill, and J. Maiz, "Radiation-Induced soft error rates of advanced CMOS bulk devices," IRPS, pp.217–225, March 2006.
[2] D. Krueger, E. Francom, and J. Langsdorf, "Circuit design for voltage scaling and SER immunity on a quad-core itanium processor," ISSCC, pp.94–95, Feb. 2008.
[3] S. Mitra, M. Zhang, S. Waqas, N. Seifert, B. Gill, and K.S. Kim, "Combinational logic soft error correction," ITC, pp.1–9, Oct. 2006.
[4] N. Mikami, T. Nakauchi, A. Oyama, H. Kobayashi, and H. Usui, "Role of the deep parasitic bipolar device in mitigating the single event transient phenomenon," IRPS, pp.936–939, April 2009.
[5] K. Zhang, R. Yamamoto, J. Furuta, K. Kobayashi, and H. Onodera, "Parasitic bipolar effects on soft errors to prevent simultaneous flips of redundant flip-flops," IEEE International Reliability Physics Symposium, pp.5B.2.1–5B.2.4, April 2012.
[6] I. Chatterjee, B. Narasimham, N.N. Mahatme, B.L. Bhuva, R.D. Schrimpf, J.K. Wang, B. Bartz, E. Pitta, and M. Buer, "Single-event charge collection and upset in 40-nm dual- and triple-well bulk CMOS SRAMs," IEEE Trans. Nucl. Sci., vol.58, no.6, pp.2761–2767, Dec. 2011.
[7] J. Furuta, R. Yamamoto, K. Kobayashi, and H. Onodera, "Correlations between well potential and seus measured by well-potential perturbation detectors in 65 nm," Solid State Circuits Conference (A-SSCC), 2011 IEEE Asian, pp.209–212, Nov. 2011.
[8] J. Furuta, C. Hamanaka, K. Kobayashi, and H. Onodera, "A 65 nm bistable cross-coupled dual modular redundancy flip-flop capable of protecting soft errors on the C-element," VLSI Cir. Symp., pp.123–124, June 2010.
[9] N. Seifert, V. Ambrose, B. Gill, Q. Shi, R. Allmon, C. Recchia, S. Mukherjee, N. Nassif, J. Krause, J. Pickholtz, and A. Balasubramanian, "On the radiation-induced soft error performance of hardened sequential elements in advanced bulk cmos technologies," IRPS, pp.188–197, May 2010.
[10] R. Yamamoto, C. Hamanaka, J. Furuta, K. Kobayashi, and H. Onodera, "An area-efficient 65 nm radiation-hard dual-modular flip-flop to avoid multiple cell upsets," IEEE Trans. Nucl. Sci., vol.58, no.6, pp.3053–3059, Dec. 2011.
[11] R. Garg and S.P. Khatri, Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations
[12] P. Hazucha, C. Svensson, and S. Wender, "Cosmic-ray soft error rate characterization of a standard 0.6 μm CMOS process," IEEE J. Solid-State Circuit, vol.35, no.10, pp.1422–1429, 2000.
[13] P. Hazucha and C. Svensson, "Impact of CMOS technology scaling on the atmospheric neutron soft error rate," IEEE Trans. Nucl. Sci., vol.47, no.6, pp.2586–2594, 2000.
[14] J. Furuta, C. Hamanaka, K. Kobayashi, and H. Onodera, "A 65 nm flip-flop array to measure soft error resiliency against high-energy neutron and alpha particles," Asia and South Pacific Design Automation Conference, no.6, pp.83–84, Jan. 2011.



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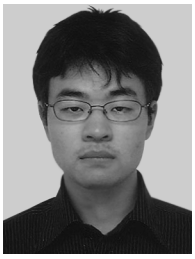

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