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Variation-Tolerance of a 65-nm Error-Hardened Dual-Modular-Redundancy Flip-Flop Measured by Shift-Register-Based Monitor Structures

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SUMMARY We show measurement results of variation-tolerance of an error-hardened dual-modular-redundancy flip-flop fabricated in a 65-nm process. The proposed error-hardened FF called BCDMR is very strong against soft errors and also robust to process variations. We propose a shift-register-based test structure to measure variations. The proposed test structure has features of constant pin count and fast measurement time. A 65 nm chip was fabricated including 40k FFs to measure variations. The variations of the proposed BCDMR FF are 74% and 55% smaller than those of the conventional BISER FF on the twin-well and triple-well structures respectively.

key words: *soft error, hardened design, variability, test structure, shift register*

1. Introduction

According to recent aggressive process scaling, a tremendous number of transistors can be integrated on a semiconductor device. It invokes several issues related to variations, reliability, power and so on. As for reliability, early failures on semiconductor devices are mainly caused by defects and wear-out failures are mainly caused by aging degradations such as BTI (Bias Temperature Instability) [1]. In addition to that, soft errors caused by a particle hit are becoming dominant during the period between the early and wear-out failures. Micro processors has ECC (Error check and Correct) circuitry to protect cache memory against soft errors since the past several decades. In addition to that, recent micro processors for servers are equipped with error-hardened clocked storage cells (latches or FFs) to protect them against soft errors [2].

We propose an error-hardened flip-flop called "Bistable Cross-coupled Dual Modular Redundancy Flip-Flop" (BCDMR FF) based on the well-known BISER (Built-In Soft-Error Resiliency) FF [3]. The error resiliency of BCDMR FFs is 150x and 7000x better than those of BISER FFs and ordinary FFs respectively [4]. BCDMR FF is also very robust to process variations due to its cross-coupled structure. We have fabricated a 65 nm chip to measure variations of BCDMR FF by implementing a large number of ring oscillators (ROs) and counters. We propose a shift-register-based test structure to measure variations of the embedded ROs. Compared with the conventional matrix-array-based test structure, the proposed test structure has features of constant pin count and fast measurement time.

The main contribution of this paper is to show the variation tolerance of BCDMR FF and proposes a shift-register-based test structure to measure performance fluctuations due to process variations by implementing a large number of ROs.

This paper is organized as follows. Section 2 introduces BCDMR FF, its robustness to soft errors and its variation tolerance. Section 3 explains the proposed shift-register-based test structure. Section 4 gives experimental results obtained from a test chip fabricated in a 65 nm process. Section 5 concludes this paper.

2. Bistable Cross-Coupled Dual-Modular-Redundancy Flip-Flop

Redundant FFs are widely used to protect them against soft errors. This section explains several related works followed by the error resiliency and variation tolerance of the proposed BCDMR FF.

2.1 Related Works

To protect FFs from soft errors caused by α particles or neutrons, redundant flip-flop structures are usually used such as TMR (Triple Modular Redundancy) FF, DICE (Dual Interlocked Storage Cell) latch [5] or BISER (Built-In Soft-Error Resiliency) FF [3] (Fig. 1). DICE has four redundant storage nodes to prevent an SEU (Single Event Upset). TMR is the supreme solution to prepare three FFs for voting by paying a large area penalty, while the BISER (also called Dual Modular Redundancy, DMR) structure has two FFs with a small weak keeper to reduce the large area overhead of TMR. The DMR structure protects an SEU caused by a particle hit on a storage node using two latches, an inverting Muller C-element and a weak keeper. Compared with TMR FF, its area penalty is smaller since the C-element and the weak keeper work as the third latch and the voter of the

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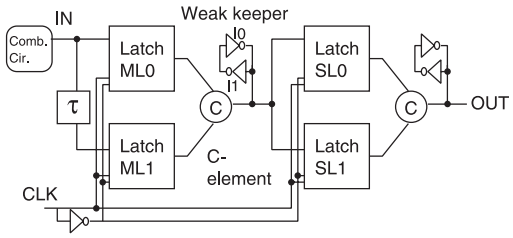

Fig. 1 BISER FF and inverting Muller C-element.

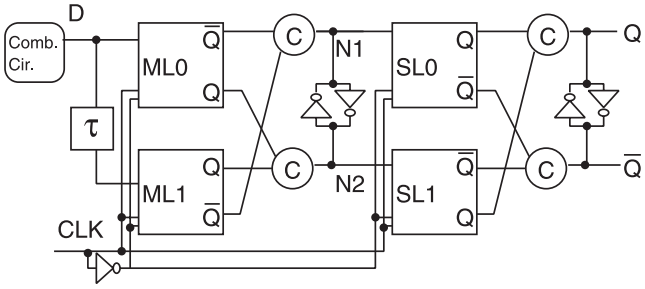

Fig. 2 BCDMR FF.

TMR. However, it is very weak to an SET (Single Event Transient) pulse caused by a particle hit on the C-element. We propose a modified DMR flip-flop called Bistable Cross-coupled Dual Modular Redundancy Flip-Flop (BCDMR FF) as in Fig. 2 [4]. It contains cross-coupled C-elements and weak keepers to prevent an unnecessary flip caused by a particle hit on the C-element.

2.2 Error Resiliency of BCDMR

BCDMR FF is very robust to soft errors compared with conventional BISER FF [4]. When a particle hit on the node N1 in the BCDMR structure, the node N1 completely flips. The node N2, however, is almost stable since the other C-element prevents N2 from flipping. In the BISER structure, however, an SET pulse from a C-element may be captured both redundant latches, which causes an upset of the redundant FF. Thus BCDMR FF is very robust to an SET pulse on the C-element. The possibility for the slave latches to capture an SET pulse from the C-element is increased by the clock frequency. The measurement results by α-particle irradiation follows such tendency. The SER (Soft Error Rate) of BCDMR FF is 15x smaller than that of BISER FF at 1 MHz, while it is 150x smaller at 160 MHz.

2.3 Variation Tolerance of BCDMR

BCDMR FF is also very robust to process variations since the weak keepers are alternately driven by two C-elements. In BISER FF, the weak keepers are driven by one C-element. If one of the weak inverter I0 in Fig. 1 becomes faster and the other inverter I1 and the C-element become slower due to the process variation, it becomes very slow for the C-element to flip the weak keeper. In BCDMR FF, however, both inverters in the weak keeper are driven by the C-elements. It is very easy to flip the cross-coupled weak keeper when process variations fluctuates characterizations of these components.

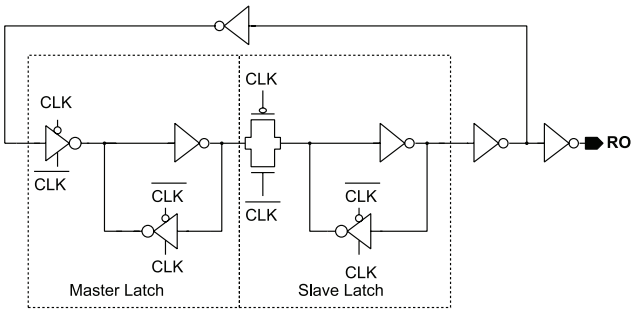

Fig. 3 Ring oscillator implemented with master and slave latches. Both latches are negative to utilize CLK as the enable signal for oscillation.

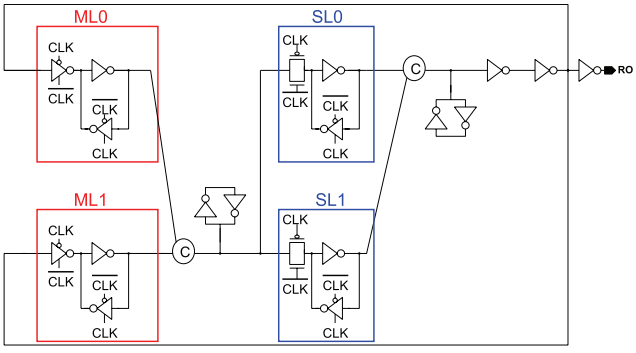

Fig. 4 BISER RO.

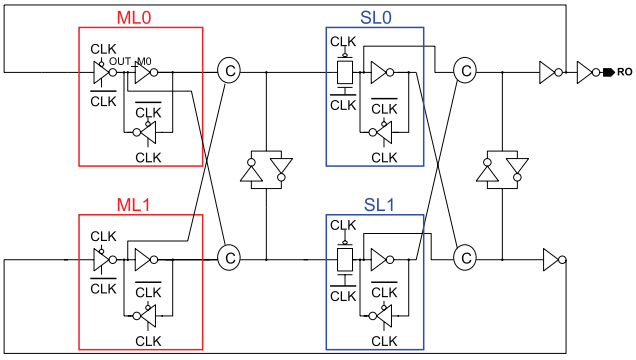

Fig. 5 BCDMR RO.

We use ring oscillators (ROs) implemented by FFs to compare variations. The ordinary master-slave edge-triggered FF is composed of master and slave latches. It consists of cascading a negative latch (master stage) and a positive one (slave stage) [6]. In order to implement ROs with the master and slave stages, both latches are constructed with negative ones as shown in Fig. 3. The clock signal CLK enables oscillation in this structure. Figures 4 and 5 show the ROs implemented with BISER and BCDMR FFs respectively. Figure 6 shows distributions of frequency due to device variations obtained from Monte Carlo simulations of 10,000 ROs, in which threshold voltages (V_{th}) of all tran-

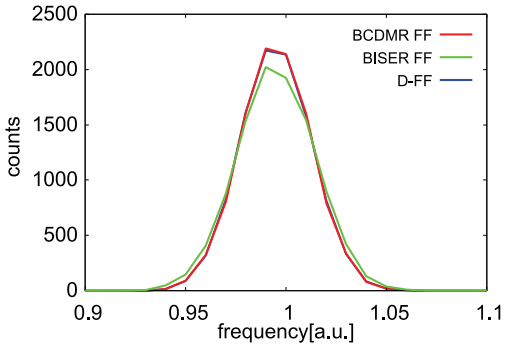

Fig. 6 Variations of D-FF, BISER FF and BCDMR FF by Monte-Carlo simulations of 10,000 ROs.

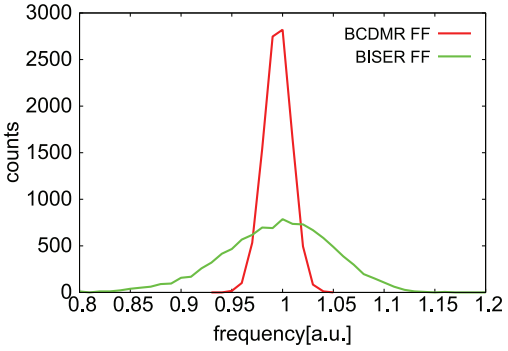

Fig. 7 Variations of BCDMR and BISER to fluctuate V_{th} of transistors in C-elements and weak keepers.

sistors are fluctuated according to a normal distribution. We assume that the standard deviation σ of V_{th} is 20% of σ defined in the SPICE parameter. Note that the value of 20% is derived to fit simulation results to measurement results of BCDMR shown later in Sect. 4.2. The standard deviation of BCDMR, σ_{BCDMR} normalized by the average oscillation frequency μ_{BCDMR} is 1.74% which is almost same as 1.75% of the ordinary D-FF, while that of BISER $\sigma_{BISER}/\mu_{BISER}$ is 1.93%. Figure 7 shows distributions from Monte Carlo simulations, in which only threshold voltages of the C-elements and weak keepers are fluctuated. The standard deviations normalized by the average oscillation frequency of BCDMR and BISER are 1.31% and 4.08% respectively. It clarifies that the device variations on the C-elements and weak keepers are dominant factors of performance fluctuations on the BISER structure, while they are not dominant in the BCDMR.

3. Shift-Register-Based Test Structure to Measure Process Variations

In order to measure variations of the BISER and BCDMR FFs, we have fabricated a test chip in a 65-nm bulk CMOS process including a large number of ring oscillators (ROs) implemented with these redundant FFs. This section shows the structure of the test chip and compares it with conventional structures to measure variations using ROs.

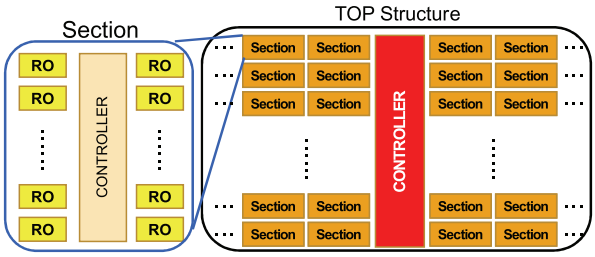

Fig. 8 Conventional matrix-array-based (MAB) test structure.

3.1 Conventional Matrix-Array-Based (MAB) Test Structure

ROs are widely used to measure variations of logic gates. [7] proposes a matrix-array-based (MAB) test structure to measure variations of ROs. [8] proposes another test structure based on the equivalent MAB structure. In the MAB structure, one of ROs is chosen by an address for oscillation. The oscillated waveform is fed to a counter. Variations can be measured by counting the oscillations of ROs on a chip in a fixed period. ROs generally consists of odd prime number of inverters or logic gates, which oscillates several GHz in a recent sub-nanometer process. The counter must be placed close to each RO to count such GHz-waveforms correctly. But its area penalty is very huge. Alternatively, dividers are placed before a shared counter to reduce oscillation frequency. Dividers are also indispensable to suppress noise. If such a high-frequency signal propagates through a chip, large amount of noise are generated to prevent correct measurement. In addition to that, the shared controller and peripheral circuits must be carefully designed to guarantee the correct functionality under such a high-frequency operation. Conventional MAB structures consist of arrays of ROs with local dividers and a shared counter. Figure 8 shows the MAB test structure in [7]. Local controllers in sections contain local dividers and a global controller includes a shared counter.

3.2 Shift-Register-Based (SRB) Test Structure

Figure 9 shows a conceptual block diagram of the proposed shift-register-based (SRB) test structure. It is a serially-connected shift register with ROs. A unit structure consists of an RO and a 1-bit counter which also works as a shift register. An oscillated waveform is counted by serially-connected n-bit counters. In Fig. 9, oscillated waveforms are stored in 4-bit counters. First, RO0 oscillates while a 4-bit counter implemented with COUNTER[3-0] is counting the oscillation. Then RO4 and COUNTER[7-4] are working. Counters in the blue polygons store the counts of RO0 and RO4. Finally, the counted values are obtained by shift operations. Then RO1 oscillates while COUNTER[4-1] is counting. Counters in the green polygons store the counts of RO1 and RO5. The SRB test structure has the following advantages compared with the conventional MAB ones.

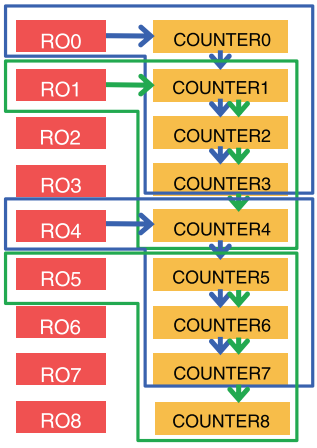

Fig. 9 Conceptual block diagram of the shift-register-based test structure. Oscillating waveform of RO1 is captured by COUNTER[3-0].

Table 1 Advantages and disadvantages of the conventional matrix-array-based (MAB) and proposed shift-register-based (SRB) test structures.

	MAB	SRB
# of IO pins	$\propto \log(N_{RO})$	Constant
if N_{RO}==100	7 pins	6 pins
if N_{RO}==40k	13 pins	6 pins
Measurement Time	Slow	Fast
if N_{RO}==40k	41.9 sec.	1.32 sec.
Whole structure	Heterogeneous with N_{RO}	Homogeneous
Area overhead	Small	Moderate
Area/bit	67.4 μmm^2	81.0 μmm^2
Observability	Good	Bad

Constant pin count The MAB test structure must have address pins to choose the oscillated RO. The number of pins are increased by the number of ROs (N_{RO}). On the other hand, the proposed SRB structure has constant pin count since all control and data signals can be serially connected.

Fast measurement time Counters can be placed very close to ROs, which reduces the measurement time. In the MAB structure of [7], a shared counter counts oscillation waveforms divided by 64, while the counters in our SRB structure stores oscillation waveforms divided by two. It suggests that the measurement time of our structure is 32x faster than that of the conventional MAB structure.

Table 1 summarizes advantages and disadvantages of the conventional MAB and proposed SRB test structures. The proposed structure is homogeneous since all components are serially-connected, while the MAB is heterogeneous by N_{RO} since the structure of the address decoder depends on N_{RO}. But the MAB has good observability. The divided oscillating waveforms in all ROs of the MAB can be exported outside a chip, while only ROs located in the tail of the shift register can be observed in the proposed SRB structure. One of disadvantages of the SRB test structure is area penalty since counters must be placed closely to each RO to correctly count waveforms oscillated in several GHz.

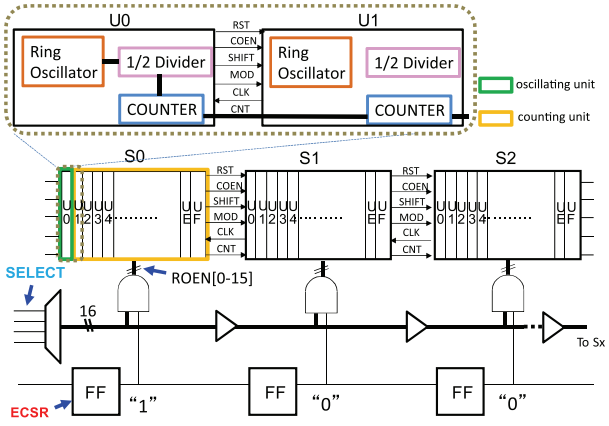

Fig. 10 Block diagram of the shift-register-based test structure.

In the proposed structure, however, each RO just has a 1-bit counter. The adjacent serially-connected counters form multiple-bit counters. Its area penalty is reduced by such shared structure. In the fabricated chip, the area of the section including 16 ROs is 1296 μm^2. The area per unit (RO) becomes 81.0 μm^2. Note that the cell area of the BCDMR-RO is 23.7 μm^2. In the MAB structure, the area per RO becomes 67.4 μm^2 which consists of 23.7 μm^2 of the RO, 16.7 μm^2 of a local divider and 26.9 μm^2 of address decoders and controllers. Thus the area of the proposed SRB structure is 28.9% larger than the conventional MAB structure.

Another drawback of the proposed circuit is the measurement time due to the serially-connected control signals. But it is not dominant. We inserted a buffer between sections for all the serially-connected control signals. Thus the number of buffers is 1/16 of ROs. In the implemented chip shown later in Sect. 4.1, the number of ROs and buffers are about 40k and 2,500 respectively. It takes approximately 100 ns for a control signal to propagate through all sections that enables 100 ns cycle time for measurement. The number of cycles is 11 to complete the measurement of an RO. The total required time to control units and sections are 44 ms for 40k ROs. The measurement time in Table 1 consists of the time for oscillation and controls but does not include the time to read the counter values. It is because the counter values are exported outside the chip by shift operations in the conventional MAB and the proposed SRB structures. The required exporting time are almost same in the both structures.

Figure 10 shows the block diagram of the SRB test structure to measure variations of ROs. A section indicated as S0, S1, S2 consists of 16-bit unit cells to measure variations in a 16-bit resolution. The bottom ENABLE-CONTROLL shift register (ECSR) and the 4-bit SELECT signal specify the section and the oscillated RO respectively. A unit cell is composed of an RO, a 1/2 divider and a 1-bit counter.

The measurement procedure is as follows. First, the head bit of ECSR is set as one, while the other bits are set as zero. SELECT becomes zero (4'b0000) to oscillate the unit

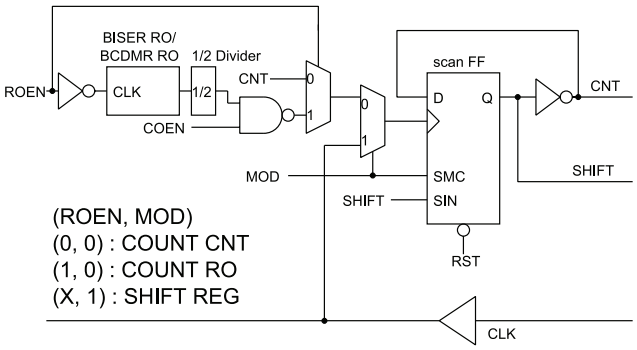

Fig. 11 Schematic diagram of the unit including an RO, a counter and its three functionalities.

cell U0. All 16 counters in the first section S0 forms a 16-bit counter to count the oscillated waveform. After counting it in a fixed period, the 16-bit counter in S0 stores number of counts. Then, ECSR is shifted as 1-bit to oscillate U0 in S1. The 16-bit counter in S1 count the oscillation. All 16-bit counters in all sections store counted values of the first ROs U0 by shifting ECSR from head to tail. All the measured counter values are obtained to shift the counter values. To measure the oscillation of U1, SELECT becomes one (4'b0001). The oscillated waveform of U1 in S0 is captured by U1, U2,... UF in S0 and U0 in S1. These 16-bit unit cells in the cascaded two adjacent sections capture the waveform. Note that U0 in S1 works as one-bit counter because ROEN is not active. By changing SELECT from 0(4'b0000) to 15(4'b1111), all unit cells in all sections can be measured.

Figure 11 shows the detailed schematic of the unit composed of an RO, scan FFs, muxs and other logic gates. All signals including the clock signal CLK except for ROEN are connected in series. These serially-connected signals except for CLK of the scan FF is given from the head of the shift register, while CLK is given from the tail of the shift register to relieve tight hold constraints of shift registers. Note that such clock distribution does not make the measurement time slower since the tail bit of the shift register is connected to the head of the clock chain. The value stored in the tail bit of the shift register can be obtained within very short delay time after the rising edge of the clock signal. In our experiments by the fabricated chip shown in the following section, the clock frequency is 10 MHz on the shift operation of ECSR. It has three functionalities by changing the control signals ROEN and MOD. When U0 is oscillating, (ROEN,MOD) is (1,0) in U0 and (0,0) in the other unit (U1-UF). When shifting the counted values, (ROEN,MOD) becomes (X,1) in all units.

4. Experimental Results

This section gives the overview of the fabricated chip and experimental results of variations obtained from measurements by a commercial engineering LSI tester.

Table 2 Specification of the fabricated chip.

Process	65 nm bulk CMOS
Chip Size	4mm×4mm
# of ROs	9856×4
# of Trs. in 4 seg.	3.66M
Package	QFP208

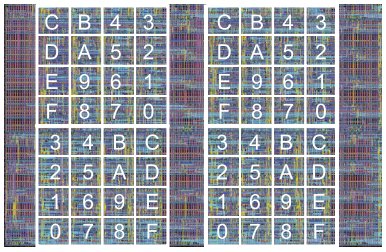

Fig. 12 Layout pattern of the 2×2 units.

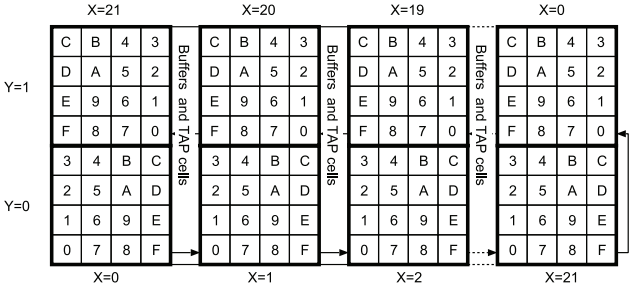

Fig. 13 Detailed layout structure of the sections and units.

4.1 Chip Overview

Table 2 shows a specification of the fabricated chip. We implemented four segments, each of which contains 9,854 ROs. These four segments are connected in series with the proposed shift-register-based structure. The first segment has ROs with BCDMR FFs and the second one has ROs with BISER FFs. These two are on the twin-well structure in which PMOS transistors (trs.) are on N-well, while NMOS trs. are on P-bulk. The lower two segments are equivalent to the upper two, but they are on the triple-well in which both PMOS and NMOS trs. are on N-well and P-well respectively.

Figures 12 and 13 show the detailed layout and floorplan of the section in the thick rectangles and units in the thin small rectangles. All units in each section meet the constraints that adjacent units are placed as close as possible to correctly count oscillations. Buffers for clock and other control signals and TAP cells to stabilize well and bulk potential are placed between units. Each segment includes 616 ($= 22 \times 28$) sections and 9856 ($= 616 \times 16$) units.

4.2 Measurement Results

We have measured variations of 21 chips by a commercial

Table 3 Measurement results of variations. μ and σ denote the average and the standard deviation of the oscillation frequency, respectively.

FF	Well	μ(GHz)	σ (GHz)	σ/μ
BISER	twin	1.80	0.0438	2.43%
	triple	1.82	0.0554	3.05%
BCDMR	twin	2.07	0.0375	1.81%
	triple	2.12	0.0356	1.68%

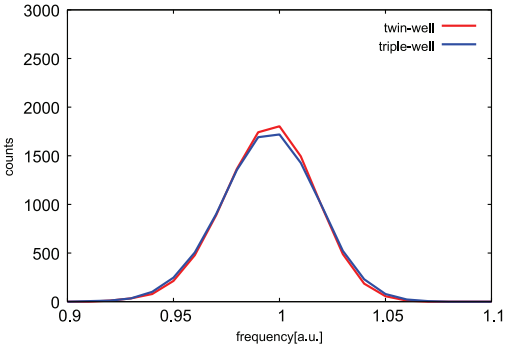

Fig. 14 Distributions of variations of BISER FF.

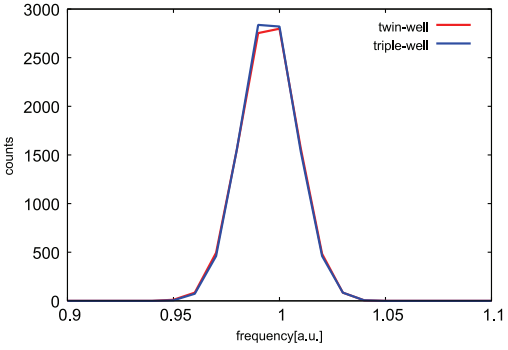

Fig. 15 Distributions of variations of BCDMR FF.

LSI tester. Table 3 shows measurement results of variations at the nominal operating conditions (VDD = 1.2 V). Figures 14 and 15 are the distributions of measured frequency.

As for the average oscillating frequency (μ), ROs in triple-well is about 1% faster than in twin well. It is assumed that the different process flows between twin and triple-well produce differences of impurity density. As for the standard deviation (σ), the measured tendencies are different between BISER and BCDMR. In BISER FF, σ/μ on triple-well is larger than that on twin-well, while in BCDMR FF σ/μ on triple-well is smaller. In twin-well, σ/μ of BCDMR FF are 74% and 55% smaller than those of BCDMR FF on twin-well and triple-well respectively. It can be assumed that the instability of well potential on triple-well degrades the variation of BISER because of its asymmetric structure.

5. Conclusion

This paper declares that the error-hardened dual-modular-redundancy FF called the BCDMR FF is not only stronger against soft error but also more variation-tolerant than the conventional BISER FF. We also propose a shift-register-based test structure to measure variations of the BCDMR FFs. Variations are measured with a ring oscillator implemented by the BCDMR and BISER FFs. The proposed shift-register-based test structure has features of constant pin count and fast measurement time. We have fabricated a 65-nm test chip including 40k ring oscillators to measure variations of BCDMR FFs and conventional BISER FFs. Measurement results shows that the variations of BCDMR FF are 74% and 55% smaller than those of the conventional BISER FF on twin-well and the triple-well structures respectively. Variation-tolerance is one of most important factors for commercial products. Simulation results show that the BCDMR FF has the standard deviation equivalent to the ordinary D-FF, which means that the BCDMR structure has as good error resiliency as the D-FF has.

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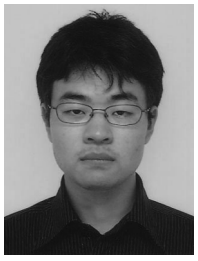

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