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An Area/Delay Efficient Dual-Modular Flip-Flop with Higher SEU/SET Immunity

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SUMMARY According to the process scaling, semiconductor devices are becoming more sensitive to soft errors since amount of critical charges are decreasing. In this paper, we propose an area/delay efficient dual modular flip-flop, which is tolerant to SEU (Single Event Upset) and SET (Single Event Transient). It is based on a "BISER" (Built-in Soft Error Resilience). The original BISER FF achieves small area but it is vulnerable to an SET pulse on C-elements. The proposed dual modular FF doubles C-elements and weak keepers between master and slave latches, which enhances SET immunity considerably with paying small area-delay product than the conventional delayed TMR FFs.

key words: *TMR, built-in soft error, SEU, SET*

1. Introduction

Process scaling makes LSIs less reliable to temporal and permanent failures. Temporal failures flip a stored value on SRAMs or flip flops. High-energy neutron is one of main sources of temporal failures, which is called a "soft error." Soft errors are classified into Single Event Upset (SEU) and Single Event Transient (SET). SEU is caused by a particle hit on sequential elements, and SET is caused by a particle hit on combinational circuits.

One of the solutions to remove soft errors is using dual interlocked storage cell latch (DICE latch) [1]. Since DICE latch have four storage nodes, it is very strong to SEU. However, it cannot protect errors from SET. Thus its soft-error tolerance is just 10 times stronger than ordinal FFs. To remove SET and mitigate more soft errors, redundant circuits are usually used. TMR (Triple modular redundancy) [2] is an ultimate solution for soft errors, in which all circuit elements are tripled and unmatched results are resolved by majority voting. It is very robust to soft errors since it does not fail until two modules fail at the same time, but its area penalty is relatively huge.

In this paper, we propose an area and delay efficient dual modular flip-flop, which is tolerant to SEU and SET. The proposed dual modular FF is based on the flip-flop with C-elements and weak keepers so called a "BISER" (Built-in Soft Error Resilience) [3]. The original BISER FF achieves small area but it is vulnerable to an SET pulse on C-elements. The proposed dual modular FF doubles C-elements and weak keepers between master and slave latches, which enhances SET immunity considerably with paying very small area overhead.

The remainder of this paper is organized as follows. In Sect. 2, we introduce conventional multiple modular flip flops and detailed structure of the proposed dual modular FFs. Section 3 describes how to estimate soft error rates of the flip flops by using circuit-level simulations. Section 4 examines area and delay penalties of the proposed and conventional redundant FFs for error resilience. Section 5 summarizes this paper.

2. Soft Error Tolerant Flip Flops

2.1 Dual Interlocked Storage Cell Latch

Figure 1 shows dual interlocked storage cell latch using transmission gate, so called "DICE latch." It has four storage nodes. Even if one storage node is flipped by SEU, other storage nodes keep correct values. However DICE latch can not keep correct value when two storage nodes are flipped by a particle hit, which situation is called Multi Cell Upset (MCU). While MCU may be happened to other redundant FFs. DICE latch has no tolerance to SET. Thus its tolerance to soft error is just 10 times better than ordinal non-redundant FFs.

2.2 Conventional Multiple-Modular FFs

Figure 2 shows a conventional TMR circuit (TMR_{conv}). The voter resolves stored values at latches. Voters must be tripled to avoid failure due to SET pulses from a voter itself.

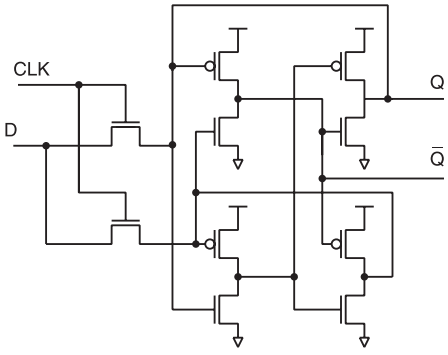

Fig. 1 Dual interlocked storage cell latch [1].

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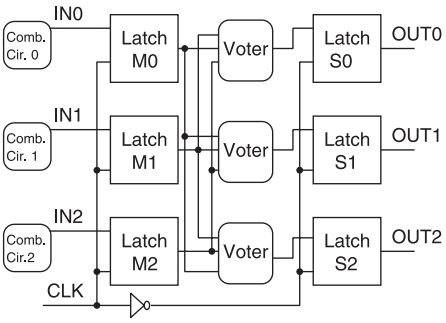

Fig. 2 Conventional TMR flip flop tolerant to temporal errors from combinational circuits and FFs (TMR_{conv}) [2].

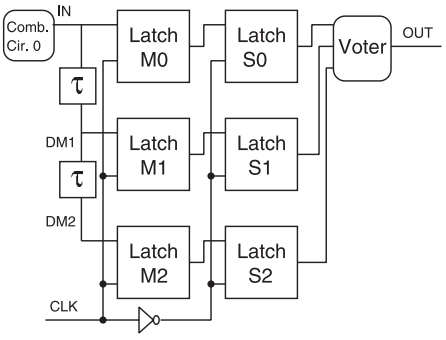

Fig. 3 Delayed-TMR flip flop tolerant to temporal errors from combinational circuits and FFs. (DTMR) [4].

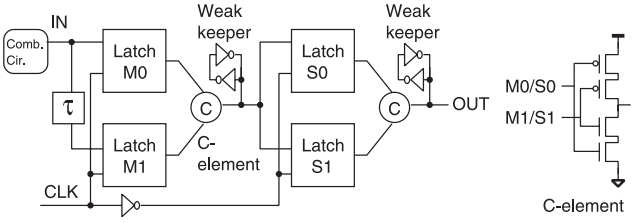

Fig. 4 Delayed-DMR flip flop (DDMR FF or BISER) using a delay element, C-elements and weak keepers to remove SETs and SEUs [3].

It shows tight robustness to soft errors from combinational circuits and FFs, but the area penalty should be huge. It is more than 3 times bigger than a non-redundant circuit.

Figure 3 is a delayed-TMR FF (DTMR) [4] tolerant to soft errors on combinational circuits, master and slave latches. Two delay elements denoted by τ prevent an SET pulse being captured by multiple latches. Temporal soft errors on latches can be resolved using the voter and delay elements. An SET pulse from the voter can be removed by the delay elements on the next stage. Thus a voter is placed after slave latches and have no redundancy.

Figure 4 is a delayed DMR (DDMR) FF using C-elements and weak keepers (BISER) [3]. A C-element and a weak keeper hold the current value if two input signals are different. It is also robust to an SET pulse from combinational circuits and also to an SEU on latches or weak keepers. But it is very weak against an SET pulse from C-elements. If an SET pulse is generated from a C-element

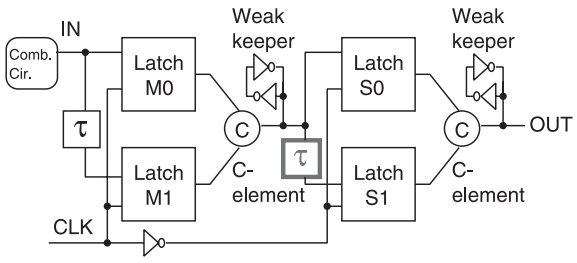

Fig. 5 A proposed DMR FF called Double-Delayed DMR FF.

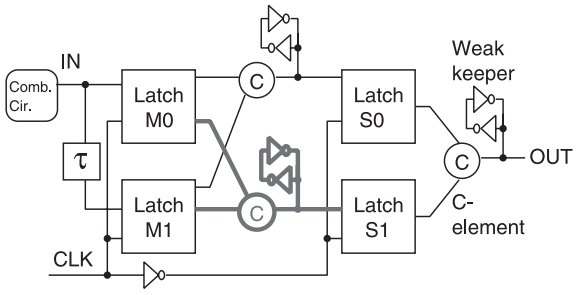

Fig. 6 Another proposed DMR FF called Enhanced delayed DMR FF.

before the slave latches, both of them capture the incorrect value caused by the SET pulse.

2.3 Proposed DMR Flip Flops Immune Against Soft Errors on C-Elements

As described in the previous section, the conventional BISER FF is not resilient to SET pulses on the C-element. We propose two modified structure to enhance SER immunity with small area and delay penalty. In order to avoid multiple flips on latches by an SET pulse from the C-element, one possible solution is to insert another delay element between the C-element and the redundant slave latch. The other solution adds another pair of the C-element and weak keeper between redundant master and slave latches.

Figure 5 shows one proposed structure called "Double-Delayed DMR FF (D^3MR FF)." To avoid multiple flips caused by an SET pulse from the C-element, an additional delay element is attached before the redundant slave latch. But the dual modular FF has a fundamental drawback to eliminate multiple flips by a delay element. It is because the weak keeper prolongs an SET pulse. When an SET pulse is generated at the input port of the slave latch, the weak keeper is flipped temporally. The feedback inverter in the weak keeper prevents the input port going back to its original state.

Figure 6 shows another proposed structure called "Enhanced delayed DMR FF (ED^2MR FF)." C-elements and weak keepers between master/slave latches are doubled to avoid simultaneous flips on slave latches. It achieves small area and delay penalties compared with D^3MR FF.

Details of the error resiliency, area and delay overhead of the proposed and conventional multiple-modular FFs are discussed in Sect. 4.

3. Soft Error Rates of FFs

Here we estimate amount of charge to flip latched in a DICE latch and multiple-modular FFs caused by a particle hit on latches, weak keepers and combinational circuits by circuit-level simulations and show analytical equations to compute SERs of soft error tolerant FFs.

3.1 Estimation of SERs by Critical Charge

In the terrestrial environment, high-energy neutrons are main sources of errors. A high-energy neutron injected to silicon produces a secondary charged particle. If it hits a silicon atom near a drain region, electrons or holes are collected to the drain region by drift and diffusion. We use the single-exponential model as in Eq. (1) [5], for transient current caused by the particle.

$$I(t) = Q\frac{2}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(\frac{-t}{T}\right) \quad (1)$$

where T is a time constant depending on a fabricated process and Q is a total charge collected to the drain region. Q_{crit} is defined as the minimum charge to flip a latch in FFs. After obtaining Q_{crit}, Eq. (2) from [6] is used to compute SERs.

$$N_{\mathrm{SER}}(Q_{\mathrm{crit}}) = F \times A \times K \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}\right) \quad (2)$$

where F is the high-energy neutron flux and A is the drain area of transistors related to soft errors. K is a fitting parameter. Q_{s} is called "charge collection efficiency" that is correspond to the sensitivity of the critical charge. Q_{s} strongly depends on doping and supply voltage [7]. We use the parameter values as in Table 1 obtained from [6] for a 100 nm process. But circuit simulations are done by 90 nm process parameters. We use three different T value, 10 ps, 20 ps and 30 ps, since T widely changes by process conditions. On the other hand, Q_{s} value is equivalent to that of the 100 nm process because Q_{s} is proportional to the process scaling instead of process conditions.

In our experiments, an ideal current source in Eq. (1) is attached to a circuit node to estimate the critical charge. Circuit-level simulations with a 90 nm process estimate amount of critical charge by adding the ideal current source on a node of a particle hit. We assume the following conditions to simply circuit simulations.

1. Particles hit on drain regions of only NMOS, not PMOS.
2. NMOS is always off so as to flip the inverter by the charges generated from the particle hits.

From the condition 1, we may underestimate the SER. The overall SER should be doubled in the CMOS circuits. But it can be said that the probability when NMOS is off is 50%. Therefore, the above assumption gives the reasonable SERs considering particle hits on both NMOS and PMOS.

Table 1 Parameters for SER estimation.

F	0.00565 $\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Q_{s}	13fC
K	2.2e-5
f	1 GHz
T	10–30 ps

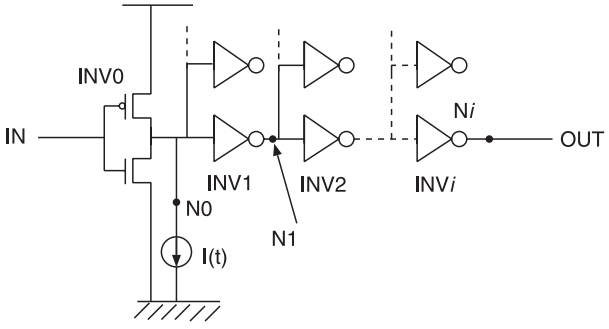

Fig. 7 Inverter chain with fanouts. A high-energy neutron hits to N0.

3.2 SER Caused by a Particle Hit on Combinational Circuits

Figure 7 shows a circuit structure to estimate SEUs caused by SET pulses from combinational circuits. We assume that a 11FO4 inverter chain is connected to an FF. Q_{crit} of logic gates cannot be estimated easily since operating circuits fail only when a generated transient pulse is latched. We have to consider these three masking effects to estimate SEUs caused by SET pulses from logic gates, electrical masking, latching window masking and logical masking [8]. Because of electrical masking, SET pulses are gradually attenuated after passing through the series of logic gates. Table 2 shows amount of required charge on N0 to generate an SET pulse at the output node of the 11FO4 inverter chain. The row of the "Minimum" means the required charge to generate a minimum pulse at the output node, while that of the "50 [ps]" means the required charge to generate a pulse continuing for 50 ps at the output node. By assigning each value of charge to Q_{crit} in Eq. (2), we can obtain the rate of the pulse above the width such as 50 ps, 75 ps, etc. After obtaining the charge tables for all nodes (N0-N10), the rate of the SET pulse above all widths in the table can be derived by accumulating the error rates of all nodes. Table 3 shows the rate of the SET pulse above the specified with (N_I) and the rate of the SET pulse between the specified width range (ΔN_I).

An SEU happens if an SET pulse is longer than the sum of setup and hold time of an FF called latching window. But the possibility to latch the SET pulse is varied according the the latching window time w and the clock period c. The total SER caused by the 11FO4 inverter on the non-redundant conventional FF is computed from Eq. (3) [8].

$$N_{\mathrm{I\ FF}} = \int_{w}^{c+w} \Delta N_{\mathrm{I}}(t)\frac{t-w}{c}dt \quad (3)$$

where $\Delta N_{\mathrm{I}}(t)$ denotes the rate of the SET pulse with the

Table 2 Amount of required charge at N0 to generate an SET pulse at the output node of the 11FO4 inverter chain.

Pulse Width [ps]	Q[fC]					
	N0	N2	N4	N6	N8	N10
Minimum	11.0	16.9	18.1	18.5	18.9	19.0
50	15.5	17.8	18.4	18.7	19.0	19.2
75	20.8	19.5	19.7	20.0	20.2	20.3
100	39.1	24.7	24.6	24.7	24.8	25.2
125	104	44.6	44.2	43.9	43.2	44.6
150	306	107	101	100	101	106
175	941	296	287	287	288	294
200	NA	897	881	862	879	927

Table 3 Rate of the SET pulse according to the pulse width.

Pulse Width [ps]	N_I[FIT]	PW Range[ps]	ΔN_I[FIT]
Min.	1.697e-03		
<50	1.568e-03	Min~50	1.290e-04
>75	1.360e-03	50~75	2.080e-04
>100	8.533e-04	75~100	2.080e-04
>125	1.722e-04	100~125	5.067e-04
>150	1.477e-06	125~150	1.710e-04
>175	7.497e-13	150~175	1.477e-06
>200	1.467e-32	175~200	7.497e-13

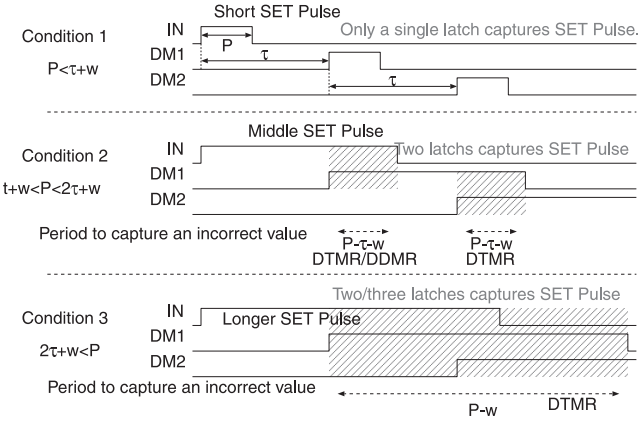

Fig. 8 Filtering a SET pulse by delay elements.

pulse width t, which value can be complemented from ΔN_I in Table 3. The SER caused by the 11FO4 inverter on DICE latch is also computed from Eq. (3) because of having no mitigation to SET pulse.

A delay element before redundant master latches prevents to flip multiple latches by an SET pulse. Suppose that the width of an SET pulse is P and $P < c$. Figure 8 explains three conditions in the case of DDMR and DTMR flip flops. A delay element with τ delay time prevents multiple flip flops to capture an incorrect value caused by an SET pulse shorter than $\tau + w$ (Condition 1). When $\tau + w < P < 2\tau + w$, multiple FFs may capture an incorrect value for $(P - \tau - w)$ within a clock cycle (Condition 2). The latching window appears once in DDMR and twice in DTMR. When $P > 2\tau + w$, the period to capture an incorrect value becomes $P - w$ only in DTMR (Condition 3).

By considering the above three conditions, error rates

Table 4 SER in FIT/bit of a 11FO4 inverter chain according to τ of delay elements.

T(ps)→	10ps		20ps		30ps	
τ(ps)↓	DMR	TMR	DMR	TMR	DMR	TMR
0	9.3e-5		1.0e-4		9.7e-5	
50	2.6e-6	5.1e-6	2.7e-5	5.3e-5	3.8e-5	7.3e-5
75	6.5e-16	1.3e-15	5.0e-6	1.0e-5	1.5e-5	3.0e-5
100	0	0	5.3e-8	1.1e-7	3.2e-6	6.5e-6

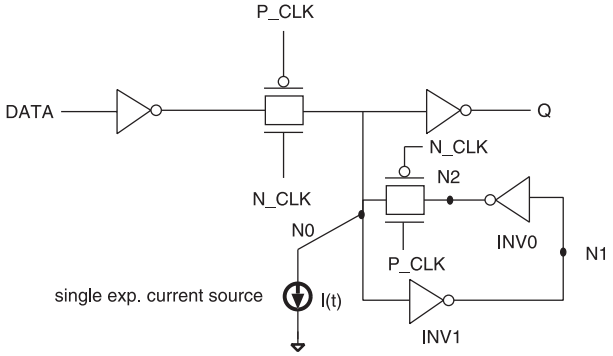

Fig. 9 A Latch circuit diagram. A high-energy neutron hits to N0, 1 or 2 to flip the stored value of the latch.

of the delayed FFs are expressed as follows.

$$N_{\mathrm{I\ DTMR}} = 2\int_{\tau+w}^{2\tau+w} \Delta N_{\mathrm{I}}(t)\frac{t-\tau-w}{c}dt + \int_{2\tau+w}^{c+w} \Delta N_{\mathrm{I}}(t)\frac{t-w}{c}dt \quad (4)$$

$$N_{\mathrm{I\ DDMR}} = N_{\mathrm{I\ D^3MR}} = N_{\mathrm{I\ ED^2MR}} = \int_{\tau+w}^{2\tau+w} \Delta N_{\mathrm{I}}(t)\frac{t-\tau-w}{c}dt \quad (5)$$

Table 4 shows SER of a 11F04 inverter chain computed from Eqs. (4), (5). It is exponentially reduced by τ of the delay element.

3.3 SER Caused by a Particle Hit on Latches

A latch in Fig. 9 is used for simulations. If CLK is 0, DATA drives all inverters and CMOS switches in the latch. Therefore, SEUs at CLK=0 can be ignored and the possibility of SEUs in latches is almost halved. The total SER of a latch is expressed as in Eq. (6)

$$N_{\mathrm{L}} = \frac{1}{2}\sum_{i=0}^{2} N_{\mathrm{SER}}(Q_{\mathrm{cL}i}) \quad (6)$$

where $Q_{\mathrm{cL0}}, Q_{\mathrm{cL1}}, Q_{\mathrm{cL2}}$ are the critical charges to flip the latch caused by particle hits at N0, 1, 2 respectively. In the case of the DICE latch, the total SER is described as in Eq. (7).

$$N_{\mathrm{D}} = \frac{1}{2}\sum_{i=0}^{3} N_{\mathrm{SER}}(Q_{\mathrm{cD}i}) \quad (7)$$

Q_{cDi} indicate the critical charges of four storage nodes. Table 5 shows SERs in FIT/bit of latch and DICE latch. Compared with latch, DICE latch is very strong to SEU in our simulation results.

In the delayed TMR circuit, even if one latch flipped by a particle hit, it keeps correct value by a voter. However, if two or three latches are flipped by particle hits during a clock cycle, it cannot keep correct value. Hereafter, we call the error in which an FF is flipped to the wrong state as "critical error." For example, it is a critical error when two master/slave latches are flipped in the TMR FFs. The SER caused by SEUs on latches ($N_{\mathrm{L\ DTMR}}$) is described as in Eq. (8).

$$\begin{aligned} N_{\mathrm{L\ DTMR}} &= 3 \times N_{\mathrm{L}}^2 - N_{\mathrm{L}}^3 \\ &\simeq 3 \times N_{\mathrm{L}}^2 \end{aligned} \tag{8}$$

Figure 10 shows how to estimate SER of the DDMR FF. The bottom two lines in Table 5 are SERs of a weak keeper and a C-element. SER of the weak keeper is the sum of SERs caused by particles on N3-5. If there is no error on the two master latches, N4 is strongly driven by the inverter. But when one of master latches is flipped, N4 is floating. In that case, a particle hit on N3 flips the state of the weak keeper and causes critical error. The SER values in Table 5 is estimated considering these floating state. SER of the C-element is defined as the SER in which two slave latches are flipped by an SET pulse from the C-element. As shown in Table 5, SERs of the weak keeper and C-element are close to that of the latch. An SEU on a weak keeper can be recovered by the C-element. On the other hand, simultaneous SEUs on the two slave latches caused by SET pulses on the C-element always become critical errors. The total SER of the DDMR FF caused by a particle hit on latches, weak keepers and C-elements can be expressed as follows.

$$N_{\mathrm{L\ DDMR}} \simeq N_{\mathrm{L}}^2 + 2N_{\mathrm{L}}N_{\mathrm{W}} + N_{\mathrm{C}} \tag{9}$$

Table 5 SERs in FIT/bit of a latch, weak keeper and C-element.

T	10 ps	20 ps	30 ps
Latch (N_{L})	3.4e-4	3.3e-4	3.1e-4
DICE latch (N_{D})	NO ERROR	NO ERROR	4.1e-37
Weak Keeper (N_{W})	2.4e-4	3.8e-4	3.5e-4
C-element (N_{C})	1.9e-5	2.7e-5	3.0e-5

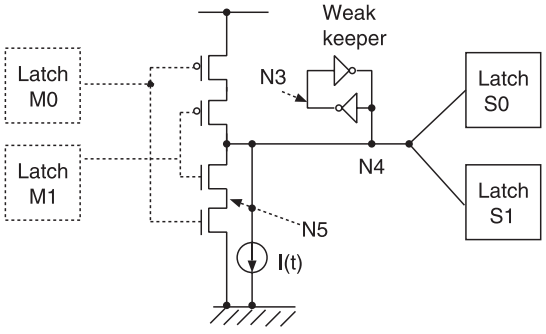

Fig. 10 Estimation of SER of weak keeper and C-element. High-energy neutron on N3-5 may flip a weak keeper and two slave latches.

$$N_{\mathrm{C}} = \int_{w}^{c+w} \Delta N_{\mathrm{C}}(t) \frac{t-w}{c} dt \tag{10}$$

where $\Delta N_{\mathrm{C}}(t)$ denotes the rate of the SET pulse on the C-element with the pulse width t. As shown in Eq. (9), the SER of the DDMR does not become small because of the SER of the C-element (N_{C}). These simultaneous SEUs on the slave latches should be eliminated to decrease the error rate. In the case of our proposed DMR FFs, N_{C} is eliminated by delay element or doubled C-element and expressed as follows.

$$N_{\mathrm{C\ D^3MR}} = \int_{\tau+w}^{2\tau+w} \Delta N_{\mathrm{C}}(t) \frac{t-\tau-w}{c} dt \tag{11}$$

$$N_{\mathrm{C\ ED^2MR}} = (N_{\mathrm{C}})^2 \tag{12}$$

Compared with DDMR, D^{3}MR FF and ED^{2}MR FF achieves relatively small SER.

4. Simulation Results

4.1 Total SERs of the Conventional Redundant FFs

From Eqs. (3)–(12), we can compute the total soft error rates considering SEUs caused by a particle hit on FFs or inverter chains connected to them. Table 6 shows the total SERs of DICE latch and redundant FFs with the 11FO4 inverter chain at their input ports. We assume three time constant (T) values from 10 ps to 30 ps. Since DICE lath can not mitigate SET, its soft-error tolerance is just 10 times stronger than ordinal FF. This result show that SET mitigation is necessary to achieve higher soft error tolerance.

Figures 11–13 show the total SERs of multiple-modular FFs and proposed FFs from delay value τ=0 ps to τ=200 ps. If a sufficient value of τ is selected, DTMR FF, D^{3}MR FF and ED^{2}MR FF achieve SERs almost equivalent to conventional TMR FF which triples all circuit components. However, the SER of the DDMR FF is 1/20–1/40 of the ordinal non-redundant FF. It is because the SER by the C-element is relatively high as described in Eq. (9). SERs of delayed FFs are decreasing according to τ. We choose the values of τ to saturate the SER to the minimum values.

Table 6 SERs of conventional redundant FFs.

	T=10 ps	T=20 ps	T=30 ps
Ordinal FF	7.7e-04	7.5e-04	7.1e-04
DICE latch	9.3e-05	1.0e-04	9.7e-5
TMR FF	3.8e-28	3.5e-28	3.2e-28
DTMR FF (τ)	3.8e-28 (100 ps)	3.5e-28 (150 ps)	1.3e-26 (200 ps)
DDMR FF (τ)	1.9e-05 (75 ps)	2.7e-05 (100 ps)	3.0e-05 (125 ps)
D^{3}MR FF (τ)	4.4e-28 (100 ps)	3.9e-28 (150 ps)	6.5e-27 (250 ps)
ED^{2}MR FF (τ)	4.4e-28 (100 ps)	3.9e-28 (150 ps)	6.5e-27 (200 ps)

4.2 Area and Delay Overhead of the Proposed Dual Modular FFs

Table 7 and Fig. 14 shows area, delay and power consumption of the proposed DMR FFs and the DTMR FF normalized by those of conventional non-redundant FF. Note that the τ is chosen to make the SER is less than 1e-7 FIT. In the error rate of 1e-7 FIT, one million high-end processors including 120 thousand FFs keep on working for one year. Note that an 11FO4 inverter chain is attached to each FF to simplify the SER estimation. It may be relatively low error rate. But when 1000 processor cores embedded in a workstation, one Million processors are equivalent to 1000 workstations. The area is computed to sum up areas of latches, inverters for delay elements, voters and C-elements implemented in standard cells. The delay and power consumption are estimated by circuit-level simulations using a 90 nm process parameter. Delay is defined as the minimum transition time from D (FF input) to Q (FF output). Power is defined as

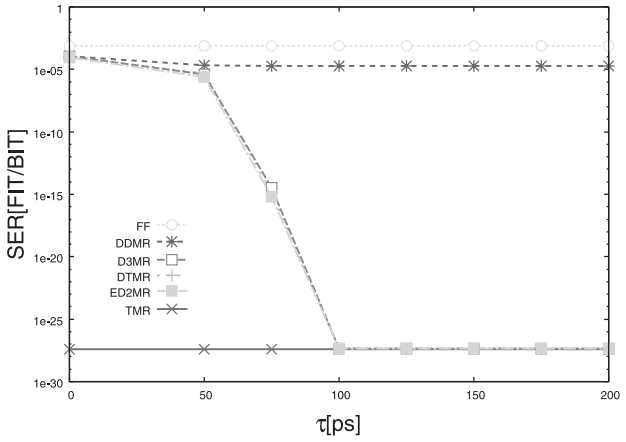

Fig. 11 Total SERs of multiple-modular FFs and proposed FFs at T=10 ps.

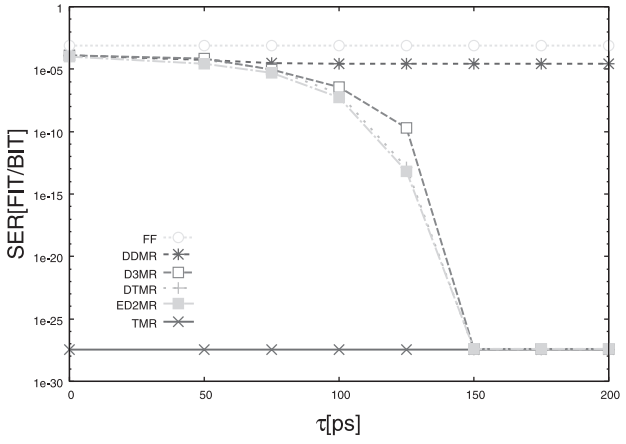

Fig. 12 Total SERs of multiple-modular FFs and proposed FFs at T=20 ps.

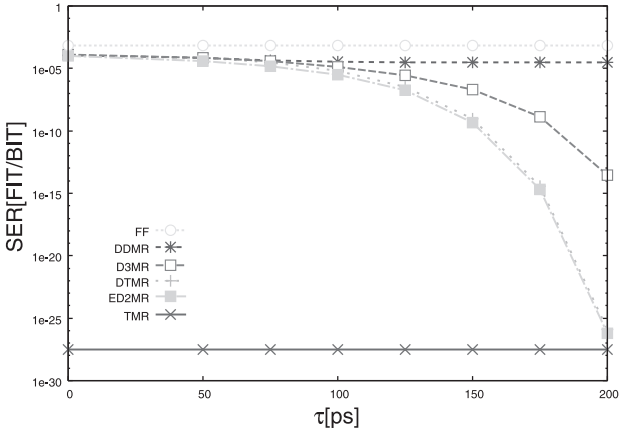

Fig. 13 Total SERs of multiple-modular FFs and proposed FFs at T=30 ps.

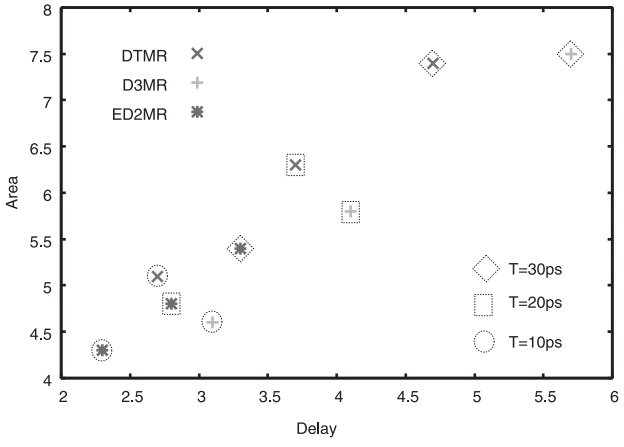

Fig. 14 Area and delay of the conventional and proposed FFs normalized by those of the conventional non-redundant FF.

Table 7 Area, delay and power consumption of the proposed DMR and DTMR FFs normalized by those of conventional non-redundant FF. (τ is chosen to make the SER <1e-7)

	T=10 ps					T=20 ps					T=30 ps				
	τ	Area	Delay	ADP*	Power	τ	A	D	ADP	P	τ	A	D	ADP	P
DTMR FF	75 ps	5.1	2.7	13.8	4.9	100 ps	5.7	3.2	18.2	5.4	125 ps	6.3	3.7	23.3	5.9
D^3MR FF	75 ps	4.6	3.1	14.2	4.2	100 ps	5.2	3.6	18.7	4.7	150 ps	6.4	4.6	29.4	5.8
ED^2MR FF	75 ps	4.3	2.3	9.9	3.8	100 ps	4.6	2.6	12.0	4.0	125 ps	4.8	2.8	13.4	4.3

ADP: Area-Delay Product

maximum dynamic consumption at 1 GHz clock frequency. As shown in Table 7, all delay values are over 2 times larger than the conventional non-redundant FF, which is mainly because the delay elements prolong the delay time of redundant latches. For all T values from 10 ps to 30 ps, ED^{2}MR FF shows smallest area-delay product (ADP). For T=30 ps, ED^{2}MR FF achieves 13.4 ADP which is 58% of the DTMR FF and 46% of the D^{3}MR FF respectively. ED^{2}MR FF also shows smallest power consumption. For T=30 ps, ED^{2}MR FF consumes 4.3X compared with non-redundant FF which is 73% of the DTMR FF and 74% of the D^{3}MR FF respectively.

5. Conclusion

In this paper, we estimate the SERs of DICE latch and conventional redundant flip-flops to eliminate soft errors on LSIs. Since DICE lath can not mitigate SET, its soft-error tolerance is 10 times stronger than ordinal FF. On the other hand, it is revealed that so-called "BISER" FF is very weak to soft errors and cannot achieve over 50 times stronger soft-error tolerance since a particle hit on the C-element can flip the two slave latches simultaneously with high possibility. In order to mitigate errors caused by the C-element, we propose two structures modified from the original BISER FF. One structure called "ED^{2}MR (Enhanced Dual Modular Redundancy) FF" achieves SERs almost equivalent to delayed TMR FF by doubling C-elements and weak keepers between master/slave latches. It achieves 76% area, 76% delay, 73% power consumption and 58% Area-Delay product of the delayed TMR FF on the lower soft error rate below 1e-7FIT/bit.

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