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A Low-Power Radiation-Hardened Flip-Flop with Stacked Transistors in a 65 nm FDSOI Process

Haruki MARUOKA[†a)], **Masashi HIFUMI**[†], ***Nonmembers***, **Jun FURUTA**[†], ***and*** **Kazutoshi KOBAYASHI**[†], ***Members***

SUMMARY We propose a radiation-hardened Flip-Flop (FF) with stacked transistors based on the Adaptive Coupling Flip-Flop (ACFF) with low power consumption in a 65 nm FDSOI process. The slave latch in ACFF is much weaker against soft errors than the master latch. We design several FFs with stacked transistors in the master or slave latches to mitigate soft errors. We investigate radiation hardness of the proposed FFs by α particle and neutron irradiation tests. The proposed FFs have higher radiation hardness than a conventional DFF and ACFF. Neutron irradiation and α particle tests revealed no error in the proposed AC Slave-Stacked FF (AC_SS FF) which has stacked transistors only in the slave latch. We also investigate radiation hardness of the proposed FFs by heavy ion irradiation. The proposed FFs maintain higher radiation hardness up to 40 MeV-cm^2/mg than the conventional DFF. Stacked inverters become more sensitive to soft errors by increasing tilt angles. AC_SS FF achieves higher radiation hardness than ACFF with the performance equivalent to that of ACFF.

key words: *single event effect, soft error, α particle, neutron, heavy ion, FDSOI, flip-flop, low-power consumption*

1. Introduction

The continuous downscaling of transistors has resulted in an increase of reliability issues for semiconductor chips. Soft Error Rate (SER) per chip has increased with technology scaling [1]. Soft errors are caused by α-particles from package and neutrons from cosmic ray in the terrestrial region. Electron-hole pairs are generated along a radiation track. The radiation-induced charge is collected to drain region. Single Event Upset (SEU) is a phenomenon that stored value in Flip-Flops (FFs) or SRAMs are upset by radiation effect. By rebooting devices, erroneous values are restored. Highly-reliable devices for high performance computing and aerospace need to mitigate soft errors. Redundant FFs have been proposed to mitigate soft errors. The triple modular redundancy (TMR) FF [2] resolves the stored values by majority voting. It has two delay elements to prevent capturing a single event transient (SET) pulse to multiple latches. Built-in soft error resilience (BISER) [3] has doubled latches, C-elements and weak keepers to mitigate soft errors. However, it is weak against a C-element-induced SET pulse. Bistable cross-coupling dual modular redundancy (BCDMR) [4] has been proposed based on BISER. C-elements and weak keepers between master latches (ML) and slave latches (SL) are doubled to mitigate a C-element-induced SET pulse. Compared with these majority-voting-based structure, dual interlocked storage cell (DICE) [5] structure achieves lower area overhead with soft error resilience. It has four storage nodes to keep values in ML and SL. But, it has no tolerance to a SET pulse. Redundant FFs have a small timing overhead, but it has larger area and power overheads than standard FFs. There is a trade-off between area overhead and radiation hardness. Therefore, FFs which have lower overheads and radiation hardness are indispensable.

Fully-Depleted Silicon On Insulator (FDSOI) processes decrease SERs without any performance overheads. Since FDSOI processes have smaller threshold voltage variations than bulk processes due to its undoped channel, they operate at lower supply voltage. In addition, transistors in FDSOI processes have a smaller charge collection volume than bulk processes because a buried oxide (BOX) layer prevent charge collection. Thus, they also have 50-110x higher soft error tolerance without any circuit level mitigation techniques [6].

In this paper, we propose radiation-hardened FFs with lower overhead fabricated in a 65 nm FDSOI process. We carried out α particle and neutron irradiation measurements to investigate the radiation hardness of the proposed FFs in the terrestrial region. We also performed heavy ion measurements, including the effect on incident angle for outer space usage.

2. Low-Power Radiation-Hardened Flip-Flop

2.1 Unhardened Standard Flip-Flops

Figure 1 shows a conventional DFF (TGFF). Weak transistors by a radiation particle hit depend on DATA and CLK states. When (DATA, CLK) = (0, 0) and (1, 1), the inverters are vulnerable. When (DATA, CLK) = (0, 1) and (1, 0), the tri-state inverters are vulnerable.

The Adaptive Coupling Flip-Flop (ACFF) [7] has pass transistors instead of transmission gates or tri-state inverters as shown in Fig. 2. ACFF has no local clock buffer for $\overline{\text{CLK}}$ which consumes large amount of power. Thus it consumes less power than TGFF. ACFF has AC elements, in which PMOS and NMOS are connected in parallel to easily overwrite the stored value in ML. When CLK = 0, a stored value

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[†]The authors are with Graduate School of Science and Technology, Kyoto Institute of Technology, Kyoto-shi, 606–8585 Japan.
a) E-mail: hmaruoka@vlsi.es.kit.ac.jp

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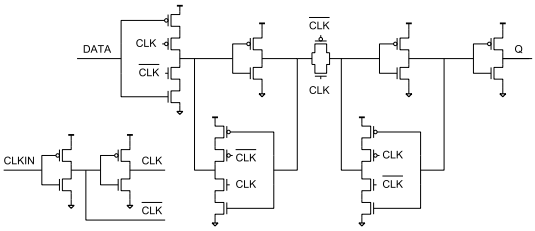


Fig. 1 Conventional transmission-gate FF (TGFF).

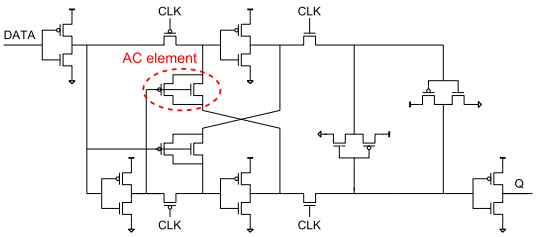


Fig. 2 Adaptive Coupling FF (ACFF) [7].

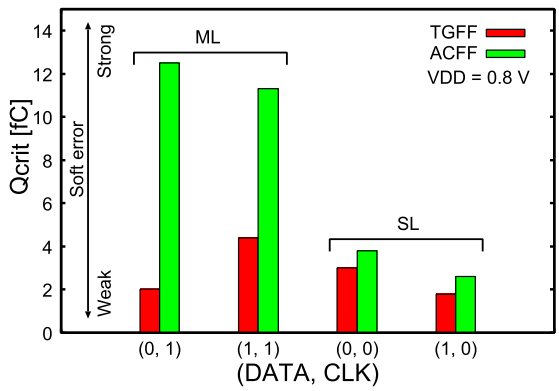


Fig. 3 Q_{crit} simulation results at 0.8 V depending on DATA and CLK state. Master Latch (ML) and Slave Latch (SL) are sensitive to soft errors when CLK is 1 and 0 respectively.

is transferred to SL. When CLK = 1, stored values in ML and SL are equivalent.

Radiation hardness is evaluated by critical charge (Q_{crit}) with SPICE simulations [8]. We determine the minimum injected charge as Q_{crit} to flip stored value. We connected a current source to a circuit node to estimate the Q_{crit}, which follows the single exponential model [9] with the time constant of 10 ps. Figure 3 shows the simulation results at 0.8 V depending on DATA and CLK states. When CLK = 0, Q_{crit} of ACFF is similar to that of TGFF. On the other hand, when CLK = 1, Q_{crit} of ACFF is higher than in TGFF. The AC element suppresses a SET pulse when a radiation particle hits in ML. We conduct SPICE simulations to confirm the difference when (DATA, CLK) = (1, 1). Under this condition, P0 and P1 turn on as shown in Fig. 4 (a). Unlike low-level signals, high-level signals can pass through the PMOS pass transistor. If the output voltage level of INV0 is sufficiently reduced by a particle hit, a SET pulse is suppressed on the input node of INV1. Figure 4 (b) shows the waveform of a SET pulse before and after passing through P1 when

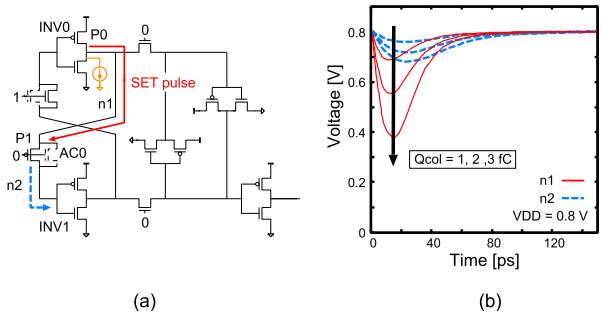


Fig. 4 SET pulse can be suppressed through PMOS transistor in AC element. Q_{col} stands for the collected charge.

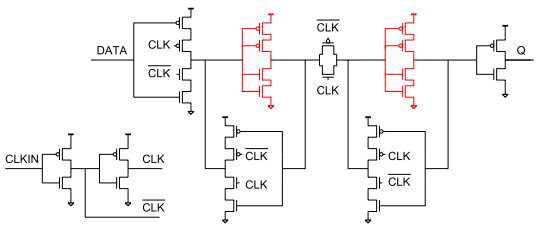


Fig. 5 Conventional stacked FF [10].

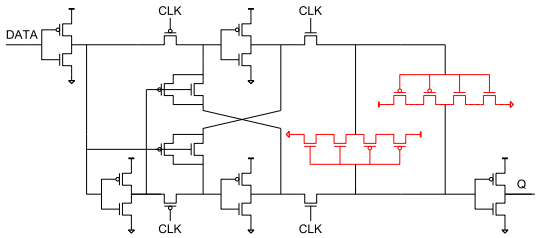
the current source injects charge from 1 fC to 3 fC at 0.8 V. The SET pulse is attenuated after it passes through P1 as shown in Fig. 4 (b). Note that the results are almost equivalent when (DATA, CLK) = (0, 1) because the ML has a symmetrical structure. Even though the NMOS pass transistor of AC0 turns on by a particle hit, the stored value does not change because charge collection is not dominant in FDSOI processes. Therefore, ACFF has higher radiation hardness when CLK = 1. However, ACFF must be strong against soft errors in SL when CLK = 0.

2.2 Radiation Hardened Flip-Flop with Stacked Transistors

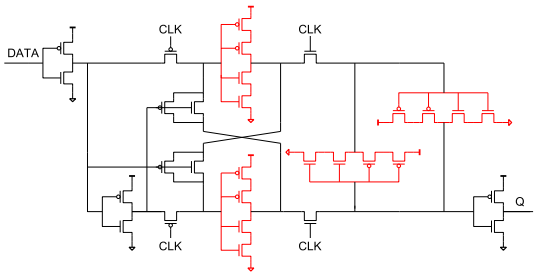
The parasitic bipolar junction transistor effect (PBE) is dominant to cause soft errors in SOI devices [6]. Stacked inverter are composed of series-connected NMOS and PMOS transistors. They resist soft errors better than a standard inverter and have been proposed as a way to prevent soft errors in SOI [10]. Series-connected NMOS transistors are rarely upset by PBE at the same time because they are isolated by a BOX layer and shallow trench isolation (STI). Therefore, it reduces the probability of soft errors. However, it has area and delay time overhead if all inverters are replaced with stacked inverters. Figure 5 shows the stacked FF that prevents soft errors in the inverters [10].

2.3 Proposed Radiation Hardened Flip-Flop Based on ACFF

Figure 6 (a) shows the proposed FF with stacked inverters only in SL called AC Slave-Stacked FF (AC_SS FF) [11]. Figure 6 (b) shows another FF with stacked transistors in both ML and SL called AC All-Stacked FF (AC_AS FF) [11]



(a) AC Slave Stacked FF (AC_SS FF)



(b) AC All Stacked FF (AC_AS FF)

Fig. 6 Proposed FFs based on ACFF.

Table 1 Number of transistor and simulation results of area and dynamic power of each FF. All values are normalized to those of TGFF. The values in parentheses are normalized to those of ACFF.

FF	Area	Power	# of Tr.
TGFF	1	1	24
TMRFF [13]	3.47	2.70	84
BISER [13]	2.74	2.27	62
BCDMR [13]	2.84	2.29	72
DICE [12]	2.00	2.28	56
Stacked FF	1.12	1.02	28
ACFF	1.00	0.55	22
AC_SS FF	1.12 (1.12)	0.58 (1.05)	26
AC_AS FF	1.24 (1.24)	0.58 (1.07)	30

to compare with radiation hardness of AC_SS FF. As previously discussed, ACFF is sensitive to soft errors in SL. AC_SS FF can be suppressed with soft errors in SL with lower performance overheads than ACFF. The ML structure in ACFF and AC_SS FF are weaker than SL. AC_AS FF can be suppressed soft errors in both ML and SL, although it has some amount of delay time and area overheads due to stacked inverters in ML.

2.4 Comparison of Performance among Standard FFs and Proposed FFs

Table 1 shows the number of transistors and the simulation results of area and dynamic power consumption at 10% data activity. All simulations were done at the standard voltage (1.2 V) using SPICE netlists which are extracted from the layout of each FF. The performances of TMRFF, BISER, BCDMR and DICE in bulk processes are reported in [12] and [13]. Data activity is the probability that the output node of FF changes from 0 to 1 or from 1 to 0. All values are normalized to those of TGFF. The values in parentheses are normalized to those of ACFF. The area of AC_SS

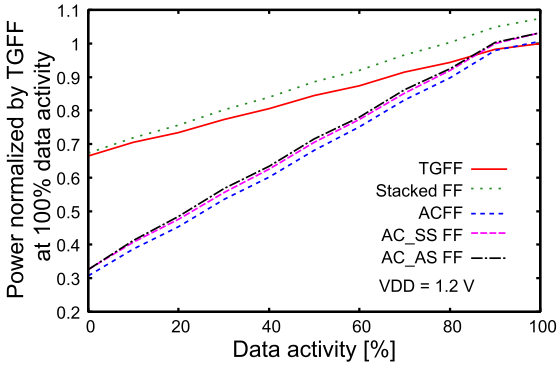


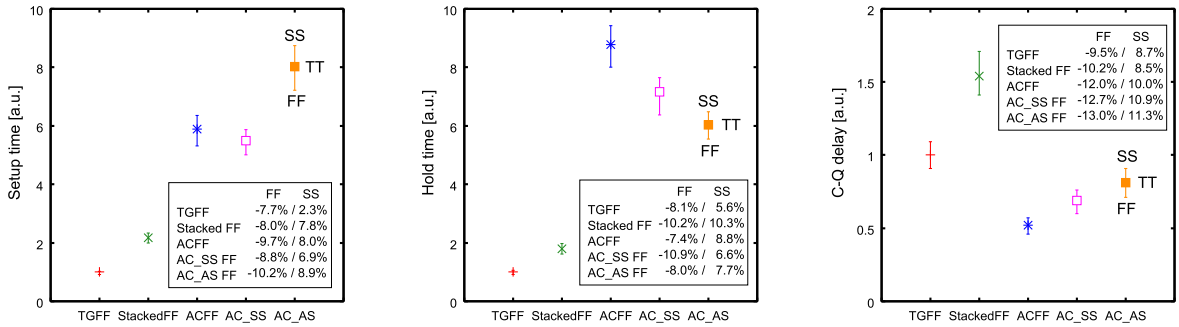
Fig. 7 Simulation results of power consumption of each FF depending on data activity. All values are normalized to those of TGFF at 100% data activity.

Table 2 Simulated setup, hold and C-Q delay times of each FF on TT corner. All values are normalized to setup time of TGFF.

	Setup time	Hold time	C-Q delay
TGFF	1	−0.48	4.47
Stacked FF	2.17	−0.87	7.04
ACFF	5.88	−4.26	2.33
AC_SS FF	5.49 (0.93)	−3.48 (0.82)	3.07 (1.32)
AC_AS FF	8.03 (1.36)	−2.92 (0.69)	3.64 (1.56)

FF and AC_AS FF are bigger than ACFF due to the increase of the number of transistors. The power consumptions of all ACFFs are equivalent. The area overheads of AC_SS FF are equivalent to those of stacked FF. However, AC_SS FF has lower power consumption than the stacked FF. Figure 7 shows power consumption of each FF depending on data activity. The power consumptions of ACFFs are lower than that of TGFF at lower data activity because the power consumption of clock buffers is dominant. In contrast, the power consumptions of ACFFs are equivalent to that of TGFF in higher data activity. Stacked FF consumes the highest power among all FFs at any level of data activities.

Table 2 shows the simulated setup, hold and C-Q delay times of TGFF, stacked FF and ACFFs. The setup times of ACFFs are 5x~8x longer than those of TGFF. Thus, there are some amount of penalties for high-speed operation. On the other hands, the hold times of ACFFs are shorter than that of TGFF. Designers do not consider hold time violations using ACFFs because hold times are negative. The setup and C-Q delay times of the stacked FF are longer than those of TGFF because stacked inverters affect its setup and C-Q delay times. In contrast, stacked inverters give a small impact on C-Q delay time in SL of AC_SS FF because the output inverter (Q) is directly connected to ML through the NMOS pass transistor. Figure 8 shows the simulated C-Q delay times of each FF depending on supply voltage. All values are normalized by the C-Q delay time of TGFF at 1.2 V. There is no data for AC_AS FF at 0.5 V. ACFFs have longer C-Q delay times than TGFF at below 0.8 V because NMOS pass transistors affect their C-Q delay times. It is



(a) Setup time (b) Hold time (c) C-Q delay

Fig. 9 Simulated setup, hold and C-Q delay times of each FF depending on three different process corners. All values are normalized by that of TGFF on TT corner.

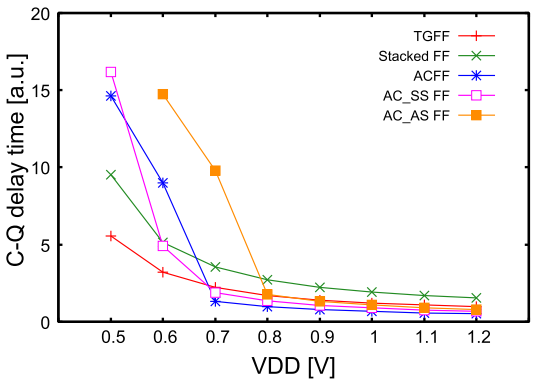
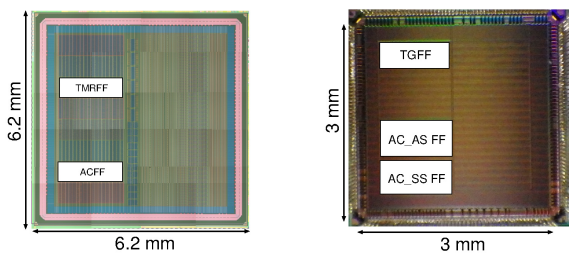


Fig. 8 Simulated C-Q delay time of each FF depending on supply voltage on TT corner. All values are normalized by the C-Q delay time of TGFF at 1.2 V. There are no data for AC_AS FF at 0.5 V.



(a) (b)

Fig. 10 Two fabricated chips in the 65 nm FDSOI process.

better to use the proposed FFs at more than 0.7 V.

We also simulate the setup, hold and C-Q delay times on several process corners to evaluate the variation tolerance. Figure 9 shows the simulated setup, hold and C-Q delay times of each FF on three different process corners. All values are normalized by that of TGFF on the TT corner (both of PMOS and NMOS transistors are typical). The delay variations on FF (fast and fast) and SS (slow and slow) corners are shown in Fig. 9, respectively. Note that the performance is better as the y-axis is higher in Fig. 9 (b). The proposed FFs are more sensitive against process variations than TGFF. The setup, hold and C-Q delay times are almost equivalent among the FFs besides TGFF.

Figure 10 shows two fabricated chips in the 65 nm thin

Table 3 Number of contained FF in each chip.

	FF
Chip (a) in Fig. 10 (a)	ACFF (40,320 bit) TMRFF (17,280 bit)
Chip (b) in Fig. 10 (b)	TGFF (23,976 bit) AC_SS FF (41,760 bit) AC_AS FF (39,150 bit)
Chip (c) [15]	Stacked FF (99,360 bit)

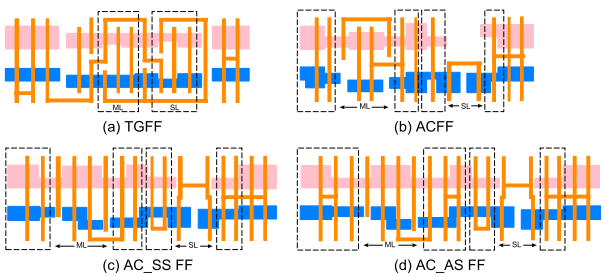


Fig. 11 Simplified layouts of TGFF, ACFF and the proposed FFs.

BOX FDSOI process which has 12 nm SOI and 10 nm BOX layers [14]. We measure radiation hardness of three fabricated chips as shown in Table 3. Figure 11 illustrates the simplified layouts of TGFF, ACFF and the proposed FFs.

3. Radiation Hardness in Terrestrial Environment

3.1 α Particle Irradiation Tests at Normal Incidence

α particle irradiation experiments were carried out using a 3 MBq ^{241}Am source. The irradiation time is one minute. We measure the radiation hardness of four static conditions; (DATA, CLK) = (0, 1), (1, 1), (0, 0) and (1, 0). The experiments were conducted at 0.8 V to get more soft errors by decreasing the minimum charge than at the standard voltage (1.2 V).

Figure 12 shows experimental results of α particle-induced SER. The error bars are within 68% confidence intervals. α particles are emitted from the various materials inside and outside of semiconductor chips. [16] has reported that mold compounds emit 0.024 ~ 0.0005 count/h/cm^2 of α particles. In this paper, we choose 0.001 count/h/cm^2

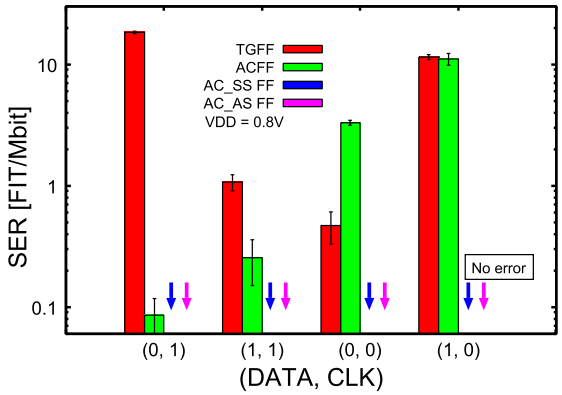


Fig. 12 Experimental results of α particle-induced SER from four DATA and CLK states. The error bars are within 68% confidence intervals.

as the emissivity of α particles to evaluate α-induced SER. The SERs of ACFF show the same tendency as Q_{crit} simulations. SL of ACFF is weak against soft errors. On the other hand, there is no error in ML and SL of the proposed FFs. AC_SS FF has higher radiation hardness than ACFF despite the same circuit structures in ML. It is because SL of AC_SS FF drives larger capacitive load than in ACFF. Higher radiation hardness can be achieved by replacing inverters with stacked inverters only in SL.

3.2 Spallation Neutron Irradiation Tests at Normal Incidence

The spallation neutron experiments were carried out at Research Center for Nuclear Physics (RCNP) at Osaka University. To increase the number of upset FFs, stacked device under test (DUT) boards with four test chips are used. We measured SERs at four static conditions; (DATA, CLK) = (0, 1), (1, 1), (0, 0) and (1, 0). All measurement were done by initializing all FFs, and read data after five minutes. The neutron tests were carried out for two types of fabricated chips as shown in Fig. 10. Acceleration factors of chip (a) and chip (b) measurement are 3.8×10^8 and 3.9×10^8 respectively compared with the sea level at NYC. Experimental results of the stacked FF are quoted from [15].

To increase the number of soft errors, neutron irradiation tests were carried out at lower supply voltage. Figures 13 (a) and (b) show neutron-induced SERs at 0.8 V and 0.4 V respectively. Note that all FFs can hold stored values at 0.4 V and read/write operations were done at 0.8 V. The error bars are within 68% confidence intervals. Stacked FF can decrease SERs to 11% compared with TGFF at 0.8 V when (DATA, CLK) = (1, 1). The stacking transistor is an effective method to decrease SERs. The SERs of ACFF are higher than those of TGFF at 0.4 V when CLK = 0 as shown in Fig. 10 (a). Except for AC_AS FF at 0.4 V when (DATA, CLK) = (0, 0), there was no error in the proposed FFs under the other three conditions. Our results suggest that soft errors can be eliminated by replacing inverters with stacked inverters only in SL. Note that there was no error on TMRFF by the α particle and neutron irradiation tests.

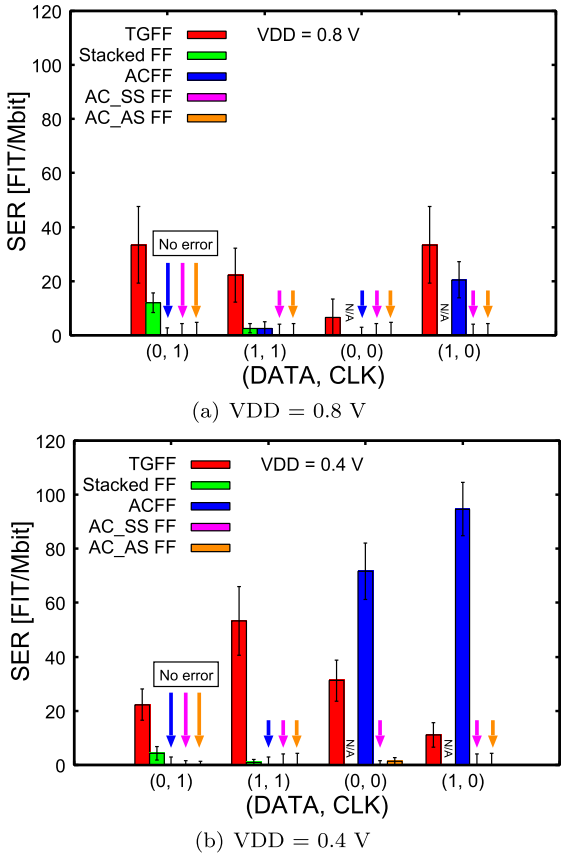


Fig. 13 Neutron irradiation results from four DATA and CLK states. The error bars are within 68% confidence intervals.

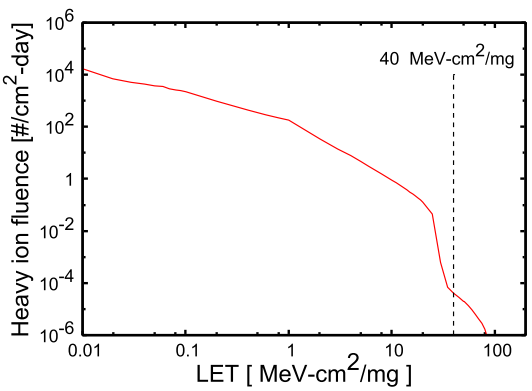


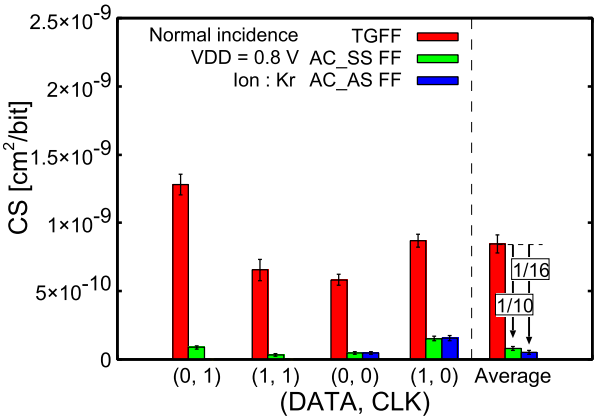
Fig. 14 Integral LET spectrum of heavy ion in outer space [17].

4. Radiation Hardness under Space Environment

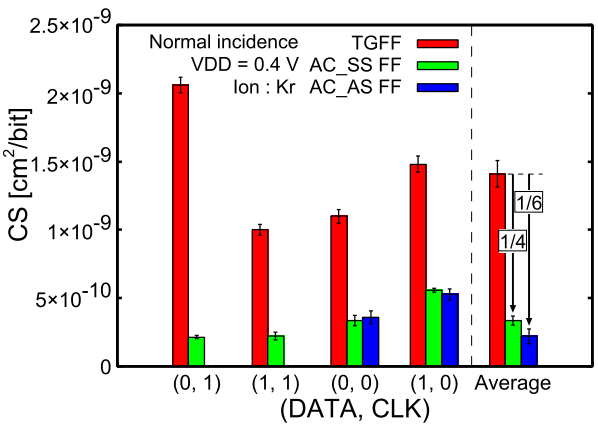
Heavy ion irradiation experiments were carried out at Takasaki Ion accelerators for Advanced Radiation Application (TIARA). TIARA can expose 5 ion sources: N, Ne, Ar, Kr and Xe. We used ions up to linear energy transfer (LET) of 40 MeV-cm^2/mg (Ne, Ar and Kr). Figure 14 shows the integral LET spectrum of heavy ion in outer space [17]. Heavy ion fluence decreases by 1% from 30 MeV-cm^2/mg to 40 MeV-cm^2/mg. Thus, heavy ions up to 40 MeV-cm^2/mg have the greatest impact on SER. Table 4 indicates details of the

Table 4 Specifications of the heavy ions at TIARA.

Ion	Energy [MeV]	LET [MeV-cm^2/mg]	Range [μm]
$^{20}Ne^{4+}$	75	6.5	38.9
$^{40}Ar^{8+}$	150	15.8	36.1
$^{84}Kr^{17+}$	322	40.3	37.3



(a) VDD = 0.8 V



(b) VDD = 0.4 V

Fig. 15 Experimental results of Kr-induced CS from four DATA and CLK states. The error bars are within 68% confidence intervals.

heavy ion irradiation experiments at TIARA. All measurements were done by initializing all FFs, and read data after thirty second irradiation using chip (b) in Fig. 10. All error bars are within 68% confidence intervals.

4.1 Heavy Ion Tests at Normal Incidence

We investigated the radiation hardness of the proposed FFs at normal incidence. We evaluate the radiation hardness by Cross-Section (CS) from Eq. (1).

$$CS = \frac{N_{\mathrm{SE}}}{N_{\mathrm{FF}} \times N_{\mathrm{ion}}} \tag{1}$$

where N_{SE} is the number of errors caused by a heavy ion in thirty seconds, N_{FF} is the total number of each FF array. N_{ion} is the heavy ion fluence.

Figures 15 (a) and (b) show Kr-induced CSs depending on these static conditions; (DATA, CLK) = (0, 1), (1, 1), (0, 0) and (1, 0). SEU in SL was detected, which did not appear at α and neutron tests as shown in Figs. 12 and 13. It implies that stacked inverters are insufficient to eliminate soft errors by heavy ions. It is because both of NMOS transistors in the stacked inverter collect generated charge as the same time when a heavy ion hits between a pair of stacked NMOS transistors. It is reported in [18] that CSs decrease to modify the layout structure of stacked inverters.

SEU occurred in SL of AC_SS FF when CLK = 1. In contrast, there was no error in SL of AC_AS FF. However, the average of CSs of the proposed FFs are equivalent; 1/4 and 1/10 of TGFF at 0.4 V and 0.8 V, respectively.

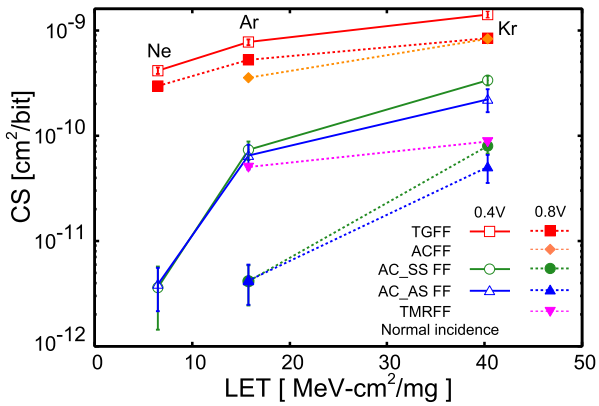


Fig. 16 Experimental results of CS vs. LET at normal incidence. Each value is the average of five measurements at all DATA and CLK conditions. The error bars are within 68% confidence intervals. There is no error for proposed FFs at 0.8 V in Ne test. There is no data for ACFF and TMRFF at 0.4 V and 0.8 V by Ne.

Figure 16 shows experimental results of CS vs. LET at 0.4 V and 0.8 V, respectively. Each value is the average CS of five measurements at all conditions. Note that the measurements of ACFF and TMRFF were conducted once at all conditions. There was no error in the proposed FFs by Ne. There is no data for ACFF and TMRFF at 0.4 V and 0.8 V by Ne. CSs of the proposed FFs by Kr are 93x of those by Ne at 0.4 V, while CS of the conventional TGFF by Ne is 115x of those by Ne at 0.4 V. Thus, the proposed FFs are much stronger against soft errors by heavy ions than TGFF even at higher LET. Even though the radiation hardness of ACFF is equivalent to that of the conventional TGFF, the proposed FFs achieve higher radiation hardness than TMRFF up to 40 MeV-cm^2/mg.

4.2 Cross-Section by Incident Angles

Particles enter semiconductor chips from various directions in outer space. We examined Ar-induced CSs depending on incident angles at 0.4 V and 0.8 V at static conditions; (DATA, CLK) = (1, 0) and (1, 1). Experiments were carried out for tilt angles of 30, 45 and 60 degrees. Figure 17 shows the experimental setup. Figure 17 (a) presents the tilt angle (θ) of the DUT board. Transistors are tilted as Fig. 17 (b). The tilt angle affects irradiated fluence into the chip. Effective CS (CS_{eff}) is calculated from Eq. (2) [19].

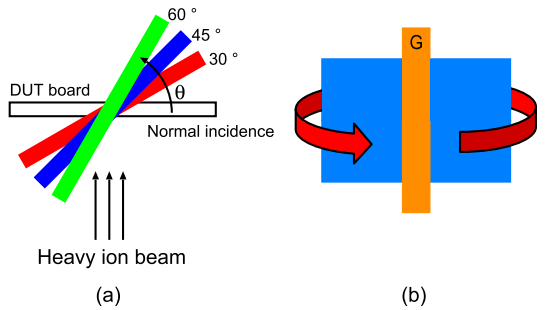
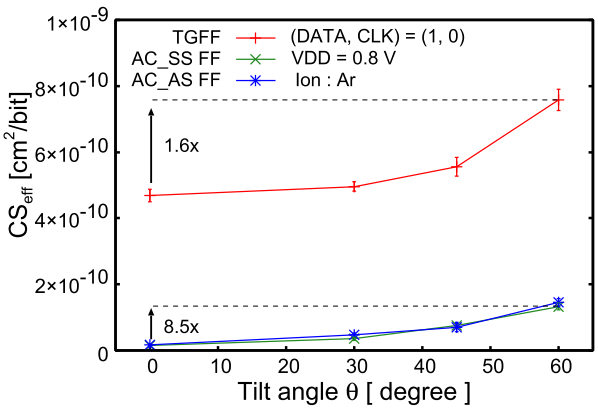
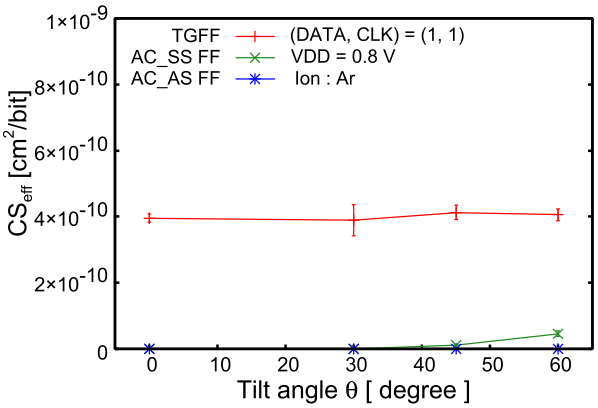


Fig. 17 Measurement setup depending on tilt angles. (a) shows tilt angles of DUT board (θ). Transistors are tilted as (b).



(a) (DATA, CLK) = (1, 0)



(b) (DATA, CLK) = (1, 1)

Fig. 18 Experimental results depending on tilt angles. The error bars are within 68% confidence intervals.

$$CS_{\text{eff}} = \frac{N_{\text{SE}}}{N_{\text{FF}} \times N_{\text{ion}} \cos\theta} \tag{2}$$

Where $N_{\text{ion}} \cos\theta$ is the effective heavy ion fluence at θ.

Figures 18 (a) and (b) show the experimental results. Except for the results of TGFF at (DATA, CLK) = (1, 1), CS_{eff}s increase as tilt angles become larger. The possibility of errors in TGFF and the proposed FFs increases by tilt angle because the possibility of heavy ions passing through the sensitive volume increases. The collected charge to a pair of stacked transistors in the proposed FFs also increase as the tilt angle increases as shown in Fig. 19. Therefore, the

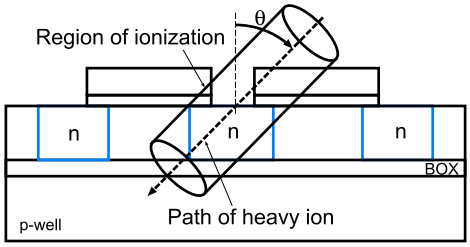


Fig. 19 Path of heavy ion depending on tilt angle in stacked transistors. The cylinder shows the region of ionization.

stacked inverters are more sensitive to soft errors at higher tilt angle than other elements as shown in Fig. 18 (a). At 60 degrees, CS_{eff} of AC_SS FF increases to 8.5x compared with those at the normal incidence.

5. Conclusion

We propose two FFs with stacked transistors based on ACFF in a 65 nm FDSOI process. The proposed FF with stacked transistors only in SL has only 12% area, 5% power and 32% C-Q delay time overheads compared with ACFF. Neutron irradiation and α particle tests revealed no error at any static condition of DATA and CLK states. It can suppress soft errors by α particles and neutrons in the terrestrial region. It has larger radiation hardness and smaller overhead than the conventional stacked FF. We also investigated the proposed FFs by heavy ion irradiation tests. The proposed FFs accomplish higher radiation hardness than TM-RFF which has larger area, delay and power overhead. However, stacked inverters are insufficient to eliminate soft errors by heavy ions. Further methods are required to eliminate them. For example, increasing the distance between stacked transistors may lead to decrease Cross-Sections.

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Haruki Maruoka was born in Kyoto, Japan in 1993. He received the B.E. degree in Electronics and System Engineering from Kyoto Institute of Technology, Kyoto, Japan in 2016. He is currently a master course student at Kyoto Institute of Technology.

Masashi Hifumi was born in Hyogo, Japan in 1992. He received the B.E. and M.E. degrees in Electronics and System Engineering from Kyoto Institute of Technology, Kyoto, Japan in 2015 and 2017, respectively.

Jun Furuta was born in Gifu, Japan in 1986. He received the B.E. degree and M.E. and Ph.D. degrees in Electrical and Electronic Engineering in Informatics from Kyoto University, Kyoto, Japan, in 2009, 2011, 2014, respectively. Starting as a specially appointed assistant professor at Kyoto Institute of Technology in 2014, he was promoted to an assistant professor in 2017.

Kazutoshi Kobayashi was born in Kyoto, Japan in 1968. He received his B.E., M.E. and Ph.D. in Electronic Engineering from Kyoto University, Japan in 1991, 1993, 1999, respectively. Starting as an Assistant Professor in 1993, he was promoted to associate professor in the Graduate School of Informatics, Kyoto University, and stayed in that position until 2009. For two years during this time, he acted as associate professor of VLSI Design and Education Center (VDEC) at the University of Tokyo. Since 2009, he has been a professor at Kyoto Institute of Technology. While in the past he focused on reconfigurable architectures utilizing device variations, his current research interest is in improving the reliability (Soft Errors and Bias Temperature Instability) of current and future VLSIs. He was the recipient of the IEICE best paper award in 2009 and the IRPS best poster award in 2013.