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Replication of Random Telegraph Noise by Using a Physical-Based Verilog-AMS Model

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SUMMARY As device sizes are downscaled to nanometer, Random Telegraph Noise (RTN) becomes dominant. It is indispensable to accurately estimate the effect of RTN. We propose an RTN simulation method for analog circuits. It is based on the charge trapping model. The RTN-induced threshold voltage fluctuation are replicated to attach a variable DC voltage source to the gate of a MOSFET by using Verilog-AMS. In recent deca-nanometer processes, high-k (HK) materials are used in gate dielectrics to decrease the leakage current. We must consider the defect distribution characteristics both in HK and interface layer (IL). This RTN model can be applied to the bimodal model which includes characteristics of the HK and IL dielectrics. We confirm that the drain current of MOSFETs temporally fluctuates in circuit-level simulations. The fluctuations of RTN are different in MOSFETs. RTN affects the frequency characteristics of ring oscillators (ROs). The distribution of RTN-induced frequency fluctuations has a long-tail in a HK process. The RTN model applied to the bimodal can replicate a long-tail distribution. Our proposed method can estimate the temporal impact of RTN including multiple transistors.

key words: *Random Telegraph Noise, reliability, Verilog-AMS*

1. Introduction

As the CMOS technology is downscaled, reliability issues has become more serious [1]. One of the dominant issues is the transistor-performance variation. It can be classified into static and dynamic variations. Static variations are caused by manufacturing process. Dynamic variations are generated by environmental noise and intrinsic device noise. An example of dynamic variations is a performance fluctuation or a gradual performance degradation on a chip. Random telegraph noise (RTN) is one of those issues becoming dominant with process scaling. RTN fluctuates the threshold voltage ($V_{\rm th}$) when the gate bias is applied to the MOSFET [2], [3]. It is reported that RTN has a severe impact on semiconductor chips such as CMOS image sensors [4], flash memories [5] and SRAMs [6]. The impact of RTN is proportional to the gate area [7]. Thus the impact of RTN must be accurately predicted in the nanometer process design.

In this work, we propose a transient RTN simulation method on the circuit level. RTN is modeled by fluctuations of $V_{\rm th}$ caused by defects in the gate oxide [8]. The fluctuation is modeled by several parameters such as the time constant τ and the threshold voltage difference in the defect $\Delta V_{\rm th\_d}$. There are previous works of RTN simulations [9], [10]. They deal with only a single defect, although multiple defects exist in the gate oxide. We construct a model that can deal with multiple defects. The proposed model behaves like a voltage source to the gate terminal because current fluctuation from a carrier trap or emission is represented by the threshold voltage shift ($\Delta V_{\rm th}$). We perform transient analysis of NMOSFETs and ring oscillators (ROs) by attaching the voltage source to the gate terminal. It is possible to estimate the impact of widely distributed RTN fluctuation to perform Monte Carlo simulations with our model.

This paper is organized as follows. We explain the physical model of RTN and the circuit simulation method in Sect. 2. Section 3 shows the simulation results of RTN on NMOSFETs and ROs. Section 4 concludes this paper.

2. Physics Based RTN Model and Application to Circuit Simulation

We explain the mechanism of RTN based on physics and modeling of RTN. Section 2.2 describes how to fluctuate $V_{\rm th}$ by using a variable DC voltage source. The behavior of the voltage source is described in Sect. 2.3.

2.1 RTN Mechanism and Model Based on Physics

RTN is caused when defects in gate dielectrics trap or emit carriers in the channel as shown in Fig. 1. It can be represented by the threshold voltage shift $\Delta V_{\rm th}$ in a transistor model. Figure 2 shows a $V_{\rm th}$ fluctuation caused by RTN from a single defect. Time constants $\hat{\tau}_{\rm c}$ and $\hat{\tau}_{\rm e}$ are defined as the average time to capture and emit carriers respectively. They depend on gate voltage ($V_{\rm G}$). As $V_{\rm G}$ increases, $\hat{\tau}_{\rm c}$ and $\hat{\tau}_{\rm e}$ become short and long respectively [6]. As shown in Fig. 2, $V_{\rm th}$ has two states. When a defect captures or emits a carrier,

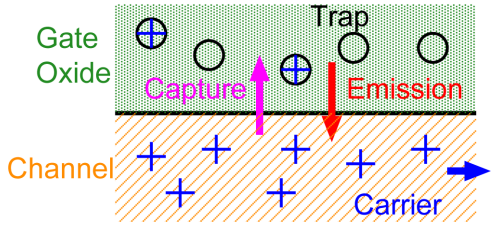

Fig. 1 Mechanism of RTN based on physics in gate oxide.

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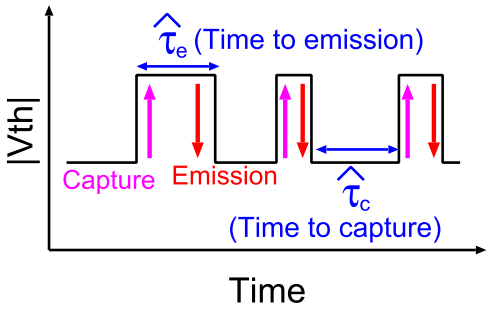


Fig. 2 RTN-induced V_{th} shift by a single defect.

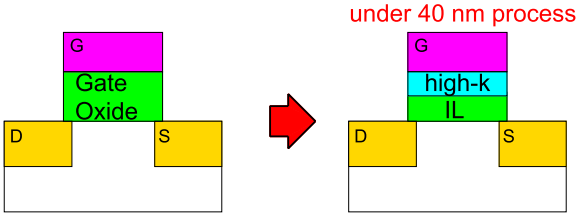


Fig. 3 The high-k (HK) materials are used in gate dielectrics to decrease leakage current.

V_{th} becomes the high or low state respectively. A threshold voltage shift ΔV_{th_d} is constant in each defect [11]. If multiple defects exist in the gate oxide, V_{th} fluctuates among multiple-states. This phenomenon is explained by the charge trapping model (CTM) [8]. In this work, we propose an RTN simulation method based on CTM.

In recent deca-nanometer processes, high-k (HK) materials such as HfSiO and HfO_2 are used in gate dielectrics to decrease leakage current (Fig. 3). The interface layer (IL, e.g. SiO_2) is fabricated between Si and HK because HK on Si causes threshold voltage pinning and phonon scattering. It is found that the defect distribution characteristics are different between HK and IL dielectrics [12]. For this reason, we must consider the bimodal CTM which is adequate to utilize two different defects in HK and IL. When gate dielectrics consists of the interface layer without HK, we apply the unimodal model instead of the bimodal model.

CTM has parameters n, ΔV_{th_d} and $\hat{\tau}_c$ and $\hat{\tau}_e$, where n is the number of defects in the gate oxide. n is different for each transistor and follows the Poisson distribution [13].

The Probability Density Function (PDF) of the Poisson distribution $P(n)$ is expressed as in Eq. (1).

$$P(n) = \frac{N^n e^{-N}}{n!} \tag{1}$$

Where N is the expected value of n and explained as in Eq. (2).

$$N = D{\cdot}LW \tag{2}$$

Where D is the number of defects per gate area. We assume $D_{HK} = 4.0\times10^{-3}$ nm^{-2} and $D_{IL} = 2.0\times10^{-4}$ nm^{-2} [2], [13]. ΔV_{th_d} follows an exponential distribution and τ follows a logarithmic distribution [8], [14]. PDF of the distribution of

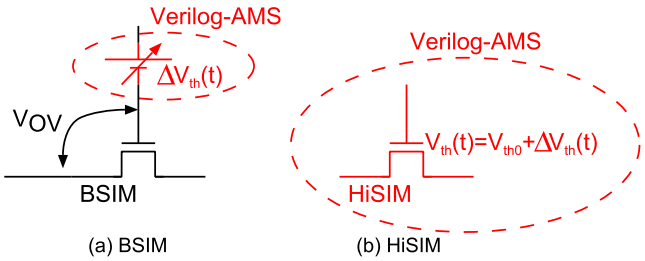


Fig. 4 V_{th} shift method in a circuit-level transient simulation.

ΔV_{th_d} is described by Eq. (3).

$$P(\Delta V_{th\_d}, \eta) = \frac{1}{\eta}\exp\left(\frac{\Delta V_{th\_d}}{\eta}\right) \tag{3}$$

Where η is the expected value of ΔV_{th_d} explained as in Eq. (4).

$$\eta = \frac{s}{LW} \tag{4}$$

Where s is a coefficient of η. We assume $s_{HK} = 9$ V·nm^2 and $s_{IL} = 90$ V·nm^2 [15]. τ follows the logarithmic uniform distribution from 10^{-9} to 10^9 s [14]. It depends on the V_{GS} and changes exponentially as in Eq. (5) [9], [16].

$$\tau = \tau_0 \exp(B{\cdot}V_{GS}) \tag{5}$$

Where τ_0 is the time constant at $V_{GS} = 0$ and B is the sensitivity to V_{GS}. As mentioned above, τ_0 distributes from 10^{-9} to 10^9 s. for each defect. The sensitivity B is distributed from 1 to 10 [9], [16].

2.2 Charge Trapping Model to MOSFET

In the RTN circuit simulation, we must temporally fluctuate V_{th}. Moreover, as mentioned above, τ depends on V_{GS}. It is impossible to use a set of voltage waveforms prepared prior to transient simulations.

V_{th} is shifted by changing device parameters. Standard transistor models are generally used such as BSIM (Berkeley Short channel IGFET Model). But in those models, we cannot change device parameters during transient simulations. As shown in Fig. 4(a), we replicate the RTN-induced threshold voltage fluctuation to connect a variable DC voltage source implemented by using Verilog-AMS attached to the gate terminal. We call the voltage source an RTN module. In the case of HiSIM (Hiroshima-University STARC IGFET MODEL) [17], we can directly change V_{th} because it is usually described in Verilog-AMS (Fig. 4(b))

$\Delta V_{th}(t)$ means the V_{th} shift value at time t during transient analysis. In the case of the BSIM in Fig. 4(a), a variable DC voltage source is connected to the gate terminal of the MOSFET implemented by using Verilog-AMS to shift V_{th} by changing gate overdrive voltage (V_{OV}). It is because it is impossible to change V_{th} in BSIM during transient analysis. On the other hand, ΔV_{th} can be directly changed in the HiSIM in Fig. 4(b) during transient analysis, in which V_{th0}

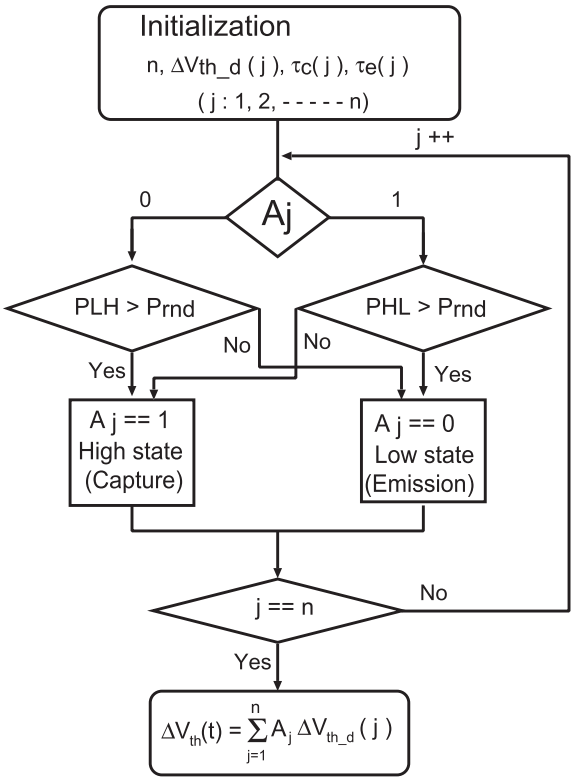


Fig. 5 Flowchart of RTN module.

Table 1 Parameters to calculate RTN.

Name	Explanation
L	Gate length
W	Gate width
n	The number of defects in the gate oxide
N	Expected value of n
D	Defects of gate oxide per unit area
$\Delta V_{\text{th\_d}}$	Threshold voltage fluctuation per defect
η	Expected value of $\Delta V_{\text{th\_trap}}$
s	Coefficient of η
τ_c	Time to capture a carrier
τ_e	Time to emission a carrier
T_{step}	Time step of transient analysis
P_{LH}	Probability to capture a carrier
P_{HL}	Probability to emit a carrier

means the threshold voltage at time 0.

The I_{DS}-V_{DS} characteristics up to ΔV_{th} within $\pm 3\eta$ at the body bias from 0.5 V to -1.0 V are exactly same obtained from our voltage source and delvto in the device model. Note that 3η is close to the maximum ΔV_{th} in the exponential distribution. The transistor model of a commercial 40 nm CMOS technology are used.

2.3 RTN Circuit Simulation Method Using CTM

In this section, we explain the detail of the RTN module. Figure 5 shows the flowchart to compute RTN-induced ΔV_{th}. Parameters to calculate RTN are shown in Table 1.

First, n, $\Delta V_{\text{th\_d}}$ and τ are initialized. Then, a carrier is emitted or captured according to the Markov process without the hysteresis. Finally, ΔV_{th} is increased by $\Delta V_{\text{th\_d}}$ if the carrier is trapped. This process is repeated for all defects.

A_j in Fig. 5 stands for the defect-capture state. "High state" and "Low state" mean that a carrier is captured and emitted respectively. If the state is "High", A_j is equal to 1 while the state is "Low" when A_j is equal to 0. P_{LH} is the transition probability from "Low" to "High". P_{HL} is the reverse transition of P_{LH}. P_{LH} and P_{HL} are expressed as in Eqs. (6) and (7) respectively.

$$P_{\text{LH}} = 1 - \exp\left(\frac{T_{\text{step}}}{\tau_{\text{c}}}\right) \tag{6}$$

$$P_{\text{HL}} = 1 - \exp\left(\frac{T_{\text{step}}}{\tau_{\text{e}}}\right) \tag{7}$$

Where T_{step} is the time step on transient analysis. The defect state is determined by comparing P_{LH} (P_{HL}) with P_{rnd}, which is a random number from 0 to 1. After the states of all defects are determined, ΔV_{th} is calculated by Eq. (8).

$$\Delta V_{\text{th}}(t) = \sum_{j=1}^{n} A_j \Delta V_{\text{th\_d}}(j) \tag{8}$$

Where $\Delta V_{\text{th\_d}}(j)$ is the threshold voltage shift by the jth defect.

In the bimodal case, $\Delta V_{\text{th\_HK}}$ and $\Delta V_{\text{th\_IL}}$ are calculated in HK and IL dielectrics separately.

3. Simulation Results of RTN-Induced Drain Current and Frequency Fluctuation

In Sect. 3.1, we analyze RTN-induced drain current fluctuations of NMOSFETs. Section 3.2 describes the distribution of RTN-induced frequency fluctuations in ring oscillators. Model parameters of a 40 nm CMOS are used in BSIM. In the case of HiSIM, we use a commercial 65 nm FDSOI technology because the 40 nm CMOS technology does not distribute HiSIM.

3.1 RTN-Induced Drain Current Fluctuation of NMOSFETs

We perform transient analysis to replicate RTN-induced current fluctuation. The simulation conditions are shown in Table 2. Figure 6 shows simulation results of drain currents in a single NMOSFET by BSIM. The upper figure shows the drain current fluctuations and the lower one is the number of defects capturing carriers. Drain current fluctuates according to the number of captured defects. Figure 7 shows RTN-induced drain current fluctuations in two NMOSFETs respectively. Figure 7(a) and (b) is the simulation result on BSIM, HiSIM respectively. The amplitudes of RTN and timing of fluctuation are different for each MOSFET. Therefore, we confirm that our proposed RTN model can successfully replicate temporal drain current fluctuation in both models.

Table 2 Simulation conditions of NMOSFET.

Explanation	Parameters	Value
Gate length	L	44 nm (BSIM) 60 nm (HiSIM)
Gate width	W	88 nm (BSIM) 260 nm (HiSIM)
Gate-Source voltage	V_{GS}	1.0 V
Drain-Source voltage	V_{DS}	1.0 V
Source voltage	V_S	0 V
Backgate voltage	V_B	0 V
Simulation time		1 μs

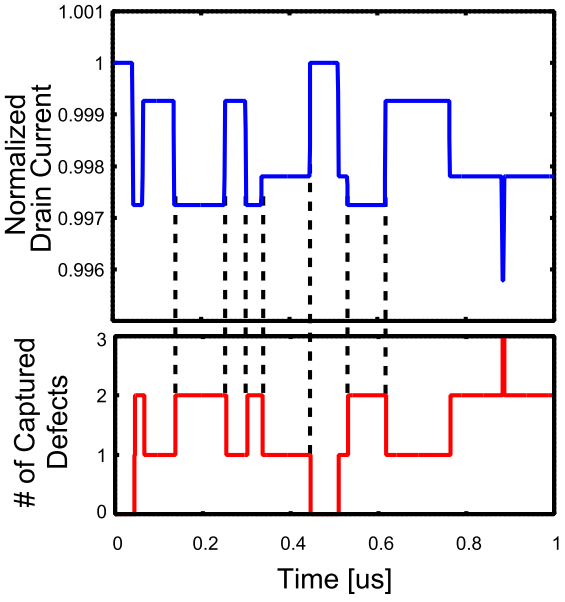


Fig. 6 Simulation results of drain currents (upper) and the number of captured defects (lower) in a single NMOSFET.

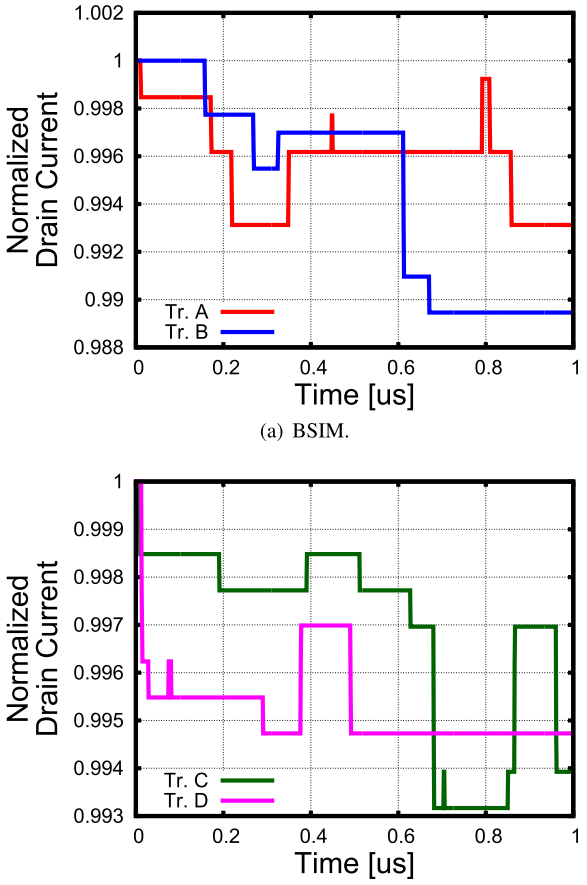


Fig. 7 Drain current fluctuations in two NMOSFETs.

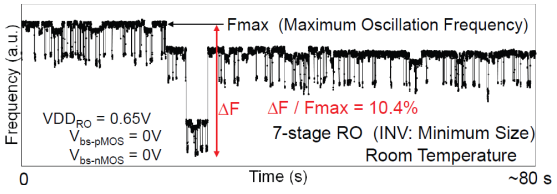


Fig. 8 Measurement result of RTN-induced frequency fluctuation [11].

3.2 The Distribution of RTN-Induced Frequency Fluctuation in Ring Oscillators (ROs)

RTN affects the oscillation frequency of ROs. Figure 8 shows the measurement result of the oscillation frequency of a 7-stage RO in the 40 nm process for 80 seconds at $V_{DD} = 0.65$ V [11]. This process includes the HK and IL (Poly-Si) gate dielectrics. Here, F_{max} is defined as the maximum oscillation frequency and ΔF is defined as the maximum frequency fluctuation shown in Fig. 8. $\Delta F/F_{max}$ is one metric to evaluate the impact of RTN-induced frequency fluctuation. The distribution of $\Delta F/F_{max}$ of 840 ROs is shown in Fig. 10(a). It has a long-tail distribution because of the process has two dielectrics (HK and IL) [12].

Figure 10(b) is the simulation results of 840 ROs by the proposed model. The simulation circuit and conditions are shown in Fig. 9. This condition are different from the measurement results. ROs with 3 stages is used to amplify RTN-induced $\Delta F/F_{max}$ [11]. The RTN-module is connected to gate terminals of each MOSFET. Note that every RTN-module is independent. $\Delta V_{th}(t)$ in all transistors are computed from different random values.

The unimodal in Fig. 10(b) is one of CTM which includes only IL characteristics. The distribution of the unimodal does not have a long-tail, while the bimodal has a long-tail. We found that the proposed model well replicates the measurement results of HK process.

It is easy to get RTN-induced fluctuation in long period over a second by using fabricated chips. But it is hard to obtain fluctuation in short period. On the other hand, it is possible to replicate RTN-induced frequency fluctuations with the same tendency as the measurement results by transient simulations for 1 μs.

Our proposed RTN-induced Verilog-AMS module can replicate RTN-induced $\Delta F/F_{max}$ distribution in the Unimodal and Bimodal models as in [3].

Simulation times by using the proposed RTN module are 2.0x and 3.1x longer in the unimodal and bimodal models

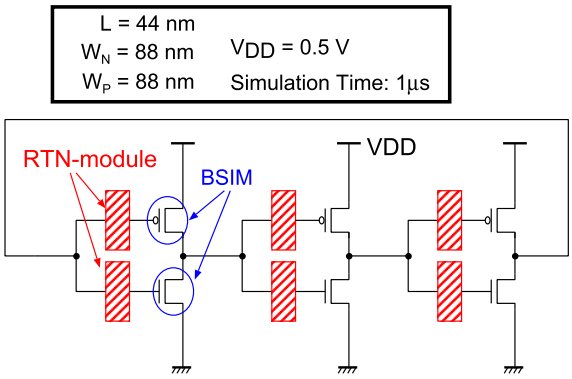
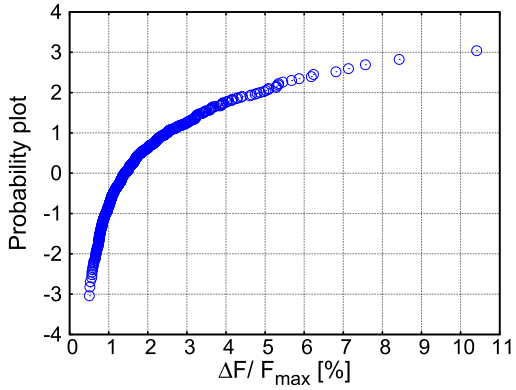
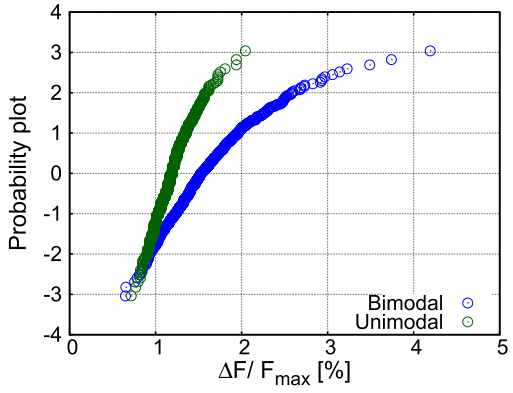


Fig. 9 3-stage ring oscillator. The RTN-module is connected to gate terminals of all MOSFETs. Simulation conditions are described in this figure.



(a) Measurement results of 840 ROs [11].



(b) Simulation results of 840 ROs by BSIM.

Fig. 10 The distribution of $\Delta F/F_{\max}$.

than those without the RTN module respectively.

4. Conclusion

We propose an RTN simulation method to implement a variable DC voltage source which fluctuates theshold voltages temporally by using Verilog-AMS. We construct the bimodal charge trapping model (CTM) which considers the defect distribution characteristics both HK and IL. In the case of BSIM, we attach an independent voltage source implemented by using Verilog-AMS to the gate terminal because device parameters can not be changed dynamically. V_{th} is shifted directly in HiSIM implemented by Verilog-AMS. The proposed model can be applied to both of the unimodal and bimodal CTM. We obtain the RTN-induced drain current fluctuation. The distribution of $\Delta F/F_{\max}$ in ROs is replicated by the bimodal model in the proposed RTN module. Our proposed method can be applied to estimate the temporal impact of RTN for digital analog circuits including multiple transistors.

Acknowledgments

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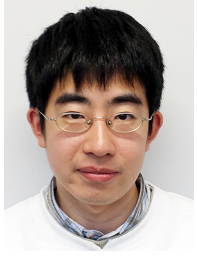

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