Monolithically Integrated E-mode GaN-on-SOI Gate Driver with Power GaN-HEMT for MHz-Switching

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***Abstract*—This paper presents the design of a gate driver, monolithically integrated with power p-gate Gallium Nitride High Electron Mobility Transistor (p-GaN HEMT). It is implemented by an enhancement mode GaN-on-SOI (Silicon on Insulator) technology. Circuit-level simulations considering parasitic components in the integrated circuit (IC) verify the switching operation at 10 MHz, 50 V of off-state V_{DS} and 10 A of on-state I_{D}. GaN-HEMT model has been calibrated by experimental results. The simulation results shows that the proposed gate driver realizes 3.8/ 3.4 ns of turn on/ turn off time, which are 89.0/ 78.9% smaller than a discrete gate driver.**

I. Introduction

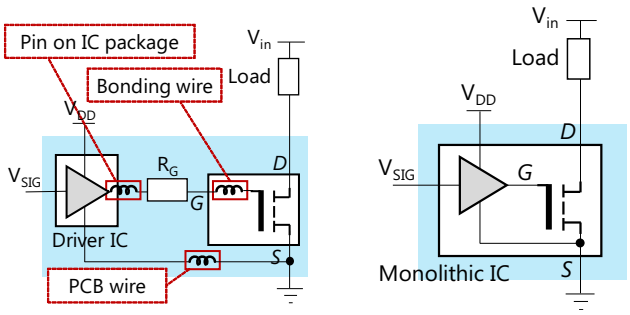
GaN-HEMTs enhance switching speeds which cannot be achieved by other Si-based MOSFETs. They decrease switching energy loss and improve power efficiency[1]. High-frequency switching enables downsized power converters by replacing passive components with smaller ones[2]. It is desirable especially for transport application such as EV (Electric Vehicle) and train. However, fast switching is limited by parasitic inductance and capacitance mainly originated from wires between the gate terminal of a power HEMT and the gate driver (Fig. 1 (a)).

In this work, a monolithically integrated gate driver with the enhancement mode GaN-HEMT is proposed based on GaN-on-SOI (Silicon on Insulator) process. The target is 10 MHz fast transition switching with less noise. The switching characteristics of IC is verified by simulations using the HEMT model calibrated by experimental results. Section II explains the motivation of this work. The proposed IC structure are described in Section III including its process, feature sizes and layout. The HEMT model development is mentioned in Secion IV. Secion V evaluates monolithic IC by simulation. Section VI concludes the paper.

II. Motivation

Fast switching of GaN-HEMTs is hardly obtained by driving GaN-HEMTs with a discrete gate driver due to parasitic inductance. The parasitic issue was verified by experiments on a power HEMT switching with a separated gate driver. Fig. 2 shows measurement results at 5 MHz switching frequency operation, 50 V of off-state V_{DS} and 5 A of on-state I_{D}. Ratio of the transition time to the switching cycle and ringing noise cannot be ignored. In order to achieve further high frequency, it is necessary to improve the trade-off between switching time and overshoot voltage.

A monolithic integration of the HEMT with a gate driver in Fig. 1 (b) has been taken to overcome the aforementioned problem. It minimizes parasitic inductance and enhances switching speed. It is expected to be a promising approach as related works have been reported in [3], [4], [5], [6]. Monolithic integration using depletion mode (D-mode) GaN-HEMTs are presented in [3], [4]. D-mode HEMTs have a risk in that accidental failure may be appeared in power converters at abnormal conditions such as uncontrollable input signals. [5], [6] addressed by using enhancement mode HEMTs. However, GaN-on-Si and GaN-on-SiC technology have negative effect by a conductive substrate as demonstrated in [7], [8].



(a) Discrete (b) Monolithically integrated

Fig. 1: Gate drivers.

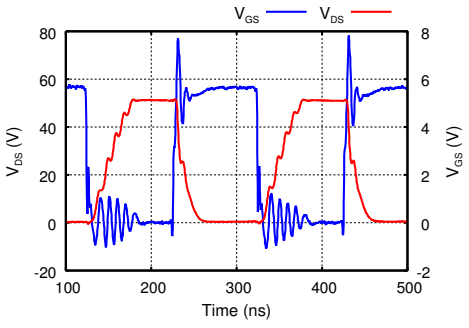


Fig. 2: Switching characteristic of GaN-HEMT driven by a discrete gate driver at 50 V of off state V_{DS} and 5 A of I_{D}.

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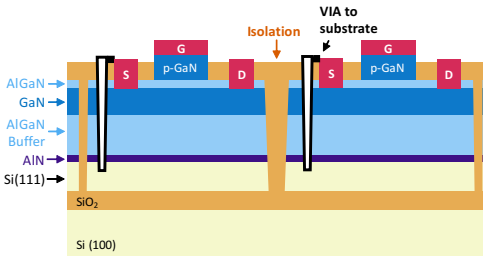


Fig. 3: GaN on SOI process.

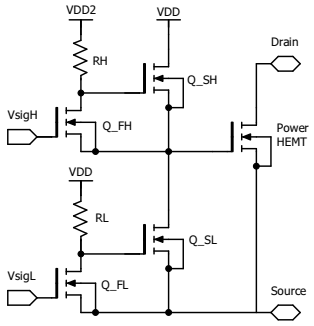


Fig. 4: Proposed monolithic GaN integrated circuit (IC).

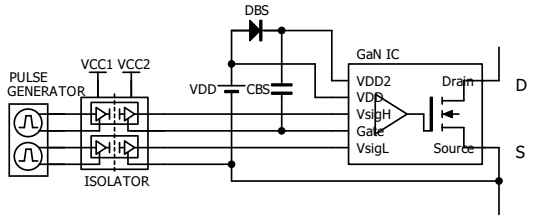


Fig. 5: Whole system schematic.

GaN-on-SOI (Silicon on Insulator) process [9], [10] enables to form HEMTs insulating substrates among GaN-HEMTs as shown Fig. 3.

III. Monolithically-Integrated Circuit

Figure 4 shows the proposed monolithically IC including the power HEMT and the gate driver[11]. The gate driver has two stages. In the first stage, two GaN HEMTs and resistors are configured as a pair of logic inverters. The HEMTs have small input capacitance, thereby delivering steep rise and fall signals to the second stage. The second stage consists of a pair of HEMTs with enough capability to charge and discharge the power HEMT. The circuit employs a bootstrap-structure voltage supply and a two-input pulse generator for the gate driver (Fig. 5).

Fig. 6 shows the input and output signals at each phase. The operation procedure is as follows:

1) Pulse generator supplies differential digital signals V_{sigL} and V_{sigH} to the first stage HEMTs, Q_FH and Q_FL.
2) Each signal V_{sigL}, V_{sigH} is inverted in the first stage, and transferred to the second stage.

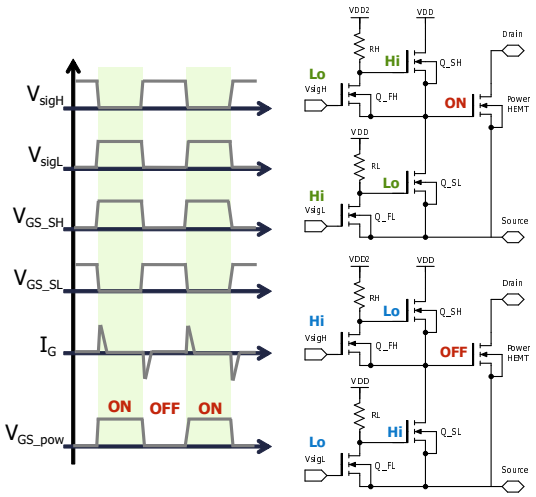


Fig. 6: Input and output signals for ON/OFF operation.

TABLE I: Feature size of HEMTs and resistance.

	W_{g}	L_{gd}	L_{gs}	L_{fp}	L_{g}
PowerHEMT	70	4	0.75	0.65	1.3
Q_SH	24	1.5	0.75	0.25	1.3
Q_SL	24	1.5	0.75	0.25	1.3
Q_FH	8	1.5	0.75	0.25	1.3
Q_FL	8	1.5	0.75	0.25	1.3

	R (Ω)
RH/RL	14.1

W_{g}: gate width (mm)
L_{gd}: gate-drain distance (μm)
L_{gs}:gate-source distance (μm)
L_{fp}: gate field plate (μm)
L_{g}: gate length (μm)

3) In the second stage, Q_SH and Q_SL form an inverter to drive the power HEMT. V_{GS} is 0 when Q_SL is on. V_{GS} is V_{DD} when Q_SH is on.

The gate driver in [11] has several advantages. It requires only one voltage supply using an external bootstrap circuit. It satisfies both fast speed and high driving capability by separating charging and discharging routes to the gate.

Table I shows dimensions of HEMTs and resistance values correspond to the circuit in Fig. 4. The power HEMT has 100 V drain-source breakdown voltage. On-resistance $R_{\mathrm{DS(ON)}}$ is 67 mΩ. Fig. 7 shows the simplified layout of the IC. Resistors RH, RL are formed by two dimensional electron gas (2DEG) sheet resistance.

IV. GaN-HEMT Model

A. Model Development

There are several available models for GaN-HEMT as introduced in [12], [13], [14]. The MVSG-HV (MIT Virtual Source GaNFET-High Voltage) compact model [13] is chosen to evaluate the proposed integrated circuit because it is geometry scalable and takes into account both of dynamic and static characteristics. MVSG-HV is based on transport and charge model. Table II shows the list of key parameters used in fitting. Parameters are extracted from experiments using a discrete GaN-HEMT. DC characteristics of the model are evaluated

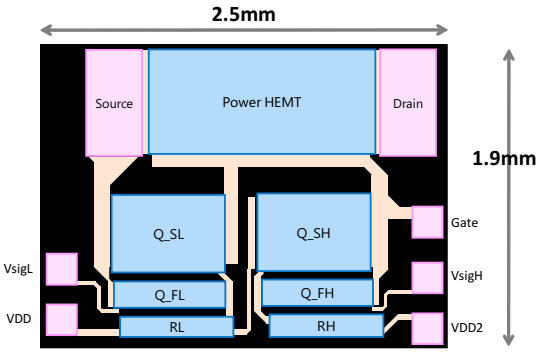
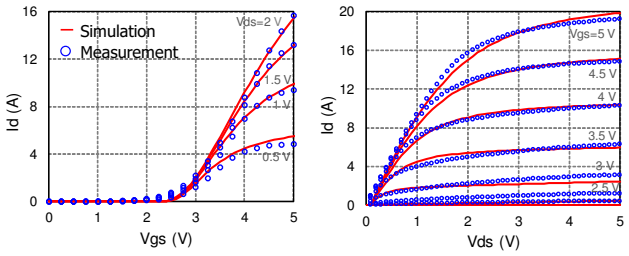


Fig. 7: Layout of monolithic IC.

TABLE II: Parameters in MVSG-HV model.

parameters		Explanation
w	-	Width per finger
L_{gd}	-	Gate-drain distance
L_{gs}	0.75 μm	Gate-source distance
r_{sh}	500 Ω/sq	2 DEG Sheet resistance
v_{xo}	1.3e5 m/s	Source injection velocity
μ	0.1 $\mathrm{m}^2/(\mathrm{V}\cdot\mathrm{s})$	Low field mobility
SS	0.15 V/dec	Sub threshold voltage



(a) Id-Vgs (b) Id-Vds

Fig. 8: HEMT-model DC characteristics fitting with measurement results.

by the ADS (Advanced Design System) circuit simulator from Keysight. Fig. 8 shows DC characteristics obtained from simulations and measurements. The simulation results in DC characteristics are well matched with measurement data.

B. Model Verification by Switching Characteristics

The accuracy of the model for switching characteristics is verified by comparing simulation results with measurement data. The measurement circuit was designed using a discrete gate driver.

The measurement circuit is shown in Fig. 9. The DUT (device under test) is an E-mode p-gate GaN-HEMT, which is developed by IMEC. The feature sizes are as follows: 150 mm of W_{g}, 6 μm of L_{gd} and 0.75 μm of L_{gs}. The DUT packaged in HSOP-24 (24-pin small outline package with heat sink) are mounted to the socket on the measurement board. An input signal is generated by the Intel FPGA EP1C6Q240, which provides 20 MHz input signals at maximum. The FPGA is programmed to control input signals of the gate driver.

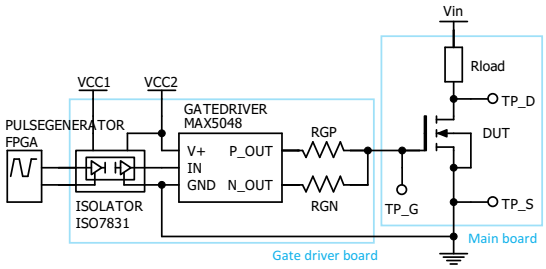


Fig. 9: Measurement circuit designed with discrete gate driver.

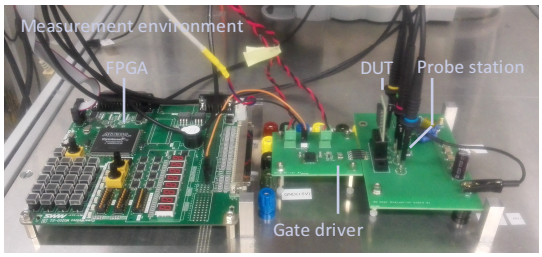


Fig. 10: Measurement setup.

The oscilloscope employed in the measurement is HDO6054 (Lecroy). A photograph of the measurement setup is shown in Fig. 10. Switching characteristics are measured at V_{in} = 50 V, R_{load} = 10.5 Ω, R_{GN} = 10 Ω and R_{GP} = 10 Ω.

Figure 11 shows the schematic of the measurement circuit for simulation with parasitic elements listed in Table III. The input signal is equivalent to measurement to evaluate in the same condition with experiment.

Comparison of the switching waveforms with the measurements and simulations is shown in Fig. 12. The tendency of the transition characteristics at turn on and off are quite similar. Table IV shows switching time according to the definition of switching time parameters shown in Fig 13. Difference between simulation and measurement is 12.1% on average. It can be caused by process variations and mismatches of

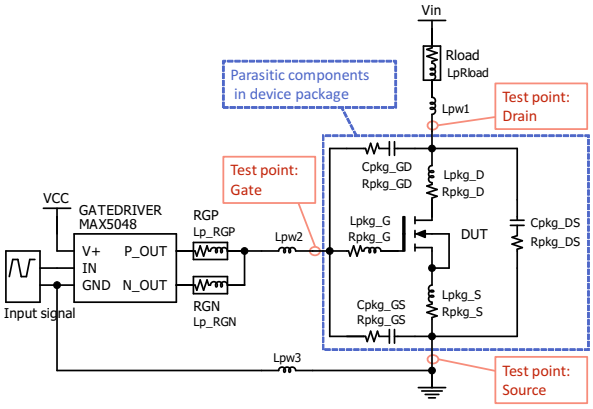


Fig. 11: Measurement circuit by discrete gate driver for simulation.

TABLE III: Parasitic components in measurement circuit.

Package				Exterior of DUT	
$L_{\mathrm{pkg\_G}}$	5 nH	$R_{\mathrm{pkg\_G}}$	30 mΩ	$L_{\mathrm{p\_RGP}}$	3 nH
$L_{\mathrm{pkg\_D}}$	2.4 nH	$R_{\mathrm{pkg\_D}}$	0.4 mΩ	$L_{\mathrm{p\_RGN}}$	3 nH
$L_{\mathrm{pkg\_S}}$	4 nH	$R_{\mathrm{pkg\_S}}$	0.5 mΩ	$L_{\mathrm{p\_Rload}}$	4 nH
$C_{\mathrm{pkg\_GS}}$	0.4 pF	$R_{\mathrm{pkg\_GS}}$	70 Ω	L_{pw1}	5 nH
$C_{\mathrm{pkg\_GD}}$	0.8 pF	$R_{\mathrm{pkg\_GD}}$	0.72 Ω	L_{pw2}	4 nH
$C_{\mathrm{pkg\_DS}}$	0.9 nF	$R_{\mathrm{pkg\_DS}}$	3.3 Ω	L_{pw3}	3 nH

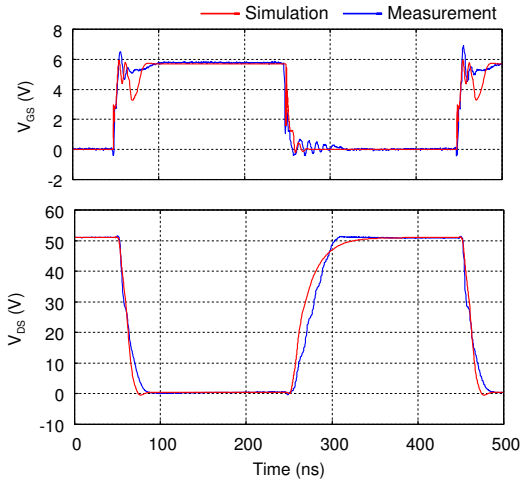


Fig. 12: Switching waveforms (simulation vs. measurement).

the parasitic elements between simulations and experiments, not only by precision of the model. Same amount of design margin should be considered when designing IC layout based on simulation results.

From the results, it is verified that the developed model has enough accuracy to estimate switching characteristics and switching time.

V. Evaluation of Monolithic IC by Simulation

The monolithic integrated circuit and discrete gate driver are compared by simulation. Influence of a package on the switching characteristics, power dissipation in IC are also evaluated.

TABLE IV: Switching time (simulation vs. measurement).

unit:ns

	t_{ON}	$t_{\mathrm{r\_GS}}$	t_{OFF}	$t_{\mathrm{f\_GS}}$
Measurement	26.4	5.2	49.0	7.0
Simulation	20.8	4.8	47.1	8.1
Difference	5.6	0.4	1.9	-1.1
	+21.2%	+7.7%	+3.9%	-15.7%

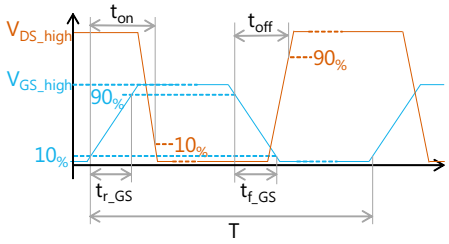


Fig. 13: Definition of switching time.

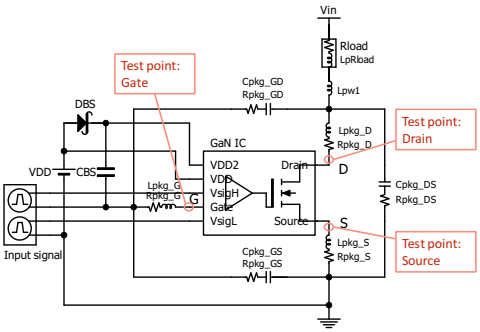


Fig. 14: Evaluation circuit of monolithic IC for simulation.

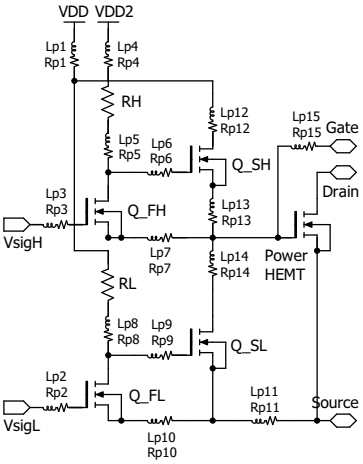


Fig. 15: Parasitic components in IC.

Figure 14 shows the evaluation circuit using the monolithic IC. Parasitic elements in the package, PCB wires, R_{load} in Table III and IC are considered in the simulation to evaluate switching characteristics in an environment close to reality. Fig. 15 and Table V shows parasitic components in the IC extracted from the IC layout. The parasitic inductance value becomes smaller over an order of magnitude in the path between the gate driver and the gate terminal of power HEMT. The bootstrap circuit is composed of 50 nF of C_{BS} and a schottky barrier diode (Panasonic DB2J20900L). The evaluation circuit using the discrete gate driver is shown in Fig. 11, which was introduced in Section IV-B. Dimension parameters of the model are set to the power HEMT in Table I, which is the same condition with the monolithic IC. The pulse generator provides ideal input signals having recutangular waveform at 2.5MHz. The measurement points are gate, drain, and source terminals. Switching characteristics are evaluated at 50 V of off-state V_{DS} and 10 A of on-state I_{D}.

The switching characteristics with the IC and discrete gate driver are simulated as shown in Fig. 16. The monolithic IC shows fast and smooth transient. On the other hand, ringing appears during transient in the case of driving by the discrete

TABLE V: Parasitic components in IC.

L_{para} (nH)		R_{para} (mΩ)		L_{p8}	0.033	R_{p8}	24.0
L_{p1}	0.075	R_{p1}	30.0	L_{p9}	0.047	R_{p9}	26.7
L_{p2}	0.143	R_{p2}	70.4	L_{p10}	0.021	R_{p10}	7.1
L_{p3}	0.134	R_{p3}	80.0	L_{p11}	0.056	R_{p11}	8.0
L_{p4}	0.092	R_{p4}	35.0	L_{p12}	0.274	R_{p12}	80.0
L_{p5}	0.004	R_{p5}	2.5	L_{p13}	0.079	R_{p13}	16.0
L_{p6}	0.037	R_{p6}	25.6	L_{p14}	0.064	R_{p14}	20.0
L_{p7}	0.028	R_{p7}	18.7	L_{p15}	0.060	R_{p15}	17.1

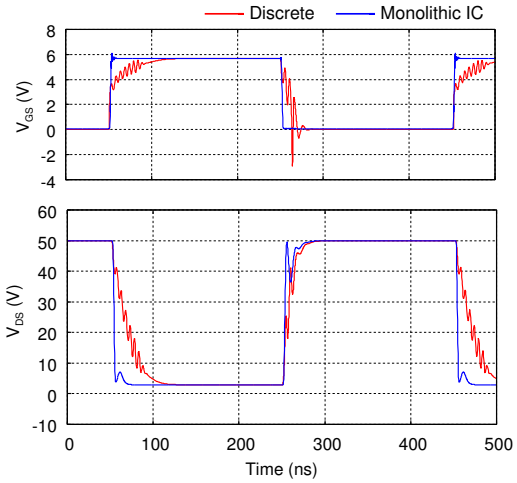


Fig. 16: Switching waveforms (IC vs. discrete).

gate driver. It is originated from parasitic inductance in gate-source loop. Note that the condition using the gate driver are different between switching characteristics in Fig. 12 and that in Fig. 16 because they have different input signals, DUT model, R_{load} and test points.

Table VI shows switching time extracted from the switching waveform. Monolithic IC reduces turn-on and turn-off time by over 70 %. The ratio of switching time t_{ON} + t_{OFF} to switching cycle α_{sw} is 7.2% at 10MHz. Even considering 20% margin for fluctuation in characteristics, the ratio α_{sw} is 8.6% at maximum. From this estimation, duty ratio range can be changed up to 91.4%, considering switching transition ratio α_{sw}. It would be enough applicable for power converters.

Fig. 17 shows 10 MHz switching characteristics comparing parasitic influence. "w/ parasitic" is evaluated by setting parasitic parameters to Table III, while "w/o parasitic" is done by setting parasitic components to 0 besides parasitic components in the IC. It can be seen from simulation results that V_{GS} waveforms are quite similar, which means external parasitic inductance does not affect V_{GS}. On the other hand,

TABLE VI: Switching time (IC vs. discrete).

unit:ns

	t_{ON}	$t_{\mathrm{r\_GS}}$	t_{OFF}	$t_{\mathrm{f\_GS}}$
IC	3.8	1.2	3.4	1.4
Discrete	34.5	22.9	16.1	12.4
Improvement	30.7	1.2	3.4	11
Rate	89.0%	94.8%	+78.9%	88.7%

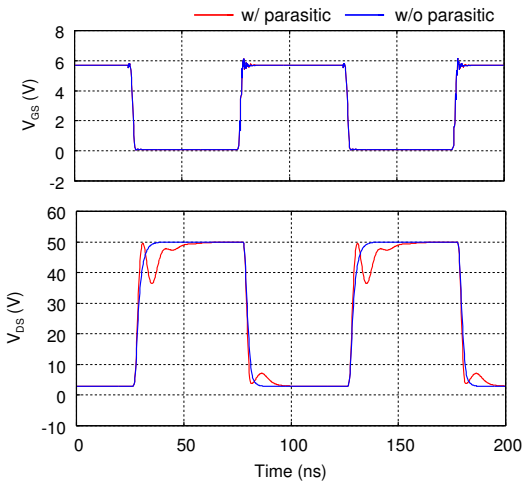


Fig. 17: 10 MHz switching waveforms comparing parasitic influence.

TABLE VII: Energy and power loss in IC.

	Energy loss/ cycle (μJ)	Power loss (W)
PowerHEMT	2.44	24.35
Q_SH	8.49e-3	8.49e-2
Q_SL	8.78e-3	8.78e-3
RH	8.20e-2	8.20e-1
RL	9.82e-2	9.82e-1
Q_FH	4.64e-3	4.64e-2
Q_FL	5.46e-3	5.46e-2
Total	2.64	26.42

V_{DS} is affected by the parasitic inductance. This is because voltage drop causes as expressed by $L_{\mathrm{p}} \cdot \frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}$ through parasitic inductance on drain-source side such as $L_{\mathrm{pkg\_D}}$, $L_{\mathrm{pkg\_S}}$ and $L_{\mathrm{p\_Rload}}$. Those parasitic inductance should be minimized especially at high speed transition.

Power dissipation in the IC is evaluated with the circuit in Fig. 14 by simulation at 50 V of off-state V_{DS}, 10 A of on-state I_{D} and 10 MHz switching frequency. The parasitic components in the evaluation circuit is ignored while those inside the IC is considered. The calculation results are shown in Table VII. Power loss in the gate driver $P_{\mathrm{loss\_driver}}$ is 7.9% of total power loss $P_{\mathrm{loss\_total}}$ at 10 MHz. The gate driver structure is unsuitable for low frequency switching condition because the ratio of $P_{\mathrm{loss\_driver}}$ in $P_{\mathrm{loss\_total}}$ increases due to continuous power dissipation in RH and RL. For the high frequency operation, the monolithic IC is expected to contribute to decrease $P_{\mathrm{loss\_total}}$ by saving power loss in power HEMT due to small switching time compared to driving with a discrete gate driver.

VI. Conclusion

The monolithic integration circuit of the p-gate power HEMT and gate driver has been proposed. Switching operation is verified by simulation using the MVSG-HV model whose parameters are calibrated by experimental results. 10 MHz switching of the power HEMT driven by monolithically integrated gate driver is demonstrated at 50 V of off-state

V_{DS} and 10 A of on-state I_{D}. The turn-on/ turn-off time of the proposed IC are 3.8/ 3.4 ns which are 89.0/ 78.9% smaller than those of a discrete gate driver structure.

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REFERENCES

[1] N. Otsuka, Y. Kawai, and S. Nagai, "Recent Progress in GaN devices for Power and Integrated Circuit," in *2017 IEEE 12th International Conference on ASIC (ASICON)*, Oct 2017, pp. 928–931.

[2] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance Trends and Limitations of Power Electronic Systems," in *2010 6th International Conference on Integrated Power Electronics Systems*, March 2010, pp. 1–20.

[3] Y. Zhang, M. Rodriguez, and D. Maksimovi, "High-frequency Integrated Gate Drivers for Half-bridge GaN Power Stage," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2014, pp. 1–9.

[4] S. Moench, M. Costa, A. Barner, I. Kallfass, R. Reiner, B. Weiss, P. Waltereit, R. Quay, and O. Ambacher, "Monolithic Integrated Quasi-normally-off Gate Driver and 600 V GaN-on-Si HEMT," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2015, pp. 92–97.

[5] M. Giandalia, J. Zhang, and T. Ribarich, "650 V AllGaN Power IC for Power Supply Applications," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2016, pp. 220–222.

[6] A. Sepahvand, Y. Zhang, and D. Maksimovic, "High Efficiency 20-400 MHz PWM Converters using Air-Core Inductors and Monolithic Power Stages in a Normally-off GaN Process," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 580–586.

[7] S. Moench, C. Salcines, R. Li, Y. Li, and I. Kallfass, "Substrate Potential of High-voltage GaN-on-Si HEMTs and Half-bridges: Static and Dynamic Four-terminal Characterization and Modeling," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–8.

[8] S. Moench, R. Reiner, B. Weiss, P. Waltereit, R. Quay, O. Ambacher, and I. Kallfass, "Effect of Substrate Termination on Switching Loss and Switching Time Using 600 V GaN-on-Si HEMTs with Integrated Gate Driver in Half-bridges," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct 2017, pp. 257–264.

[9] X. Li, M. V. Hove, M. Zhao, K. Geens, W. Guo, S. You, S. Stoffels, V. P. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, "Suppression of the Backgating Effect of Enhancement-mode p-GaN HEMTs on 200-mm GaN-on-SOI for Monolithic Integration," *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 999–1002, July 2018.

[10] X. Li, M. V. Hove, M. Zhao, K. Geens, V. P. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, "200 V Enhancement-mode p-GaN HEMTs Fabricated on 200 mm GaN-on-SOI With Trench Isolation for Monolithic Integration," *IEEE Electron Device Letters*, vol. 38, no. 7, pp. 918–921, July 2017.

[11] K. Nagaoka, K. Chikamatsu, A. Yamaguchi, K. Nakahara, and T. Hikihara, "High-Speed Gate Drive Circuit for SiC MOSFET by GaN HEMT," *IEICE Electronics Express*, vol. advpub, 2015.

[12] Q. Chen, "Latest Advances in Gallium Nitride HEMT Modeling," in *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct 2014, pp. 1–4.

[13] U. Radhakrishna, T. Imada, T. Palacios, and D. Antoniadis, "MIT Virtual Source GaNFET-high Voltage (MVSG-HV) Model: A Physics Based Compact Model for HV-GaN HEMTs," vol. 11, 02 2014.

[14] A. Dasgupta, S. Ghosh, Y. S. Chauhan, and S. Khandelwal, "ASM-HEMT: Compact Model for GaN HEMTs," in *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, June 2015, pp. 495–498.