An Asynchronous Buck Converter by Using a Monolithic GaN IC Integrated by an Enhancement-Mode GaN-on-SOI Process

1st Shumpei Noike
Kyoto Institute of Technology
Kyoto, Japan
snoike@vlsi.es.kit.ac.jp

2nd Junichiro Nagao
Kyoto Institute of Technology
Kyoto, Japan
jnagao@vlsi.es.kit.ac.jp

3rd Jun Furuta
Kyoto Institute of Technology
Kyoto, Japan
furuta@vlsi.es.kit.ac.jp

4th Kazutoshi Kobayashi
Kyoto Institute of Technology
Kyoto, Japan
kazutoshi.kobayashi@vlsi.es.kit.ac.jp

***Abstract*—A three-level gate driver and a power GaN HEMT were integrated on a monolithic chip by an Enhancement-mode GaN-on-SOI process. The chip realises high speed switching and effective three-level gate driving without any external negative power supply. However it has a problem of low heat dissipaton in continuous operations because of the BOX layer and the deep trenches for isolating power devices. Then, the IC was implemented in a C-QFN package and evaluated the tolerance for continuous operation with measuring the case temperature. The measurement result shows that the GaN IC can safely operate continuously in condition of the storage temperature below $64^\circ\mathrm{C}$. We attempted to design a small and high power density converter using the fabrication chip.**

***Index Terms*—GaN HEMT, monolithic integration, GaN-on-SOI, heat dissipation, continuous operation, downsize, power density**

I. Introduction

Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) have attracted attention as one of next-generation power devices. They can realize high frequency operation of power converters and downsizing passive components and heat radiators because they have a high performance for fast switching and high temperature tolerance [1]–[3]. Although, due to the low threshold voltage and high switching speed of GaN HEMTs, the false turn-on phenomena and reverse conduction loss are more serious than Si devices [4]–[6].

The 3-level gate driving method is an effective breakthrough to suppress false turn-on phenomena with minimizing the reverse conduction loss [7], [8]. We have proposed a 3-level gate driver circuit without any negative voltage sources and integrated it with a power GaN HEMT on a monolithic chip [9]. The chip was fabricated in an enhancement-mode GaN-on-SOI process with deep trench, which is promising for improving the performance of all-GaN power IC from the GaN-on-SI process [10]–[13]. However, in the GaN-on-SOI process, the BOX layer and the deep trench isolation suppress heat dissipaton of devices more than GaN-on-SI [14] and may result in breakdown from over-heating.

To realize a high power density converter with the GaN IC, we aimed to apply a countermeasure against heat-generation and evaluate the tolerance and practicality of the GaN IC for continuous operation. Moreover, we designed a small and high power density converter after the evaluation.

II. The Proposed GaN IC

Fig. 1 shows the 3-level gate driver circuit and Fig. 2 shows the GaN IC chip. The components except for M6 (p-MOS) and CSUB are integrated on the chip. An external discrete p-MOS device is used as M6. This chip was fabricated on a GaN-on-SOI substrate using an Enhancement-mode p-GaN technology and deep trench isolation, and the source pins are connected to the substrate with power metal wires. Fig. 3 shows an example of the cross section of two isolated GaN HEMTs. Therefore, all components of the GaN IC can be driven as a standard discrete n-MOS. The fabricated chip size is 3.3 mm $\times$ 1.9 mm and the chip is implemented in a C-QFN package as shown in Fig. 4.

Because each device on the GaN IC is isolated by deep trenches and have a BOX layer in the substrate, thermal resistance of device-to-device or device-to-substrate is higher than GaN-on-SI and each device easily accumulates Joule heat. Therefore the heat dissipaton of GaN HEMTs fabricated by the GaN-on-SOI process is less than GaN HEMTs fabricated by the GaN-on-Si process [14]. This problem is particularly prominent in the M1 power GaN HEMT applied in main circuits of the power converter. In this work, some measurements and evaluations focused on M1. The GaN IC was operated being air-cooled by an aluminum heatsink with thermal conductive double-sided tape (the thermal conductivity is $0.8\ \mathrm{W/m \cdot K}$). To acquire the performance of this heat dissipation system, we verified the thermal resistance between the storage of the GaN IC and ambient air.

III. Measurement results

In this section, the correlation between the storage temperature and calorific values of M1 are mainly evaluated to verify the safety range of continuous operation in terms of the storage temperature.

A. Circuit for Measurement

To simply evaluate the continuous operation tolerance of M1, the power GaN HEMT, we implemented the GaN IC

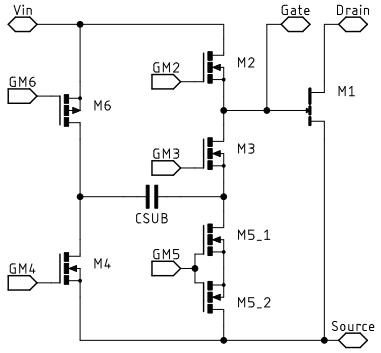


Fig. 1: Proposed 3-level gate driver (M1 is a power GaN HEMT)

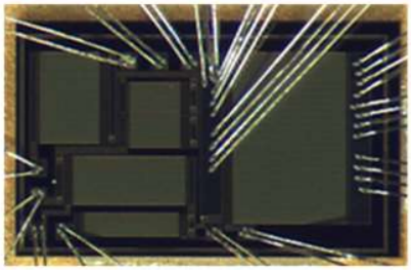


Fig. 2: GaN IC chip on which Fig. 1 components except for M6 and CSUB are integrated

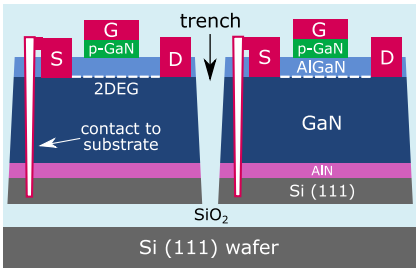


Fig. 3: Cross section of two isolated HEMTs by GaN-on-SOI process [13]

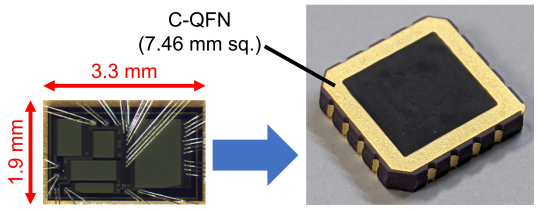


Fig. 4: GaN IC implemented in C-QFN package.

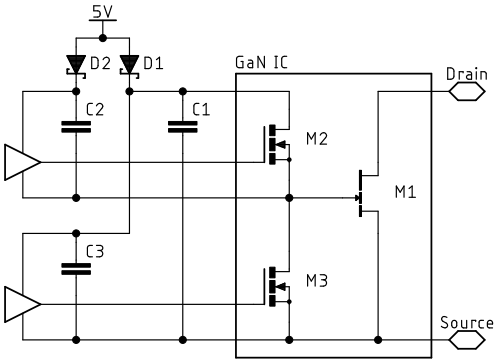


Fig. 5: Gate driver circuit for M1

into a typical asynchronous buck converter without M4 and external p-MOS M6. M2 and M3 were used to drive the M1 gate because the M1 GATE terminal is for the purpose of gate voltage measurement. M5 is always in on-state in order to short the M1 source and the M3 source terminals. Then, the GaN IC's internal circuit and M1 driving circuit are expressed as the circuit shown in Fig. 5. In this work, the M2 source and the M3 source are floating because M1 is the high side switch of the buck converter. Therefore, the bootstrap circuit, which is composed of two Schottky barrier diodes (ROHM Semiconductor, RB168MM150TFTR) and three capacitors, is applied for M2, M3 and the whole phase leg. C1 is 1 μF, and C2 and C3 are 100 nF. The pre-driver for M2 and M3 is an isolated gate driver IC (Silicon Labs, Si8274GB). The high/low side drivers synchronize with an input PWM signal and they have 20 ns deadtime.

Fig. 6 shows the schematic of the buck converter for evaluating the GaN IC. The constant parameters of this circuit are shown in TABLE I. Output current I_{out} and switching frequency f_{sw} are parameters used to change the measuring condition. To decide the range of these parameters, we verified the GaN IC's breakdown point with some variety of output current of the buck converter by measuring the GaN IC storage temperature. To measure in stable conditions, the GaN IC storage temperature was measured after 5 minutes operation. First, output current range was checked with 1 MHz switching frequency. TABLE II shows that the GaN IC was broken at 3.0 A output current. When the GaN IC was broken, the duration of continuous operation was less than 10 seconds

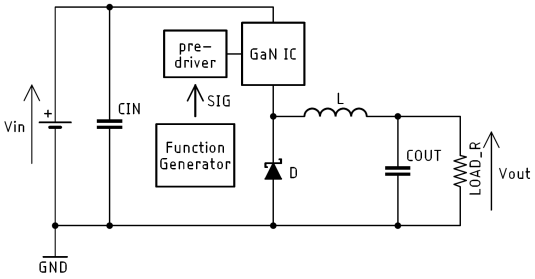
TABLE I: Circuit parameters of the buck converter

Circuit parameter		min.	typ.	max.	Unit
Input Voltage	V_{in}	–	48	–	V
Output Voltage	V_{out}	–	12	–	V
Input Capacitance	C_{in}	–	9.6	–	μF
Output Capacitance	C_{out}	–	13.7	–	μF
Inductance	L	–	22	–	μF
Output current	I_{out}	0.24	–	2.0	A
Switching Frequency	f_{sw}	1.0	–	2.0	MHz

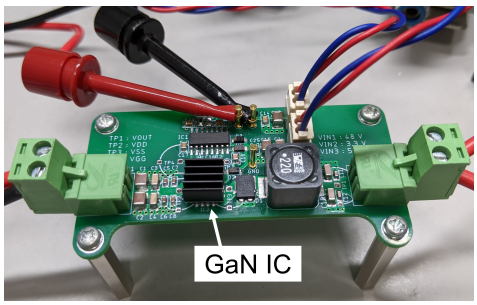
(the exact value of duration and the storage temperature could not be acquired). Therefore, the GaN IC storage temperature went below 64°C. In a similar way, the range of switching freuency was decided with output current fixed to 1.0 A. In condition of $f_{\mathrm{sw}} = 2,0$ MHz, the storage temperature rose upto 61°C which is safe temperature for the GaN IC.

TABLE II: Breakdown Point Verification Result

Output Current	GaN IC Temp.
0 A (idle)	30°C
0.24 A	37°C (+7°C)
1.0 A	46°C (+16°C)
2.0 A	64°C (+34°C)
3.0 A	(breakdown)



(a) Simplified schematic



(b) Board for measurement

Fig. 6: Buck converter for evaluating the GaN IC

B. Heat Generation Model

In an asynchronous buck converter, heat generation at the high side switch is caused by conduction loss and switching loss. Ideal waveforms of V_{DS} and I_{D} at the high side switch is shown in Fig. 7. Based on the waveforms of V_{DS} and I_{D}, conduction loss P_{co} and switching loss P_{sw} are approximately given by the following equations.

$$P_{\mathrm{co}} = R_{\mathrm{on}} \left(I_{\mathrm{out}}^2 + \frac{\Delta I_{\mathrm{L}}^2}{12} \right) \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \tag{1}$$

$$P_{\mathrm{sw}} = \frac{1}{6} (I_{\mathrm{Lv}} t_{\mathrm{fall}} + I_{\mathrm{Lp}} t_{\mathrm{rise}}) V_{\mathrm{in}} f_{\mathrm{sw}} \tag{2}$$

Because this test circuit has no internal current prove points, ΔI_{L} could not be measured. Then the following equation was used to acquire ΔI_{L}.

$$\Delta I_{\mathrm{L}} = \frac{V_{\mathrm{out}}(V_{\mathrm{in}} - V_{\mathrm{out}})}{L f_{\mathrm{sw}} V_{\mathrm{in}}} \tag{3}$$

C. Measurement and Evaluation

1) M1 on-state resistance R_{on}: As shown in Fig. 7, R_{on} can be calculated from the on-state mean value of V_{DS} and I_{out}. Then we acquired R_{on} from waveforms of V_{DD} and V_{SS} in the condition of $I_{\mathrm{out}} = 2$ A and $f_{\mathrm{sw}} = 1$ MHz. The waveforms are shown in Fig. 8 and the mean value of on-state V_{DS} is 150 mV. Then, R_{on} is 75 mΩ.

2) The GaN IC storage temperature: The total calorific value of the GaN IC P_{hg} and the storage temperature T_{s} were measured with I_{out} and f_{sw} varied as shown in TABLE III. The T_{s} values in the brakets mean increments from the idle temperature (30°C). Fig. 9 shows the correlation

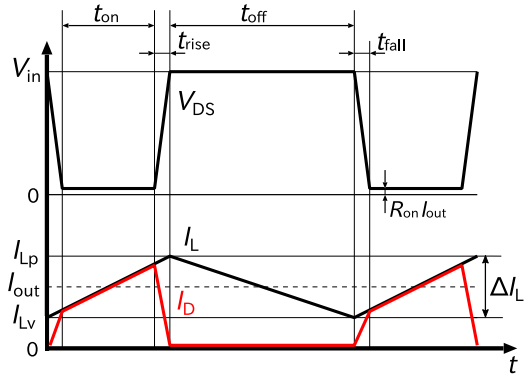


Fig. 7: Ideal waveforms of V_{DS} and I_{D} at high side switch

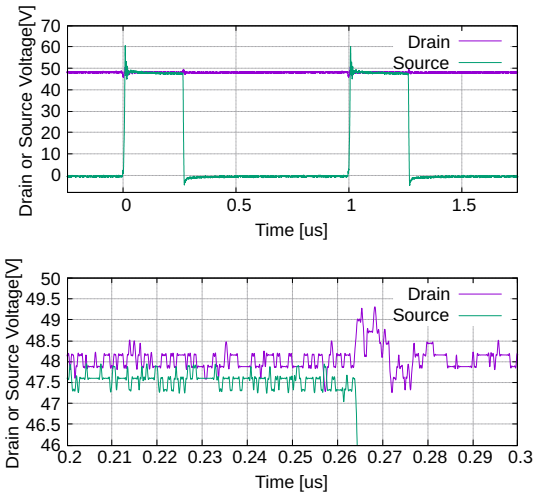


Fig. 8: Waveforms of V_{DD} and V_{SS}

between T_{s} increment and P_{hg}. The gradient of the linear fit is 0.136, that means the storage-to-ambient thermal resistance θ_{ca} is 136 K/W in this system. However, the maximum junction temperature $T_{\mathrm{j,max}}$ and the junction-to-storage thermal resistance θ_{js} are also needed to measure the maximum operation area. To measure $T_{\mathrm{j,max}}$, accurate breakdown T_{j} of the GaN IC should be verified with the chip implemented in an unsealed package and with T_{j} slowly raised up. For example, the conduction loss at $I_{\mathrm{out}} = 0.24$ A is 1.2 mW. It can realize a slow temperature increment despite the high thermal conduction between the bare chip and ambient air. On the other hand, θ_{js} is given by the following equation using $T_{\mathrm{j,max}}$, $T_{\mathrm{c,max}}$, P_{max} and $\theta_{\mathrm{ca}} = 136$ K/W.

$$\theta_{\mathrm{js}} = \frac{T_{\mathrm{j,max}} - T_{\mathrm{s,max}}}{P_{\mathrm{max}}} \tag{4}$$

To measure θ_{js}, the breakdown storage temperature $T_{\mathrm{s,max}}$ and the load power P_{max} using the C-QFN package should be verified in a stable condition. In this case, a linear regulator using the GaN IC is a simple and efficient method because it can load any power to M1 without some complicated circuits or controls.

TABLE III: Measured parameters t_{fall}, t_{rise}, T_{s} and Calculated parameters ΔI_{L}, P_{co}, P_{sw}, P_{hg}

I_{out} [A]	f_{sw} [MHz]	t_{fall} [ns]	t_{rise} [ns]	ΔI_{L} [A]	P_{co} [mW]	P_{sw} [mW]	P_{hg} [mW]	T_{s} [°C]
0.24	1.0	18.52	4.57	0.409	1.34	21.5	22.9	37 (+7)
	1.5	22.44	4.62	0.273	1.20	48.7	49.9	40 (+10)
	2.0	24.33	4.60	0.205	1.15	78.7	79.9	44 (+14)
1.0	1.0	6.49	4.74	0.409	19.0	87.0	106	46 (+16)
	1.2	6.56	4.73	0.341	18.9	105	124	48 (+18)
	1.4	6.70	4.74	0.292	18.9	125	144	52 (+22)
	1.6	6.78	4.69	0.256	18.9	143	162	55 (+25)
	1.8	6.96	4.81	0.227	18.8	166	185	58 (+28)
	2.0	7.01	4.84	0.205	18.8	186	205	61 (+31)
2.0	1.0	3.58	5.33	0.409	75.3	145	221	64 (+34)

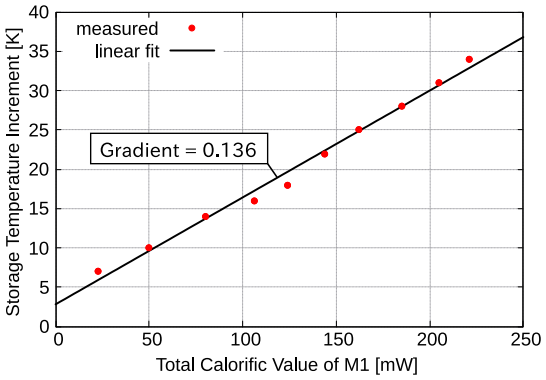


Fig. 9: Measurement result of T_{s} increment and P_{hg}

TABLE IV: Modified circuit parameters of the buck converter

Circuit parameter		Value	Unit
Input Voltage	V_{in}	48	V
Output Voltage	V_{out}	12	V
Input Capacitance	C_{in}	4.4	μF
Output Capacitance	C_{out}	40.8	μF
Inductance	L	3.3	μF
Typ. Output current	$I_{\mathrm{out,typ}}$	2.0	A
Typ. Switching Frequency	$f_{\mathrm{sw,typ}}$	1.0	MHz

IV. Downsizing the Converter

In the previous section, we verified that the GaN IC can continuously operate for minutes in the limited condition. Then we designed an asynchronous buck converter using the GaN IC with the operation condition and the optimised circuit parameters. This attempt aims to downsize the converter used for the previous measurement and realize a small and high density power converter. Modified circuit parameters are shown in TABLE IV and a manufactured board is shown in Fig. 10. The low side switch Schottky barrier diode was changed to NRVTS360ETFS (ON Semiconductor). The thickness of the main circuit is 8.1 mm then the volume of main circuit is 1.86 cm^3. Therefore, this circuit achieves 12.9 $\mathrm{W/cm}^3$ power density in the condition of $I_{\mathrm{out}} = 2.0$ A.

Because the rise-time t_{rise} and the fall-time t_{fall} of the modified circuit were shorter than the measurement circuit as a secondary effect of changing the circuit parameters and components, the circuit became able to safely operate upto $f_{\mathrm{sw}} = 1.4$ MHz at $I_{\mathrm{out}} = 2.0$ A according to the calculated value of P_{hg}. Moreover, the circuit could operate

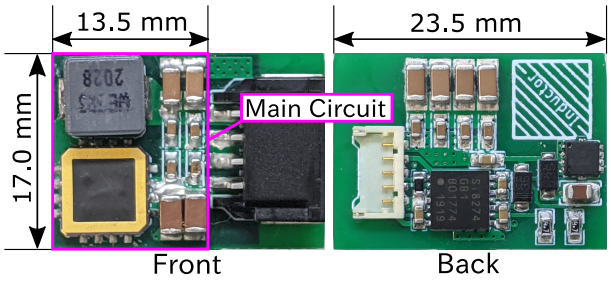


Fig. 10: Modified buck converter board

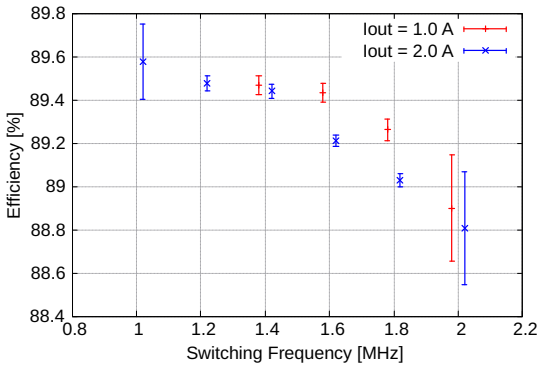


Fig. 11: Power conversion efficiency with f_{sw} varied

up to $f_{\mathrm{sw}} = 2.0$ MHz at $I_{\mathrm{out}} = 2.0$ A. TABLE V shows the parameter settings and the acquired parameters in the CCM measurement of the optimised circuit.

Fig. 11 shows the measurement result of the power conversion efficiency at $I_{\mathrm{out}} = 1.0$ A with f_{sw} varied from 1.4 MHz to 2.0 MHz and at $I_{\mathrm{out}} = 2.0$ A with f_{sw} varied from 1.0 MHz to 2.0 Mhz. In this range of I_{out} and f_{sw}, the power conversion efficieny was approximately from 88.8% to 89.6% and has negative correlation to the switching frequency because switching loss is propotional to switching freqency. However the transition is non-linear because of ΔI_{L}, t_{fall}, t_{rise} and other power losses which were not measured such as the loss from charging the parasitic capacitance of M1, the reverse recovery loss of the Shottky barrier diode, the conduction loss of the inductor and etc.

TABLE V: Parameter settings, measured parameters t_{fall}, t_{rise} and calculated parameters ΔI_{L}, P_{co}, P_{sw}, P_{hg} for the optimised circuit

I_{out} [A]	f_{sw} [MHz]	t_{fall} [ns]	t_{rise} [ns]	ΔI_{L} [A]	P_{co} [mW]	P_{sw} [mW]	P_{hg} [mW]
1.0	1.4	3.36	2.68	1.95	24.7	60.2	84.9
	1.6	3.61	2.70	1.71	23.3	70.8	94.1
	1.8	3.79	2.76	1.51	22.3	83.1	105
	2.0	4.01	2.82	1.37	21.7	96.3	118
2.0	1.0	2.27	2.79	2.73	86.6	86.6	173
	1.2	2.39	2.91	2.27	83.1	107	191
	1.4	2.47	3.00	1.95	80.9	128	209
	1.6	2.54	3.07	1.71	79.6	149	229
	1.8	2.60	3.41	1.51	78.6	182	261
	2.0	2.76	4.06	1.37	77.9	232	310

V. Conclusion

In this paper, the tolerance for continuous operation of our proposed GaN IC was evaluated with the GaN IC applied in an asynchronous buck converter. From the result of breakdown point verification, the safely operation area of the storage temperature was below $64^{\circ}\mathrm{C}$. To acquire the storage temperature and the calorific value of the GaN IC in the stable condition, they were measured after the buck converter operated continuously for 5 minutes. To change the calorific value of the GaN IC, the output current I_{out} and the switching frequency f_{sw} were varied. The correlation between the calorific value and the storage temperature shows that the thermal resistance between the GaN IC storage and ambient air θ_{sa} is $136\ \mathrm{K/W}$. This parameter is useful to design the heat dissipation equipment for some converters using the GaN IC. However, the junction-to-storage thermal resistance θ_{js} is needed to estimate the maximum operation area of the GaN IC. Moreover, the GaN IC could realize a small and high power density converter with the optimised circuit parameters. The volume of the main circuit is $1.86\ \mathrm{cm}^3$, the power density was $12.9\ \mathrm{W/cm}^3$ at $I_{\mathrm{out}} = 2.0\ \mathrm{A}$ and the power conversion efficiency was approximately from 88.8% to 89.6%.

Acknowledgment

This research is supported by Consortium for GaN Research and Applications and Technical Reseach Funding Program for Young Reseachers. We acknowledge Thibault Cosnier ' s help for the PDK.

References

[1] K. J. Chen, O. Häberlen, A. Lidow, C. l. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "Gan-on-si power technology: Devices and applications," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 779–795, 2017.

[2] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014.

[3] M. Wolf, O. Hilt, and J. Würfl, "Gate control scheme of monolithically integrated normally off bidirectional 600-v gan hfets," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3878–3883, 2018.

[4] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An analytical model for false turn-on evaluation of gan transistor in bridge-leg configuration," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–6.

[5] W. Lee, D. Han, W. Choi, and B. Sarlioglu, "Reducing reverse conduction and switching losses in gan hemt-based high-speed permanent magnet brushless dc motor drive," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 3522–3528.

[6] Z. Dong, Z. Zhang, X. Ren, X. Ruan, and Y.-F. Liu, "A gate drive circuit with mid-level voltage for gan transistors in a 7-mhz isolated resonant converter," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 731–736.

[7] X. Ren, D. Reusch, S. Ji, Z. Zhang, M. Mu, and F. C. Lee, "Three-level driving method for gan power transistor in synchronous buck converter," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 2949–2953.

[8] Z.-L. Zhang, Z. Dong, D.-D. Hu, X.-W. Zou, and X. Ren, "Three-level gate drivers for egan hemts in resonant converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5527–5538, 2017.

[9] J. Nagao, U. Chatterjee, X. Li, J. Furuta, S. Decoutere, and K. Kobayashi, "An e-mode p-gan hemt monolithically-integrated three-level gate driver operating with a single voltage supply," *IEICE Electronics Express*, vol. 18, no. 6, pp. 20 210 059–20 210 059, 2021.

[10] Y. Yamashita, S. Stoffels, N. Posthuma, K. Geens, X. Li, J. Furuta, S. Decoutere, and K. Kobayashi, "Monolithic integration of gate driver and p-gan power hemt for mhz-switching implemented by e-mode gan-on-soi process," *IEICE Electronics Express*, vol. 16, no. 22, pp. 20 190 516–20 190 516, 2019.

[11] X. Li, M. Van Hove, M. Zhao, K. Geens, V.-P. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, "200 v enhancement-mode p-gan hemts fabricated on 200 mm gan-on-soi with trench isolation for monolithic integration," *IEEE Electron Device Letters*, vol. 38, no. 7, pp. 918–921, 2017.

[12] X. Li, M. Van Hove, M. Zhao, K. Geens, W. Guo, S. You, S. Stoffels, V.-P. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, "Suppression of the backgating effect of enhancement-mode p-gan hemts on 200-mm gan-on-soi for monolithic integration," *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 999–1002, 2018.

[13] X. Li, N. Amirifar, K. Geens, M. Zhao, W. Guo, H. Liang, S. You, N. Posthuma, B. D. Jaeger, S. Stoffels, B. Bakeroot, D. Wellekens, B. Vanhove, T. Cosnier, R. Langer, D. Marcon, G. Groeseneken, and S. Decoutere, "Gan-on-soi: Monolithically integrated all-gan ics for power conversion," in *2019 IEEE International Electron Devices Meeting (IEDM)*, 2019, pp. 4.4.1–4.4.4.

[14] A. Magnani, T. Cosnier, N. Amirifar, M. Zhao, X. Li, K. Geens, and S. Decoutere, "Thermal resistance characterization of gan power hemts on si, soi, and poly-aln substrates," in *2020 21st International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2020, pp. 1–6.