A Low Surge Voltage and Fast Speed Gate Driver for SiC MOSFET with Switched Capacitor Circuit

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***Abstract*—We propose a low surge voltage and fast speed gate driver with switched capacitor circuit for Silicon-Carbide (SiC) MOSFET. Because of the high switching frequency of SiC MOSFET, the surge voltage becomes a serious problem which cause a high switching loss and may break the SiC MOSFET. There is a trade-off between surge voltage and switching speed. It is hard to fulfill both of them at the same time by using conventional gate drivers. With the switched capacitor circuit, the proposed gate driver can reduce the surge voltage by 17.2% and the switching time by 8.4% at the turn-off transient. Compared to conventional gate drivers without the switched capacitor circuit, the proposed gate driver can generate negative gate-source voltage without any isolated power supply.**

***Keywords*—SiC MOSFET, switched capacitor, gate driver**

I. Introduction

Because of the wide band-gap of SiC material, SiC MOSFET has a lot of advantages, for instance, higher frequency, lower on resistance and higher operating temperature. However, there are also some problems to limit the application of SiC MOSFETs, for instance, they have a large input capacitance, a high threshold voltage and a high surge voltage. Because of these problems, SiC MOSFETs are difficult to be driven compared to conventional Si MOSFETs. Therefore it is necessary to design a gate driver for SiC MOSFETs [1].

There is a trade-off between switching time and surge voltage [2]. A gate resistor is used to control switching time and surge voltage in the conventional gate driver. Lower gate resistance leads to higher switching speed and higher surge voltage. The fast switching speed and low surge voltage can not be obtained at the same time by using conventional gate drivers.

Several gate drivers have been proposed to reduce the switching time or surge voltage [3] [4] [5] [6] [7]. However, none of them reduce the switching time and surge voltage at the same time. A gate driver [8] was proposed which can output positive and negative voltage, however, because of the high input capacitance which consists of input capacitance of MOSFET and capacitance in gate driver circuit, it's turn-on switching speed is slow. Because the negative and positive output voltage are equivalent, they can not be changed independently, it can not drive SiC MOSFETs with the range of Vgs is from -6 V to 25 V, generally. Another gate driver [9] was proposed for SiC MOSFETs, it can drive SiC MOSFET with low loss and low noise at turn-on transient, however at turn-off transient it just use the speed up capacitor to obtain high switching speed. It can not drive an SiC MOSFET with low noise at the turn-off transient.

In this paper, a gate driver with a switched capacitor circuit is proposed to reduce both of surge voltage and switching time at the turn-off transient. The proposed gate driver generates negative gate-source voltage at the turn-off transient. The negative and positive gate-source voltage can be controlled independently. The proposed gate driver pulls down the gate voltage of the SiC MOSFET quickly without causing a high surge voltage. It is more simple and stable than conventional gate drivers, because it generates negative gate voltage without any isolated power supply.

In the section Ⅱ, we explain the principle of the proposed gate driver. In the section Ⅲ, we give the circuit and operation of the proposed gate driver. In the section Ⅳ, we measure and evaluate the switching time and the surge voltage by the double pulse method.

II. Principle of The Proposed Gate Driver

The proposed gate driver with a switched capacitor circuit can drive SiC MOSFET with high speed and low surge voltage. Negative gate-source voltage and a capacitor between gate and source of SiC MOSFET are two important factors to fulfill high switching speed and low surge voltage in our proposed gate driver. The condition when switched capacitor circuit is used is shown in Fig. 1(b), is compared to the condition without switched capacitor circuit as shown in Fig. 1(a).

A. Effect of Negative Gate-source Voltage

Negative gate-source voltage of SiC MOSFET play an important role at the turn-off transient. Negative gate-source voltage can quickly pull down the gate voltage, the Vgs of SiC MOSFET can fall under Vth faster than without negative gate-source voltage. Negative voltage can improve the noise tolerance of MOSFET to suppress turning it unintentionally. The negative gate-source voltage makes the capacitance of Cgd becoming lower which can reduce the ringing voltage.

B. Effect of Capacitor between Gate and Source

When the MOSFET turns off, Vs rises, the stray capacitor Cgd of MOSFET is charged. The charged stray capacitor Cgd generates miller current which flows through MOSFET to ground. When the miller current goes through the gate resistor R_G of the conventional gate drivers, it causes a voltage $\triangle$V as shown in Fig. 1(a). $\triangle$V leads to the switching time longer and make some amount of noise.

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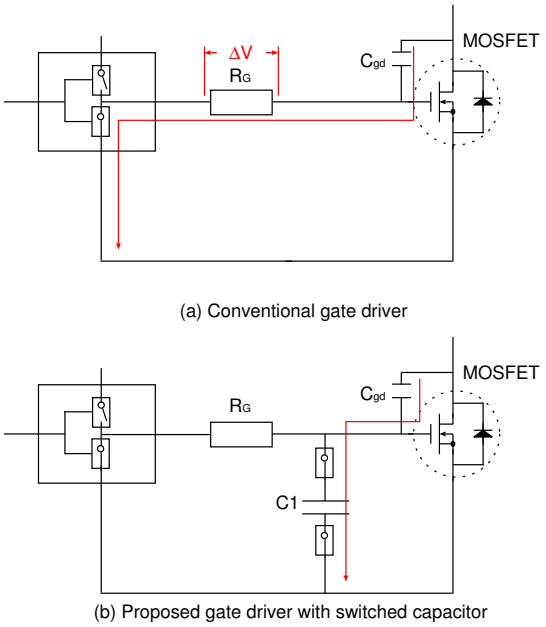

Fig. 1. The influence of miller current (a) conventional gate drivers (b) proposed gate driver with switched capacitor

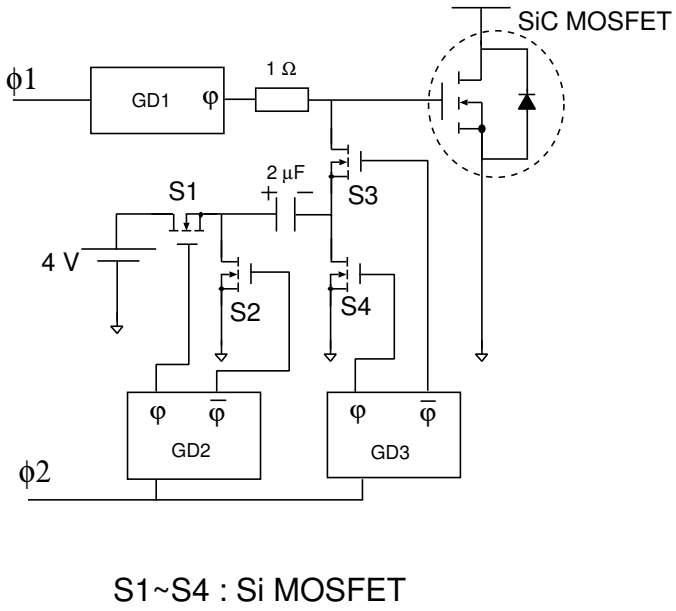

Fig. 2. Schematic of proposed gate driver with switched capacitor circuit.

As shown in Fig. 1(b), at the turn-off transient, the miller current flows through the capacitor C1 instead of flowing through R_G. No voltage drop happens. MOSFET turns off quickly with smaller noise.

III. Schematic and Operation of The Proposed Gate Driver

A. Schematic of the proposed gate driver

Fig. 2 shows the proposed gate driver with the switched capacitor circuit. It consists of three gate drivers, a 2 μF capacitor, a 1 Ω resistor, four switches and a 4 V power supply. Two gate drivers are used to drive switches. Si MOSFETs are used as switches (S1 - S4) which are controlled by the gate drivers GD2 and GD3.

B. Operation of the proposed gate driver

Fig. 3 shows the operation procedure of the proposed gate driver. Fig. 4 shows the control scheme of ϕ1, ϕ2 and Vgs. ϕ1 and ϕ2 are two independent signals. ϕ1 controls the gate driver GD1, while ϕ2 controls the gate drivers GD2 and GD3. ϕ1 and ϕ2 turn to logic low at the same time. A 0.2 μs delay, ϕ2 return to logic high to cut off the switched capacitor circuit.

P0: ϕ1 and ϕ2 are logic high. The gate voltage of MOSFET is over the threshold voltage. S2 and S3 are off, S1 and S4 are on. the switched capacitor is charged by the power supply (V1).

P1: ϕ1 and ϕ2 turn to logic low. The output of gate driver GD1 turns to 0 V. At the same time, S1 and S4 are off, S2 and S3 are on, the capacitor is connected to the gate of the SiC MOSFET. The gate voltage of the SiC MOSFET falls below 0 V.

P2: ϕ2 turns to logic high. S1 and S4 are on, S2 and S3 are off and the capacitor is charged by V1. The gate voltage of the SiC MOSFET returns to 0 V.

P3: ϕ1 turns to logic high, ϕ2 keeps logic high. The gate driver GD1 charges the gate of the SiC MOSFET without the switched capacitor circuit. The gate voltage of the SiC MOSFET rises again.

IV. Experiment and Results

A. Double pulse method

The double pulse method is used to measure the proposed gate driver. we compare the proposed the gate driver with a conventional gate driver without switched capacitor circuit. Commercially available Si MOSFETs are used as the switches. The experimental circuits and definitions of measured parameters are shown in Fig. 5. The duration time of first pulse is 10 μs, the time of the second pulse is 0.5 μs and the delay time between two pulse is 0.5 μs.

B. Experimental results

Fig. 6 depicts the experimental circuit. Fig. 7 shows the experiment results of the conventional and proposed gate drivers by Si MOSFETs as the switches (S1 - S4). Fig. 7 (a) shows the gate-source voltage of the SiC MOSFET. Fig. 7 (b) shows the drain-source voltage of the SiC MOSFET.

At first Vgs of the conventional gate driver and the proposed gate driver fall with the same speed. When Vgs of the conventional gate driver and proposed gate driver fall close to Vth of the SiC MOSFET. The falling speed of conventional gate driver become slow significantly, because the discharging current becoming low caused by the fall of Vgs and the miller current flowing through R_G. However, the falling speed of proposed gate driver keep constant, until the Vgs falls under

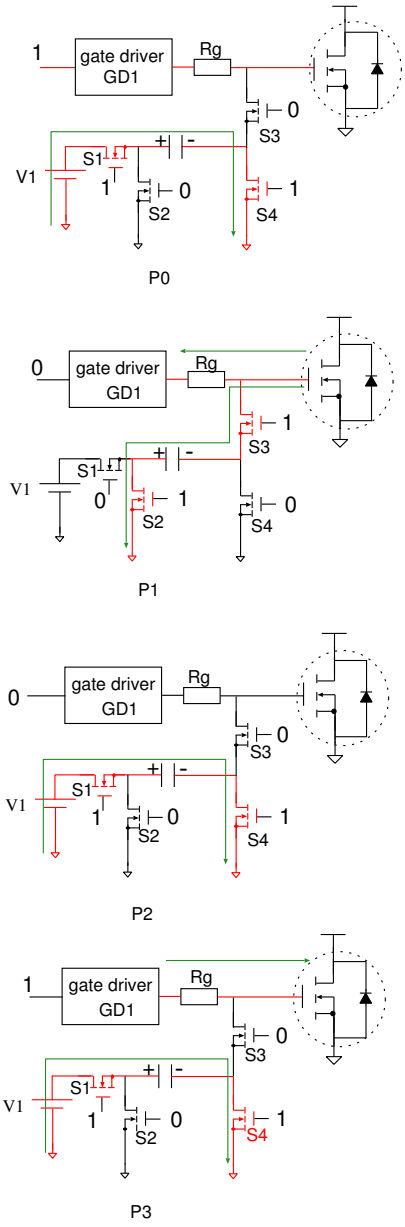

Fig. 3. Operation procedure of the proposed gate driver.

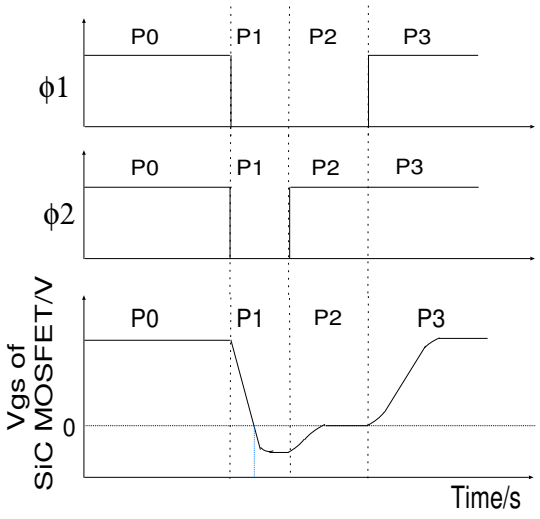

Fig. 4. Control scheme of the proposed gate driver.

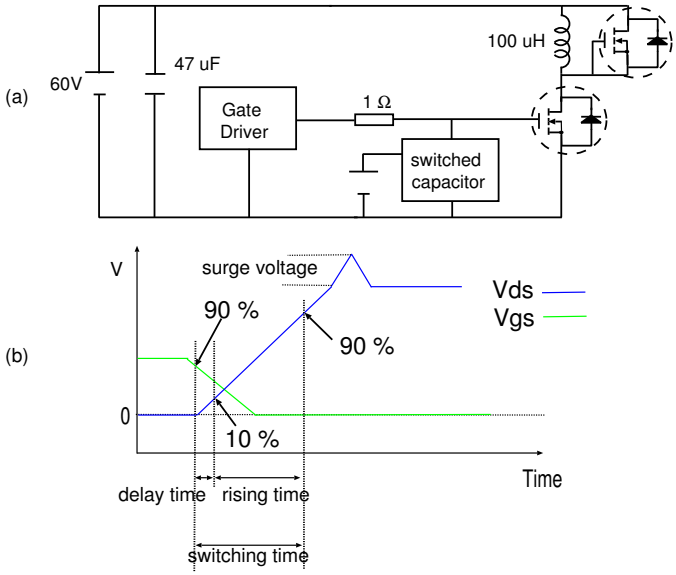

Fig. 5. Double pulse measurement circuit and definitions of measurement value.

−2 V. Therefore, Vgs of the proposed gate driver reaches Vth of SiC MOSFET quicker than the conventional gate driver.

Even though, Vds of the conventional gate driver rises first. Because Vgs of the proposed gate driver reaches the Vth of SiC MOSFET faster, Vds rises quicker than the conventional gate driver.

As shown in Table. I. The proposed gate driver turn-off switching time and surge voltage are 37 ns and 19.2 V. Those of the conventional gate driver are 40.4 ns and 23.2 V. The proposed gate driver reduces switching time by 8.4% and surge voltage by 17.2% at the turn-off transient.

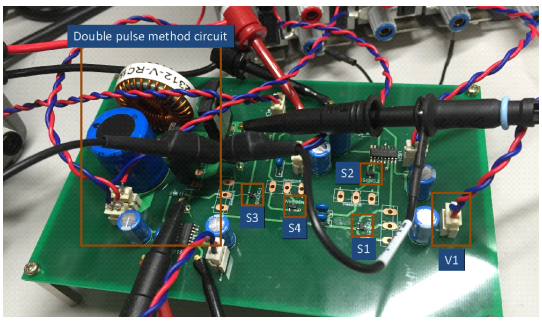

Fig. 6. Proposed gate driver with switched capacitor circuit.

TABLE I
RESULTS OF PROPOSED GATE DRIVER AND CONVENTIONAL GATE DRIVER

	Surge voltage / V	Delay time / ns	Rise time / ns
Proposed	19.2	25.0	12.0
Conventional	23.2	24.0	16.4

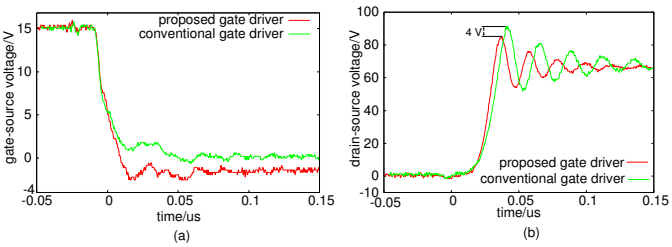

Fig. 7. Gate-source voltage (a) and Drain-source voltage (b) of the proposed gate driver with switched capacitor circuit.

V. CONCLUSION

This paper presents a gate driver with a switched capacitor circuit. The proposed gate driver just consists of capacitor, switches and gate drivers. It produces negative voltage and positive voltage independently.

The proposed gate driver can reduce both of switching time and surge voltage at the turn-off transient. The switching time is reduced by 8.4% and the surge voltage is reduced by 17.2%.

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