Impact of Body-Biasing Technique on RTN-induced CMOS Logic Delay Uncertainty

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Abstract—The impact of Random telegraph noise (RTN) on a CMOS logic circuit is evaluated. Statistical nature of RTN-induced delay fluctuation is described by measuring 1,680 ROs fabricated in a commercial 40 nm CMOS technology. Small number of samples have a large RTN-induced delay fluctuation. It is found that the impact of RTN-induced delay fluctuation becomes as much as 10.4 % under low supply voltage (0.65V) operation. The impact of RTN-induced delay fluctuation tends to be reduced by forward body-biasing technique, but a few ROs do not follow this tendency.

I. INTRODUCTION

Designing reliable systems has become more difficult in recent years[1]. RTN already has a severe impact on CMOS image sensors[2], flash memories[3], and SRAMs[4]. Recently we have shown that RTN also induces performance fluctuation to logic circuits[5]. On the other hand, adaptive body-biasing technique has been widely used to compensate for die-to-die parameter variations[6]. However, the impact of the body-biasing technique on RTN at the circuit level has not been well understood. In this paper, we investigated the impact of body-biasing technique on RTN-induced circuit delay fluctuation.

II. IMPACT OF BODY-BIASING TECHNIQUE ON RTN

Fig. 1 shows the simplest test structure that can emulate the synchronous circuit operation. Combinational circuit delay is emulated by ring oscillator (RO) oscillation frequency. Sequential circuit operation is emulated by D flip-flop (DFF) toggled by the RO output. The power supply for RO (VDD\textsubscript{RO}) and DFF (VDD\textsubscript{DFF}) can be independently controlled. The value of VDD\textsubscript{DFF} is set to be larger than VDD\textsubscript{RO} so as to guarantee the DFF operation. We can also control the substrate bias for pMOS and nMOS. Fig. 2 shows the whole test structure for RTN measurement. RTN-induced delay fluctuation is measured by a ring oscillator (RO) frequency fluctuation. There are 840 same ROs on 2 mm\textsuperscript{2} area and the statistical nature of RTN can be evaluated by the RO array. This chip is fabricated in a commercial 40 nm CMOS technology. All measurements are done at room temperature. Figure 3 shows the histogram of measured \(\Delta F/F_{\text{max}}\) for the whole test structure of Fig. 2 over two chips (1,680 ROs). Here, \(F_{\text{max}}\) is defined as the maximum oscillation frequency and \(\Delta F\) is defined as the maximum frequency fluctuation. \(\Delta F/F_{\text{max}}\) is a good measure for the impact of RTN-induced frequency fluctuation and maximum \(\Delta F/F_{\text{max}} = 10.4\%\).

Figure 4 shows the measurement results of \(\Delta F/F_{\text{max}}\) of different ROs for various substrate bias condition. Substrate bias conditions are categorized as reverse bias case (\(V_{bs-pMOS} = -0.2\text{V}, V_{bs-nMOS} = 0\text{V}\)), normal bias case (\(V_{bs-pMOS} = 0\text{V}, V_{bs-nMOS} = 0\text{V}\)), and forward bias case (\(V_{bs-pMOS} = +0.2\text{V}, V_{bs-nMOS} = +0.2\text{V}\)). 300 ROs in one test structure of Fig. 2 are investigated at VDD\textsubscript{RO}=0.65V. Figure 4 shows ROs that have more than 4 % fluctuation at reverse bias case to evaluate the forward body-bias effect on large \(\Delta F/F_{\text{max}}\) samples (28 ROs). When substrate bias is changed from the reverse bias case to the forward bias case, \(\Delta F/F_{\text{max}}\) tends to decrease. However, for example, \(\Delta F/F_{\text{max}}\) slightly increases in the case of the RO location “68”, “160”...
Data of Two Test Structures (1680ROs)

Fig. 3. The histogram of measured $\Delta F/F_{\text{max}}$ for the whole test structure of Fig. 1 over two chips (1680 ROs).

Fig. 4. $\Delta F/F_{\text{max}}$ of different ROs for various substrate bias condition. ROs that have more than 4% fluctuation at reverse substrate bias case are shown.

and “219” when forward substrate bias is applied. The impact of RTN-induced delay fluctuation tends to be reduced by forward body-biasing technique, but a few ROs do not follow this tendency.

Figure 5 shows the frequency fluctuation of RO location (section No. 1) of Fig. 4 for various substrate bias. Four-state fluctuation due to two traps is clearly observed for the normal substrate bias case. The effect of one of two traps disappears for the forward bias case. Figure 6 shows the frequency fluctuation of RO location 1 of Fig. 4 when pMOS or nMOS is forward biased. The effect of one of two traps disappears only when nMOS is forward biased. Thus the disappeared two-state fluctuation is caused by a single trap in a specific nMOS in the RO.

III. CONCLUSION

Statistical nature of RTN-induced delay fluctuation is described by measuring 1,680 ROs fabricated in a commercial 40 nm CMOS technology. Small number of samples (19 ROs) have a large RTN-induced delay fluctuation of more than 6% of nominal oscillation frequency. The impact of RTN-induced delay fluctuation becomes as much as 10.4% under low supply voltage (0.65V) operation. The impact of RTN-induced delay fluctuation tends to be reduced by forward body-biasing technique, but a few ROs still have a large fluctuation.

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REFERENCES