Impact of RTN and NBTI on Synchronous Circuit Reliability

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***Abstract*—We investigate a synchronous circuit reliability for 65nm−40nm CMOS technology. The impact of Random telegraph noise (RTN) and Negative Bias Temperature Instability (NBTI) on a circuit is evaluated. We found two things. (i) RTN at one or a few stages of a combinational circuit induces a large delay fluctuation under low voltage operation. (ii) LSI lifetime can be extended by utilizing NBTI recovery.**

I. Introduction

Designing reliable systems has become more difficult in recent years. Besides conventional problems such as transistor leakage, the degradation and variation of transistor performance have a severe impact on the dependability of VLSI systems[1]−[3]. Recently it is shown that Random Telegraph Noise (RTN) induces performance fluctuation not only to SRAM but also to logic circuits[4], [5]. Negative-Bias-Temperature-Instability (NBTI) is another reliability concern for CMOS circuits[6], [7]. Remarkable phenomena on NBTI is that degraded performance of a PMOS transistor recovers when the bias-temperature stress to the gate oxide is removed or relaxed[8]. In this paper, We investigate a synchronous circuit reliability for 65nm−40nm CMOS technology. In the following, it is found that RTN at one or a few stages of a combinational circuit induces a large delay fluctuation under low voltage operation. It is also found that LSI lifetime can be extended by NBTI recovery. It is a crucial step for this lifetime extension method to clarify the amount of NBTI recovery. It is generally believed that the measurement delay is set to as short as 1 μs to avoid NBTI recovery for the correct NBTI characterization[9]. So we characterize NBTI by a very short measurement delay (400 ns) NBTI sensor[10].

II. RTN-induced Delay Fluctuation

Fig. 1 shows a typical synchronous circuit structure where a logic path exists between two registers. As shown in Fig. 2, we propose the simplest circuit that emulates the synchronous circuit operation. Combinational circuit delay is represented by the oscillation frequency of a ring oscillator (RO). Register operation is represented by D-FF that is toggled by the RO output. The power supply for RO and D-FF can be independently controlled. There are 1680 same samples of Fig. 2 on each chip. Measurement results of the oscillation frequency at VDD_RO=0.65V show the large 2-state fluctuation that is induced by RTN at one or a few stages of the RO (Fig. 2). For low voltage (0.65V) operation, the delay fluctuation of a combinational circuit can be large (5 % of the oscillation

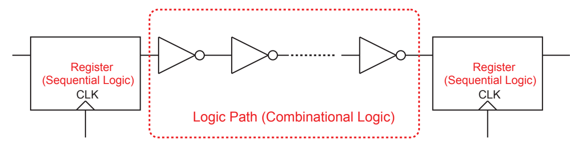

Fig. 1. Typical synchronous circuit structure.

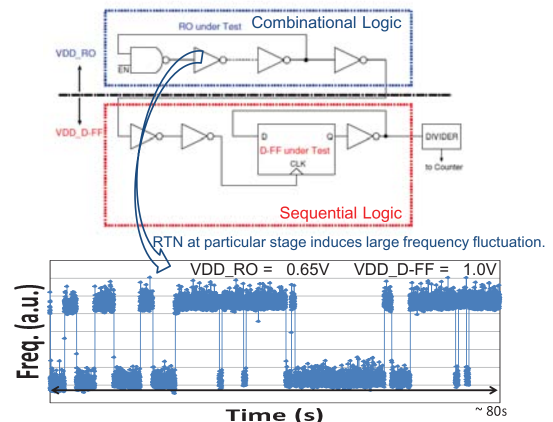

Fig. 2. The simplest circuit that emulates the synchronous circuit operation is shown. Small number of the measurement results of the oscillation frequency at VDD_RO=0.65V show the large 2-state fluctuation that is induced by RTN at one stage of the RO.

frequency in Fig. 2) and cannot be ignored with respect to the process variation. The RO of Fig. 2 is a 7-stage RO and it is not realistic that all transistors in the RO fluctuates as much as 5 % by RTN simultaneously. It is found that even if the RTN amplitude of each transistor is small, delay fluctuation at one or a few stages of the RO by RTN can induce large oscillation fluctuation under low voltage operation.

III. Lifetime Extension by NBTI-Recovery

Fig. 3 shows the degradation of oscillation frequency of a ring oscillator that is caused by NBTI and Hot Carrier Injection (HCI). The degradation follows power law and the propagation delay of a combinational circuit increases due to NBTI and HCI. Fig. 4 shows that an LSI performance degrades with time and finally reaches to its lifetime, for example, 10 years that is defined by the lower limit of LSI performance. If LSI performance is recovered with NBTI recovery, its lifetime can be further extended as shown in Fig. 4. Fig. 5 shows that

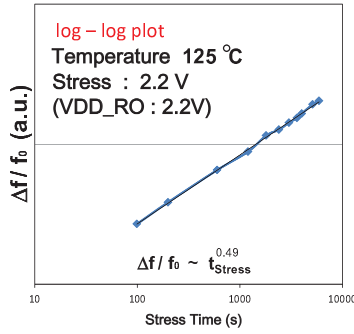

Fig. 3. The degradation of oscillation frequency of a ring oscillator that is caused by NBTI and Hot Carrier Injection (HCI).

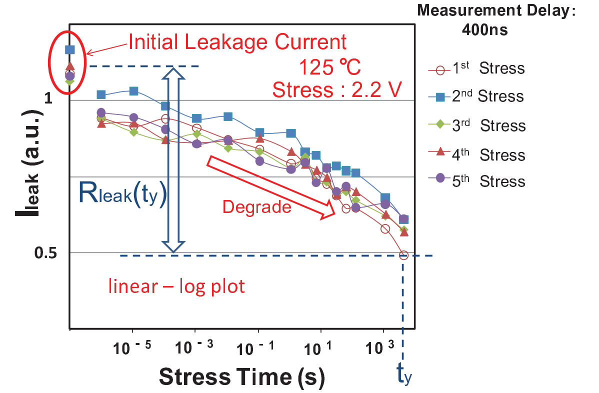

Fig. 5. The off-leak current decreases with stress time compared to its initial value. The recoverable component measured by off-leak current remains almost constant after repeatedly added NBTI stress.

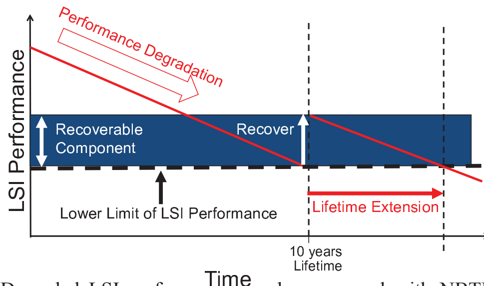

Fig. 4. Degraded LSI performance can be recovered with NBTI recovery that leads to LSI lifetime extension.

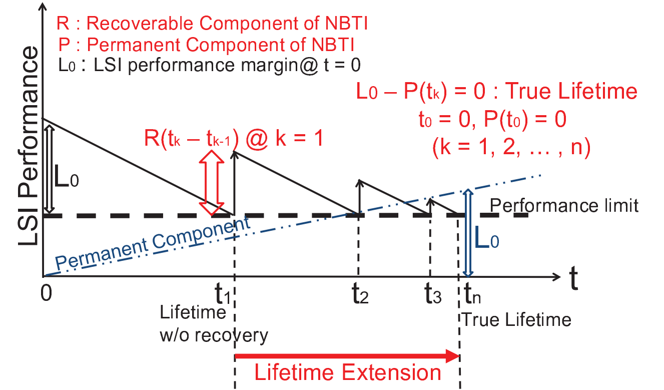

Fig. 6. The concept of a circuit operation to extend its lifetime. LSI performance can be repeatedly recovered until $L_0 - P(t)$ reaches to zero.

NBTI degradation is evaluated by PMOS off-leak current[11]. The off-leak current decreases with stress time compared to its initial value. Although NBTI stress is repeatedly (5 times for Fig. 5) added to the same device, the initial leakage current remains almost same. This means the recoverable component measured by off-leak current remains almost constant after repeatedly added NBTI stress. Fig. 6 shows the proposed LSI lifetime extension method by utilizing the recoverable component measured as in Fig. 5. In Fig. 6, $R(t)$ is the recoverable component and $P(t)$ is the permanent degradation of NBTI. L_0 is the LSI performance margin at $t = 0$. Permanent component, $P(t)$, increases gradually with stress time t (conceptually shown in Fig. 6) and LSI performance can be recovered by $R(t_k - t_{k-1})$ at $t = t_k$. Shortly before LSI reaches to its lifetime at $t = t_1$, LSI performance can be recovered by $R(t_1)$. LSI performance can be repeatedly recovered until $L_0 - P(t) = 0$. The amount of $L_0 - P(t)$ gradually decreases because $P(t)$ gradually increases with time. When power supply, VDD, becomes lower the true lifetime can be further extended.

IV. Conclusion

It is shown that RTN and NBTI have a severe impact on synchronous logic circuit performance. RTN at one or a few stages of a RO induces a large delay fluctuation under low voltage operation. Although LSI performance is degraded by NBTI, LSI lifetime can be extended by utilizing NBTI recovery and recoverable component is measured by NBTI sensor circuit with 400 ns measurement delay.

Acknowledgment

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