Extracting Voltage Dependence of BTI-induced Degradation without Temporal Factors by Using BTI-Sensitive and BTI-Insensitive Ring Oscillators

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***Abstract*—Measuring bias temperature instability (BTI) by ring oscillators (ROs) is frequently used. However, the performance of a semiconductor chip is fluctuated dynamically due to bias, temperature and etc. BTI-sensitive and -insensitive ROs are implemented in order to extract BTI-induced degradation without temporal fluctuation factors. A test chip including those 840 ROs was fabricated in a 65 nm process. BTI-induced degradation without temporal fluctuation was successfully measured by subtracting results of BTI-insensitive ROs from those of BTI-sensitive ones. Extraction of BTI-induced degradation is useful in any supply voltage. Performance degradation of NMOS and PMOS transistors mainly due to BTI increases along power law function and fitting parameters decreases as the supply voltage decreases.**

***Index Terms*—Bias Temperature Instability (BTI), voltage dependence, Negative BTI (NBTI), Positive BTI (PBTI), Ring Oscillator (RO)**

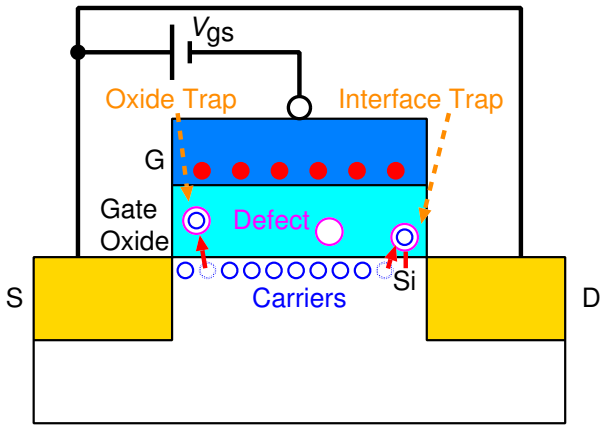

Fig. 1. Atomistic trap-based BTI (ATB) model. BTI occurs when defects trap carriers.

I. Introduction

DEVICE sizes of semiconductor chips have been shrinked with the Moore's law [1]. It has brought a lot of advantages, for example, high-performance and low-power electronic gadgets such as smartphones, smart watches and so on. However, reliability problems have appeared in nanometer-scale devices. Particularly, bias temperature instability (BTI) has become a significant concern with the miniaturization of the device size [2]. BTI is one of aging degradation. Transistor performance is degrading with time due to BTI, which results in decreasing timing margins of implemented circuits. BTI-induced degradation accelerates as voltage and temperature increase. BTI is a serious reliability issue that shortens the lifetime of circuits.

BTI measurement circuits to extract BTI-induced degradations without temporal fluctuations are required because measurement results include fluctuation factors from ambient environments. Our motivation is to extract degradation rates from only BTI-induced degradation by comparing the BTI-sensitive with the BTI-insensitive ring oscillators (ROs). It is impossible to remove BTI-induced degradation in random logic circuits including processors or hardware accelerators since input pins are not fixed. It is important to estimate BTI-induced degradation accurately by the proposed method.

BTI-sensitive and -insensitive ROs are used to extract BTI-induced degradation without temporal factors. The fluctuation factors are removed by subtracting results of those two type ROs. Our research focused on the extracting BTI-induced degradation at only 2.0 V supply voltage in ICMTS 2019 [3].

In this paper, BTI-induced degradation are measured from nominal 1.0 V to 2.0 V using BTI-sensitive and -insensitive ROs. The measurement results are fitted and degradation factors are extracted from the fitting curves. This paper shows BTI-sensitive and -insensitive ROs are useful to extract the degradation in any supply voltage.

We explain BTI in section II. Section III introduces related work of BTI. Section IV shows the structures of those ROs. In section V, measurement results are presented. Finally, section VI shows our conclusion.

II. Bias Temperature Instability (BTI)

Bias temperature instability (BTI) is one of the aging degradations and transistor performance is degrading with time as voltage and temperature increase [4]–[6]. BTI-induced degradation occurs when defects trap carriers. This degradation can be explained by the atomistic trap-based BTI (ATB) model as shown in Fig. 1 [7], [8]. There are oxygen vacancy defects in the gate oxide and dangling bonds in the interface between

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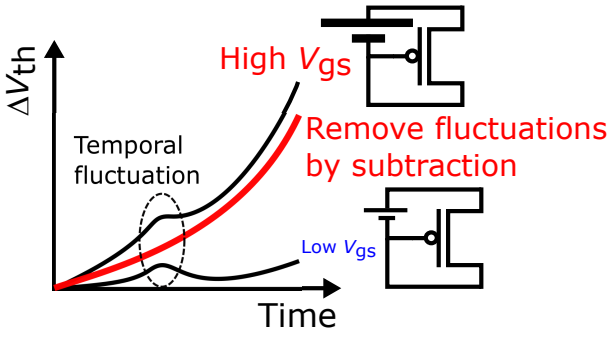

Fig. 2. BTI-induced degradation in Higher and lower gate-source voltage ($V_{\rm gs}$). Temporal fluctuations are removed by subtracting results of Higher and lower $V_{\rm gs}$.

the gate oxide and silicon substrate. When these defects trap carriers, the electric field in the gate oxide decreases and drain-source current decreases. Each defect has an individual time constant to trap a carrier. Those time constants are distributed from 10^{-9} s to 10^{9} s [8]. Particularly, defects with large time constants affect aging degradations induced by BTI. BTI-induced degradation is recovered when carrier emission is promoted as $V_{\rm gs}$ is reduced because trapped carriers in the gate oxide are easily emitted to channel.

There are negative BTI (NBTI) and positive BTI (PBTI). NBTI occurs on PMOS when $V_{\rm gs}$ is negative. Likewise, PBTI is observed on NMOS especially in technologies with high-k (HK) gate dielectrics [9]. NBTI-induced degradation is higher than PBTI-induced degradation in larger than 90 nm process. One of the reasons is assumed that $V_{\rm th}$ sensitivity is different in NMOS and PMOS due to band gap even if same charge is trapped to the gate oxide [10]. However, high-k (HK) gate dielectrics has much defects and PBTI cannot negligible in recent nano-scaled devices.

BTI-induced degradation is accelerated as $V_{\rm gs}$ increases as shown in Fig. 2. Threshold voltage shift ($\Delta V_{\rm th}$) degrades along with Eq. (1) [11],

$$\Delta V_{\rm th} = A * t^{n} * V_{\rm gs}^{m} \ , \qquad (1)$$

where A is the pre-factor, t is the stress time, n is the power law time exponent, and m is the power law voltage acceleration. BTI-induced degradation with higher $V_{\rm gs}$ is larger than that with lower $V_{\rm gs}$. However, temporal fluctuations caused by temperature and voltage affect both ROs. Temperature and voltage are fluctuated by feedback system of measurement instruments. Oscillation frequency of both ROs increases or decreases by the same amount. BTI-induced degradation without temporal factors are extracted by taking difference between BTI-sensitive and -insensitive ROs.

III. Related Work

There are several countermeasures of BTI. BTI-induced degradation is predicted during chip design. Circuit topology is changed to suppress BTI-induced degradation. Critical path changes and delay time decreases by arranging circuit topologies [12].

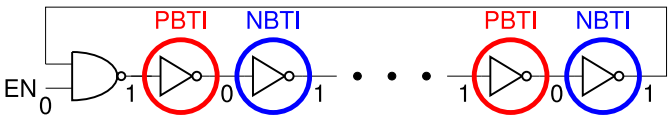

Fig. 3. An inverter-based ring oscillator (RO). PBTI and NBTI occurs in every other inverters when the RO stops. NAND gate is to control oscillation.

After chip design, degradation is monitored and suppressed by body bias in real-time [13], [14]. BTI is suppressed with decreasing supply voltage and applying the forward body bias because forward body bias compensates performance degradation by $V_{\rm gs}$ decrease. However, body bias generators and threshold voltage ($V_{\rm th}$) monitors are required.

Drain current is measured to evaluate BTI-induced degradation of a single transistor [15]. This single transistor measurement is useful to evaluate BTI of individual devices. However, it takes a lot of time to measure huge number of transistors. By using ROs, performance degradation caused by BTI can be evaluated to count the number of oscillations in a short period [16]. However, measurement results include temporal fluctuations such as temperature and voltage fluctuations. Our measurement circuits remove those fluctuations and evaluate accurate BTI-induced degradation by subtracting BTI-sensitive ROs from -insensitive ROs.

IV. Measurement Circuits

An inverter-based RO is shown in Fig. 3. The leftmost NAND-gate controls oscillation by one of input pins (EN) in the NAND-gate. The RO oscillates when EN is high because truth table of the NAND-gate is the same as inverter. When EN is low, the nodes between the inverters are alternately fixed to 0 or 1 and the RO stops oscillation. The RO suffers from BTI when it stops oscillation since $V_{\rm gs}$ is applied to transistors in all gates. The oscillation frequency is degraded when the $V_{\rm th}$ of those transistors is degraded.

PBTI becomes dominant since all inverters are replaced to NAND-gates as shown in Fig. 4. When EN is high, all outputs of NAND-gates are 1. On the other hand, NBTI becomes dominant in the RO composed of NOR-gates as shown in Fig. 5. Oscillation is controlled by ENB. When ENB is high, all outputs of NOR-gates are 0 to accelerate only NBTI.

Sensitivities to BTI can be changed by changing input connections. Figure 6 shows two-types of NAND ROs in the transistor level. NMOS is connected in series from the output terminal to ground (GND). NMOS connected to the output pin is $\rm NMOS_{OUT}$ and that connected to GND is $\rm NMOS_{GND}$. In Fig 6 (a), the gate terminals of $\rm NMOS_{OUT}$ and $\rm NMOS_{GND}$ are connected to EN and the output pins of previous stages, respectively. When EN is low, all output pins of NAND-gates become 0. PBTI is accelerated in $\rm NMOS_{GND}$ in all stages because the $V_{\rm gs}$ become supply voltage (VDD). Here this RO is called the PBTI-sensitive RO.

PBTI is suppressed by changing input connections on the PBTI-insensitive RO as shown in Fig 6 (b). Gate terminals of those NMOS are exchanged between EN and the output pins of previous stages. When EN is low, $V_{\rm gs}$ of $\rm NMOS_{OUT}$ is

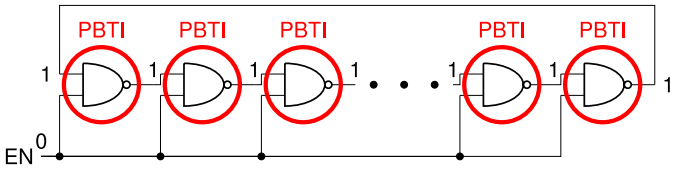

Fig. 4. RO composed NAND gates. PBTI becomes dominant when RO stops.

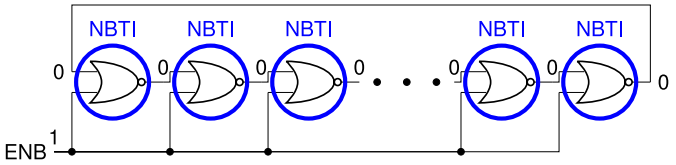

Fig. 5. RO composed NOR gates. NBTI becomes dominant when RO stops.

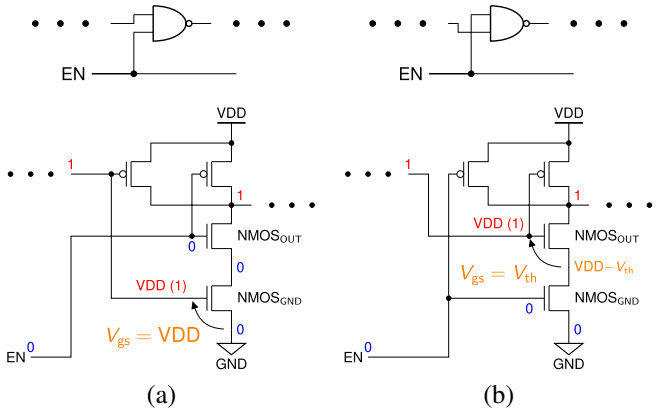

Fig. 6. NAND RO in transistor level. (a) PBTI-sensitive RO. (b) PBTI-insensitive RO.

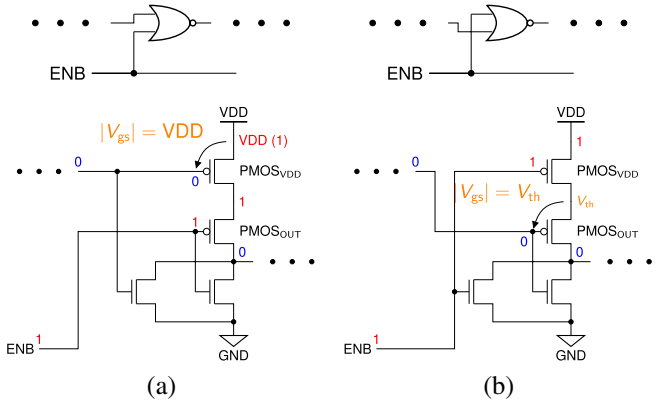

Fig. 7. NOR RO in transistor level. (a) NBTI-sensitive RO. (b) NBTI-insensitive RO.

decreased to threshold voltage ($V_{\rm th}$) instead of VDD. Although PMOS connected to EN suffers from NBTI, the oscillation frequency does not change because it is determined by delay time in MOSFETs connected to the output pins of the previous stages. This PBTI-insensitive RO suppresses PBTI because of lower $V_{\rm gs}$ than that in PBTI-sensitive RO.

Likewise, NBTI is suppressed by arranging the input connections in NOR ROs as shown in Fig. 7. Gate terminals of $\mathrm{PMOS}_{\mathrm{OUT}}$ and $\mathrm{PMOS}_{\mathrm{VDD}}$ are connected to ENB and to

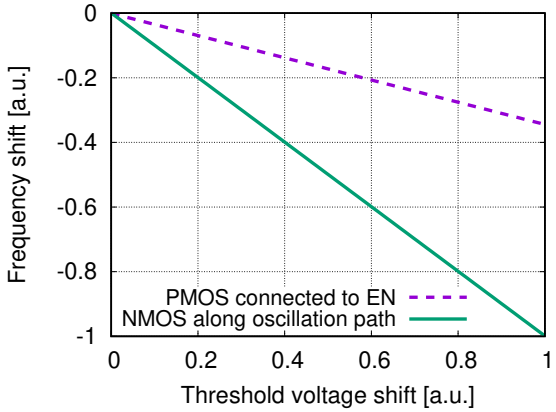

Fig. 8. Simulation results of $V_{\rm th}$ sensitivity. NMOS along the oscillation path have a three times or more sensitivity to $V_{\rm th}$ fluctuation than PMOS connected to EN terminal.

the output pins of previous stages, respectively as shown in Fig. 7 (a). When ENB is high, $\mathrm{PMOS}_{\mathrm{VDD}}$ suffers from NBTI. NBTI is suppressed by changing input connections as shown in Fig. 7 (b). $|V_{\rm gs}|$ of $\mathrm{PMOS}_{\mathrm{OUT}}$ is decreased to $V_{\rm th}$. These ROs are named as the NBTI-sensitive RO and the NBTI-insensitive RO, respectively.

Simulation results obtained by changing the $V_{\rm th}$ of transistors in NAND RO is shown in Fig. 8. The X- and Y-axis show $V_{\rm th}$ shift and the frequency degradation, respectively. Oscillation frequencies proportionally change with $V_{\rm th}$ shift. The oscillation frequency changes when the $V_{\rm th}$ of the PMOS connected to EN shifts as shown by the dotted line in Fig. 8. However, it is one-third or less sensitive than those of NMOS along the oscillation path. In addition, $V_{\rm gs}$ of NMOS connected to EN and PMOS along the oscillation path are 0 during the stress (no oscillation) phase. Thus, PBTI-induced degradation can be measured in NAND RO of Fig. 6. NOR RO of Fig. 7 also has the same tendency in $V_{\rm th}$ sensitivity.

They were fabricated in a 65 nm fully depleted silicon-on-insulator (FDSOI) process and BTI-induced degradations of them were measured. The nominal power supply voltage is 1.0 V in the 65 nm process. We measure the degradation to investigate acceleration of BTI from the nominal voltage.

Table I shows fabricated RO structures and Fig. 9 shows a chip micrograph of the test chip. The chip size is 3×2 mm^2 in which 840×4 11-stage ROs are embedded. The number of ROs is limited by the chip area. The chip is designed to implement as many ROs as possible. Oscillation of ROs is controlled by the oscillation (Osc.) controller and input pins. The number of oscillations is counted by the 16-bit counter. Those controller and counter are mainly composed by standard flip-flops. Each RO has its own controller and counter. They formed a unit that is connected in series. The number of oscillation in counters are measured and oscillation frequencies are calculated by dividing oscillation time.

Our measurement system is shown in Fig. 10. The test chip (Device Under Test, DUT) is measured by LSI tester. An external power supply and a Peltier module are used to apply higher bias and temperature stress. It is difficult to

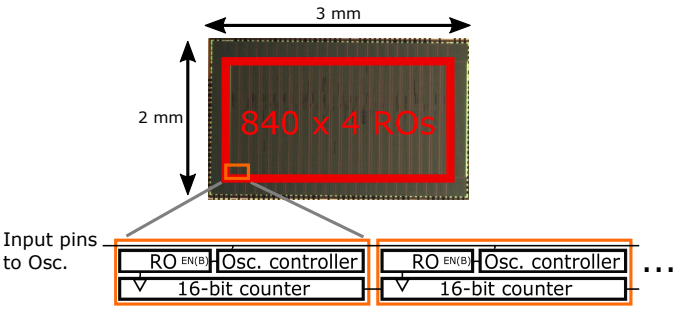

Fig. 9. Test chip micrograph. The number of oscillations is counted by embedded 16-bit counter.

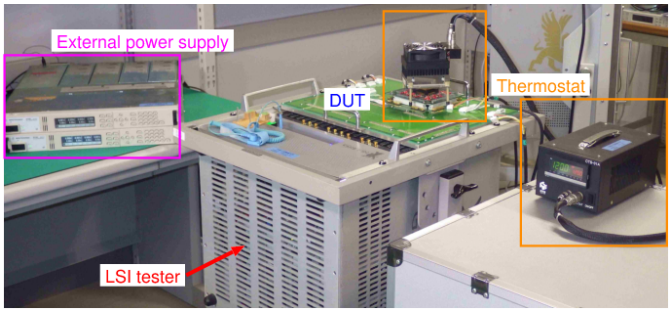

Fig. 10. Measurement system. Test chip (Device Under Test, DUT) is measured by LSI tester. Voltage is supplied by external power supply and temperature is fixed by Peltier module with temperature controller.

cover whole measurement system within higher temperature. In this system, the voltage and temperature are fluctuated by the feedback system of the measurement instruments. The subtraction method using BTI-sensitive ROs and -insensitive ROs is useful.

V. Measurement Results

Figure 11 shows a measurement flow to measure BTI-induced degradations. ROs oscillate for 12 μs in the order of gigahertz. Those stop oscillation for over 20 s for BTI stress after measuring frequencies. ROs suffer from BTI stress when it stop oscillation. Frequencies are measured every time after BTI stress. The oscillation and BTI stress are repeated. The measurements are performed at a temperature of 120 °C and a supply voltage of 2.0 V to accelerate BTI-induced degradation. Degradation rate (D_{rate}) is calculated as

$$D_{\mathrm{rate}} = \frac{f_0 - f(t)}{f_0} \ , \qquad (2)$$

where f_0 is the initial frequency at $t = 0$ and $f(t)$ is the measured frequency at time t.

TABLE I
Fabricated RO structures.

Structure	Figure	Number of ROs
PBTI-sensitive	Fig. 6 (a)	840 in all ROs
PBTI-insensitive	Fig. 6 (b)	
NBTI-sensitive	Fig. 7 (a)	
NBTI-insensitive	Fig. 7 (b)	

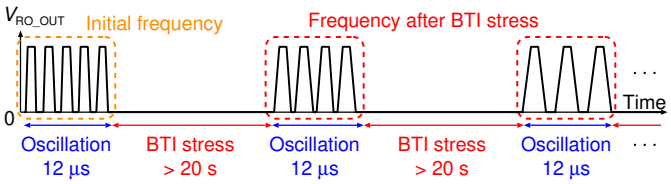

Fig. 11. Measurement flow of BTI-induced degradations.

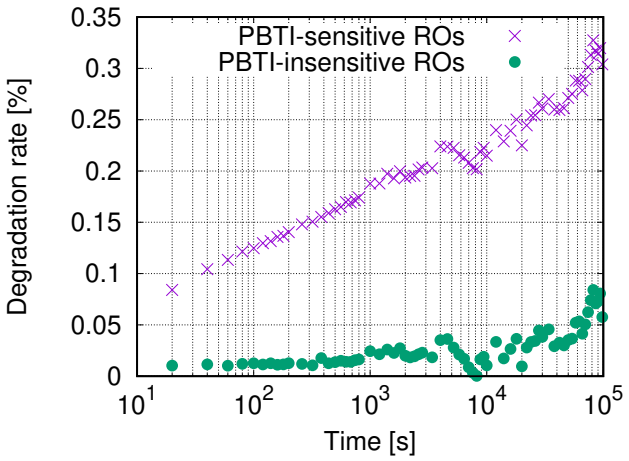

Fig. 12. Measurement results of PBTI-induced degradation.

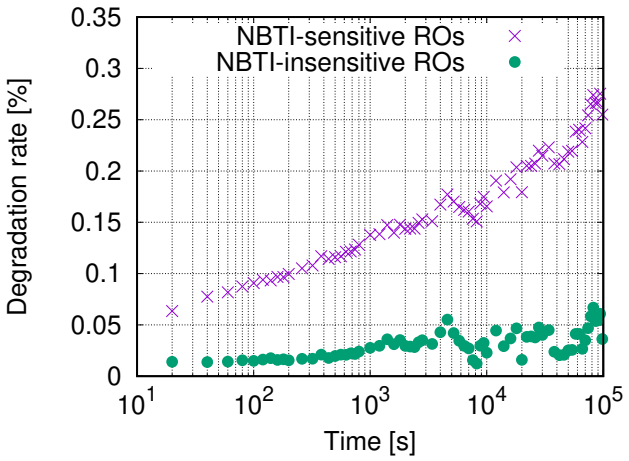

Fig. 13. Measurement results of NBTI-induced degradation.

A. Subtraction Results

Figure 12 shows the measured BTI-induced degradations in NAND ROs for PBTI-induced degradation. The X-axis and the Y-axis show the BTI stress time and D_{rate}, respectively. D_{rate} is averaged in 840 ROs. The D_{rate} values of PBTI-sensitive ROs [in Fig. 6 (a)] increase with time. However, The D_{rate} of PBTI-insensitive ROs [in Fig. 6 (b)] is almost constant. The degradation of BTI-sensitive ROs is 5x larger than that of BTI-insensitive ROs at 10^5 s. Figure 13 shows the measurement results in NOR ROs for NBTI stress. NBTI is also suppressed by arranging input connections like NAND ROs.

These results are dynamically fluctuated mainly due to temperature or voltage fluctuations. For example, D_{rate} suddenly increased at 5 ks and decreased at 10 ks. Both results

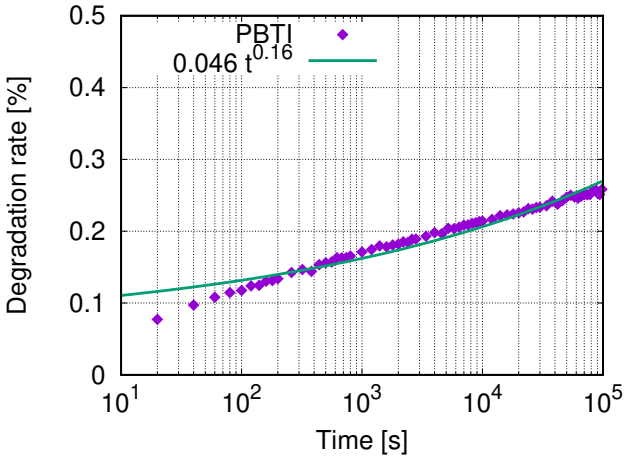

Fig. 14. Difference between PBTI-sensitive and -insensitive ROs.

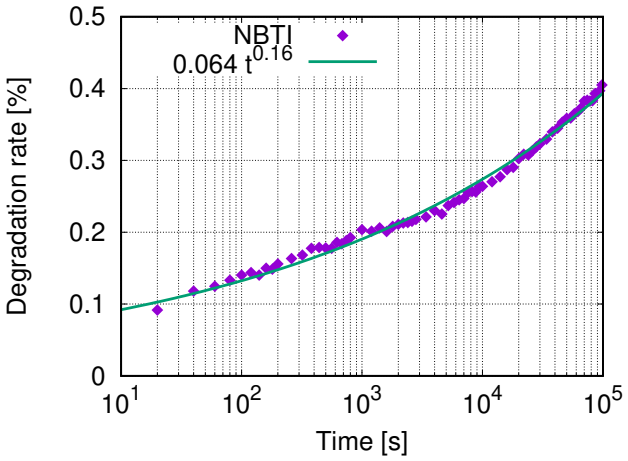

Fig. 15. Difference between NBTI-sensitive and -insensitive ROs.

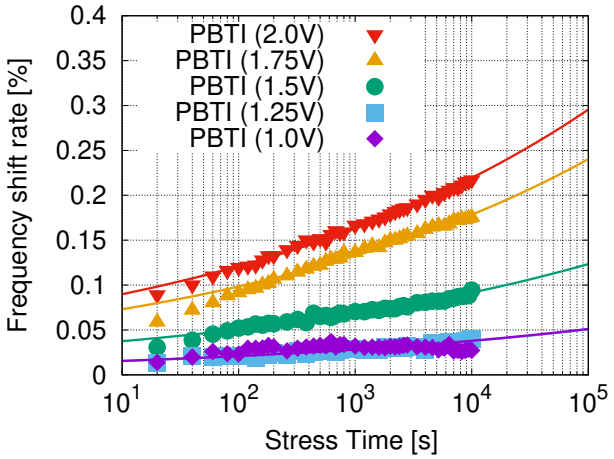

Fig. 16. Measurement results of voltage dependence in PBTI-induced degradation.

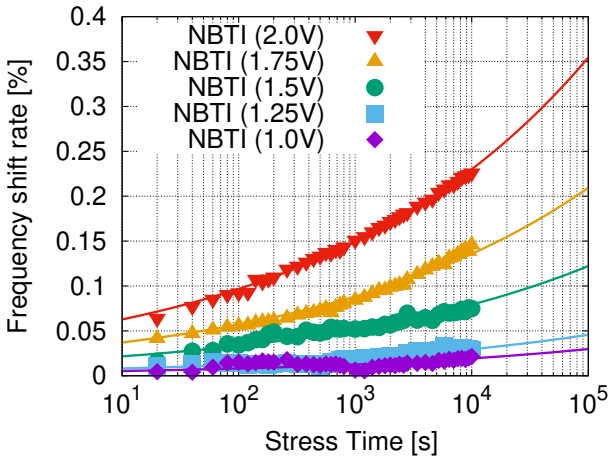

Fig. 17. Measurement results of voltage dependence in NBTI-induced degradation.

from BTI-sensitive and -insensitive ROs are correlated. Those fluctuation can be removed by subtracting BTI-insensitive results from BTI-sensitive ones. Figures 14 and 15 show the difference in NAND and NOR ROs, respectively. Fluctuations are removed and D_{rate} clearly increases with time. Subtracted data are fitted by Eq. (3) following Eq. (1).

$$\Delta V_{\mathrm{th}} = A * t^{n} * V_{\mathrm{param}} \ , \tag{3}$$

where t is the stress time, A and V_{param} are fitting parameters, and n is time exponent, which is 0.16 as in [17] because the same transistor size and process are used in NAND and NOR ROs. V_{param} represents acceleration factor of V_{gs}. Slope of the fitting fuction becomes more slightly as V_{param} is lower, which means the lower BTI-induced degradation. Measurement results are along with the fitting curve in both PBTI- and NBTI-induced degradations.

B. Voltage Dependence

Figure 16 shows the voltage dependence of BTI-induced degradations in NAND ROs for PBTI-induced degradation. PBTI-induced degradations without ambient fluctuations are extracted by subtraction in any voltage. Figure 17 shows the voltage dependence in NOR ROs for NBTI stress. NBTI-induced degradations are also extracted like PBTI.

V_{param} in Eq. (3) is the voltage dependence parameter. Table II shows fitted parameters V_{param}. A and n are fixed to those parameters at 2.0 V. Parameters V_{param} decreases as supply voltage decreases as shown in Table II. BTI-induced degradations without ambient fluctuations are extracted in any voltage.

TABLE II
FITTED PARAMETERS OF V_{param}.

Voltage [V]	NBTI	PBTI
2.0	1	1
1.75	0.59	0.81
1.5	0.34	0.42
1.25	0.13	0.17
1.0	0.084	0.17

VI. CONCLUSIONS

BTI-sensitive and BTI-insensitive ROs are used to extract BTI-induced degradations without fluctuations of ambient

environments. The test chip was fabricated in the 65 nm process and BTI-induced degradations were measured. The degradation of PBTI/NBTI-sensitive ROs is five times larger than PBTI/NBTI-insensitive ROs at 10 ks. Fluctuation originated from ambient environments are successfully removed by subtracting results of BTI-insensitive ROs from those of BTI-sensitive ones. This subtraction is useful in any voltage.

ACKNOWLEDGMENTS

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