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NBTI-Induced Delay Degradation Analysis of FPGA Routing Structures

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Abstract: Reliability issues, such as soft errors, process variations and Negative Bias Temperature Instability (NBTI), become dominant on Field Programmable Gate Arrays (FPGAs) fabricated in a nanometer process. We focus on aging degradation by NBTI, which causes threshold voltage shifts on PMOS transistors. We characterize delay degradation in the routing structures on FPGAs. The rising and falling delays vary due to NBTI and heavily depend on circuit configurations. In the independent routing switch, the delay fluctuation due to NBTI can be minimized by transistor sizing. The falling delay does not change after 10-years degradation. In the routing structures composed of the routing switches and wires, the delay fluctuation depends on the wire length and can be minimized to optimize the wire length. We also show that the signal flipping can reduce the delay degradation from 11.3% to 2.76% on the routing resources.

Keywords: NBTI, FPGA, reliability, aging degradation, threshold voltage

1. Introduction

Performance of Field Programmable Gate Arrays (FPGAs) is improved by advancement in scaling technology. In recent years, it is becoming comparable to that of Application Specific Integrated Circuits (ASICs) because FPGAs can be fabricated with the latest process. Reliability issues, such as soft errors, process variations and Negative Bias Temperature Instability (NBTI) are exposed at scaling process.

NBTI, an aging degradation on LSIs, was first reported in 1967 [1]. NBTI is known as one of dominant factors that determine life time of circuits after 65-nm process [2]. The threshold voltage (V_{th}) of PMOS increases with time caused by a stress voltage on the gate oxide, temperature and the duty cycle of the stress voltage. Interface traps are generated due to disintegration of Silicon-Hydrogen (Si-H) bonds under the stress conditions which result in NBTI.

FPGAs consist of logic parts and connection parts. Logic parts are able to be configured to any logic. Connection parts establish connection between the logic blocks by using reconfigurable switch matrices. Connection parts have a unique circuit structure which includes an NMOS switch transistor and a weak-keeper PMOS transistor called a level restorer or a half latch. Level restorers restore the voltage level lowered by the NMOS switch. Half latches are used to fix inputs of logic blocks to a constant value and are used for multiplexers which select the path on routing structures of FPGAs to prevent the input node of logic blocks from floating. The NBTI degradation of the delay time on the routing structures is a dominant design concern on FPGAs because the delay time of the routing structures determines the performance. FPGAs have an ability to reconfigure to tackle such a degradation effect.

In this paper, we analyze characterization of NBTI-induced delay degradation in routing switches of FPGAs. The degradation effects are different between the rising and falling edges of the data signal. The rising delays and the falling delays are changed by the degradation and depend on the circuit conditions. Performance of FPGAs is degraded by the degradation effects [3]. We propose two design methodologies to compensate NBTI degradation by optimizing the condition of routing structures of FPGAs. Optimizations of the size of MOS transistors reduce the degradation. The proposed design scheme mitigates NBTI-induced delay degradation by counterbalancing the degradation which are on the rising and falling edge.

The remainder of this paper is organized as follows. Section 2 introduces related works on FPGA reliability. In Section 3, we introduce NBTI characterization and analyze delay degradation on FPGA routing switches. Section 4 shows the analysis of FPGA routing structures and describes how to compensate the degradation. Section 5 summarizes this paper.

2. Related Works

In this section, we introduce several related works about reliability issues on FPGAs. Performance degradation on circuit elements of FPGAs due to NBTI has been discussed in Ref. [4]. They propose Relaxing Bitstream Technique to gain back lost stability. Their proposed technique recovers an average of 53.2% of the lost Static Noise Margin (SNM) of SRAM cells and improves the failure in time rate by 2.48% for a commercial FPGA device. The impact of NBTI is mitigated by flipping the configuration bits. Reference [5] is a survey paper about reliability in FPGAs. It explains various faults in FPGAs and the detection/repair meth-

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ods. Reference [6] is the latest work about NBTI effects on FPGAs. It also considers Hot Carrier Injection (HCI) and evaluates the DC and AC effects by its own method. It has shown that the aging behavior in FPGAs fits the predictions. An efficient technique to mitigate NBTI-induced delay degradation on the routing resources has not studied well. We analyze NBTI-induced delay degradation on the circuits in FPGAs and propose a design methodology to compensate the degradation.

3. Analysis of NBTI-Induced Delay Degradation

In this section, we show characterization of NBTI-induced delay degradation on routing resources in FPGAs. This section includes an explanation of NBTI models, how to simulate NBTI degradation on FPGAs, the simulation results and a compensation methodology by transistor sizing.

3.1 NBTI Modeling

There are many models which show how PMOS $V_{\rm th}$ is changed by NBTI degradation. NBTI degradation has a permanent part and a recoverable part. The recoverable part recovers soon after the stress is removed but the permanent part remains forever. NBTI under continuous stress is called static NBTI. NBTI alternating between stress and relax is called dynamic NBTI. Both static and dynamic NBTI have permanent and recoverable parts. Recoverable part can recover in dynamic NBTI. The dynamic NBTI effect depends on the frequency and the duty cycle. Several measurement methods are proposed in Refs. [7], [8], [9]. It is difficult to measure NBTI degradation because the degradation recovers quickly. Some predictive NBTI models are suggested in Refs. [10], [11]. The accurate model is still discussed, because the NBTI-induced degradation critically depends on the stress condition and the process node. We apply $V_{\rm th}$ degradation ($\Delta V_{\rm th}$) as in, Eqs. (1), (2) proposed in Refs. [11], [12] to evaluate performance degradation of circuit structures in FPGAs.

$$\Delta V_{\rm th,Static} = A\left((1+\delta)t_{\rm ox} + \sqrt{Ct}\right)^{2n} \quad (1)$$

$$\Delta V_{\rm th,Dynamic} = \left(\sqrt{\frac{K_{\rm v}^2 \alpha T_{\rm cyc}}{1-\beta_{\rm t}^{1/2n}}}\right)^{2n} \quad (2)$$

Eqs. (1), (2) express $\Delta V_{\rm th}$ on static NBTI and dynamic NBTI, respectively. The parameters are determined as follows. Degradation factors, A and $K_{\rm v}$, have dependence on the electrical field and the temperature. Those parameters are caluculated from the degradation amounts. The parameter δ is a fitting parameter, $t_{\rm ox}$ is the oxide thickness. The Parameter C has temperature (T) dependence as $C = T_{\rm o}^{-1}\exp(-E_{\rm a}/kT)$. The parameter $E_{\rm a}$ is the activation energy of hydrogen species, k is the Boltzmann constant, and $T_{\rm o}$ is constant with the value of 10^{-8} s·nm^{-2}. The time exponent parameter n is 1/6 for H_2 diffusion, α is duty cycle ($\alpha = T_{\rm stress}/(T_{\rm stress}+T_{\rm recover})$), $T_{\rm cyc}$ is the time period of one stress-recovery cycle, and $\beta_{\rm t}$ is fraction parameter of the recovery. We assume that $V_{\rm th}$ will be degraded by 55% on continuous DC stress under the following condition. Supply voltage ($V_{\rm dd}$) is 1.2 V and T = 100°C. Device parameters are based on 65-nm process typical devices. These parameters do not include any degradation parameter. Degradation time is 10 years (= 3.1536×10^8 s). Under the condition, $V_{\rm th}$ will be degraded by 10% on stress-recovery cycle which is $\alpha = 0.5$ and $T_{\rm cyc} = 0.01$ s. The duty cycle α of 0.5 is a little bit pessimistic value on FPGAs, because the input signals flip every clock. But we can evaluate NBTI degradations under these strict conditions. These degradation amounts are decided according to the parameters in Ref. [11]. **Figure 1** shows $V_{\rm th}$ degradations of static and dynamic NBTI under the above condition. X axis is stress time plotted in logscale and Y axis is $\Delta V_{\rm th}$. Those parameters are also described in **Table 1**.

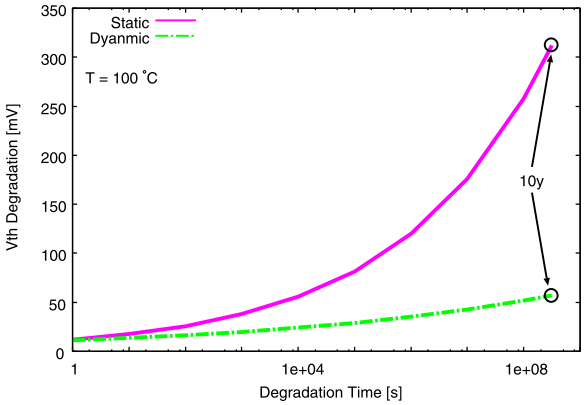

Fig. 1 $V_{\rm th}$ degradation under static/dynamic NBTI.

Table 1 Parameter descriptions. Note that $t_{\rm ox}$ is not available due to NDA.

P.	Description	Value
A	Degradation Factor (Static)	0.004
$K_{\rm v}$	Degradation Factor (Dynamic)	2×10^{-7}
δ	Fitting Parameter	0.1
$t_{\rm ox}$	Oxide Thickness	N/A
T	Temperature	100°C
k	Boltzmann Constant	1.38×10^{-23} J/K
$E_{\rm a}$	Activation Energy of Hydrogen Species	0.49 eV
$T_{\rm o}$	Constant	10^{-8} s/nm^2
n	Time Exponent Parameter	1/6
α	Duty Cycle	0.5
$V_{\rm dd}$	Supply Voltage	1.2 V
$T_{\rm clk}$	Time Period of Stress-Recovery Cycle	0.01 s

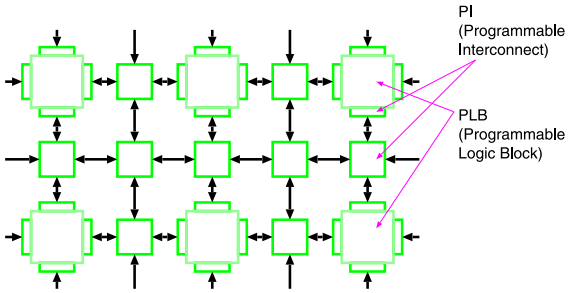

Fig. 2 FPGA architecture.

3.2 Setup for FPGA Aging Simulations

An FPGA device consists of programmable logic blocks (PLBs) and programmable interconnects (PIs). **Figure 2** shows a structure of an island-style FPGA. PLBs include several logic elements consisting of look up tables (LUTs), flip-flops and configuration memories. Users can configure it to any logic they want. PIs include a lot of switch matrices, wires and routing switches.

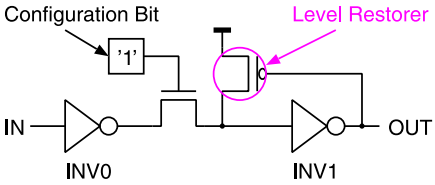

Fig. 3 Routing switch with level restorer.

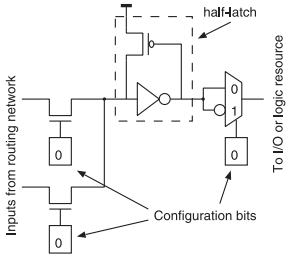

Fig. 4 Half latch circuit in FPGA.

We focus on the NBTI degradations of the routing switch shown in **Fig. 3**, which is commonly used in FPGAs [13], [14]. There are two inverters (INV0 and INV1), an NMOS transistor to be used for a switch, a pull-up PMOS transistor and a configuration bit determining ON/OFF of the switch. If the configuration bit stores 1, the switch is ON. If 0 is stored, the switch is OFF. The input node of INV1 floats if there is no pull-up PMOS transistor. The PMOS transistor is called a level restorer or a half latch to restore the voltage level lowered by the NMOS or to prevent INV1 from floating. **Figure 4** is an illustration of what half latches are at circuit level [15]. When one of the NMOS switches is on, the pull-up PMOS transistor will be driven by the incoming signals from the routing network. The half latch circuit can be used to produce a fixed output value of 0 or 1, as needed by the user's design. Note that the performance of the half latch is not degraded by NBTI because the output value is constant. NBTI degrades switching speed. Constant output signals are not degraded by NBTI. We focus on the PMOS transistor used as the level restorer rather than the half latch in this paper.

We calculate ΔV_{th} with Eqs. (1), (2) and apply it to the circuit netlists. The Parameter V_{th} is changed through a device parameter V_{TH0} in the MOS model of BSIM4 [16]. It is based on the typical condition parameter of the process variations. An input signal is given as follows in all simulations. A pulse with 1 ns rise and fall time is given to evaluate circuit performance degradations. It is applied to circuits via two inverters. The output nodes of all circuits are connected to fan-out 4 inverters. Those inverters are output loads and they are connected to simulate the circuit in a realistic way. We analyze NBTI-induced delay degradation on circuit structures commonly used in FPGAs.

3.3 Analysis of NBTI Degradation on FPGA Routing Switches

We evaluate and compare NBTI degradation on two structures, the routing switch with and without a level restorer by circuit simulations. We analyze delay degradation under the NBTI effect. **Figure 5** shows the routing switch without any level restorer. **Figure 6** shows the routing switch with the multiple inverters and cascaded level restorers. In order to compare the degradation of

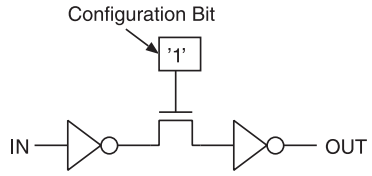

Fig. 5 Routing switch without level restorer.

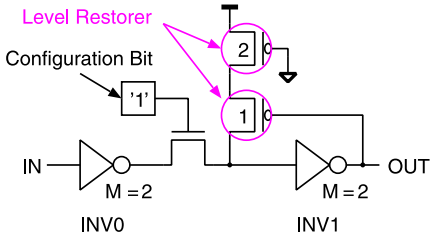

Fig. 6 Routing switch with cascaded level restorers.

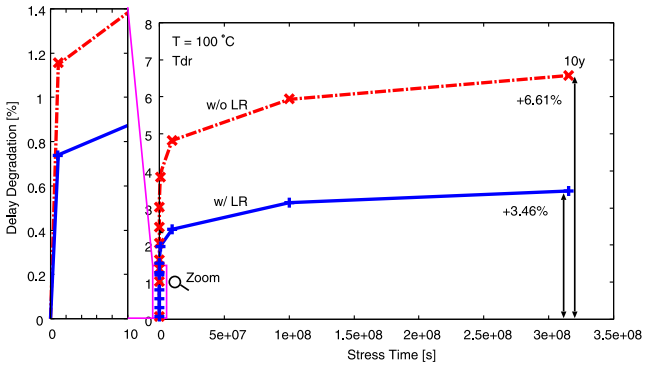

Fig. 7 T_{dr} degradation under accelerated NBTI condition at 100°C.

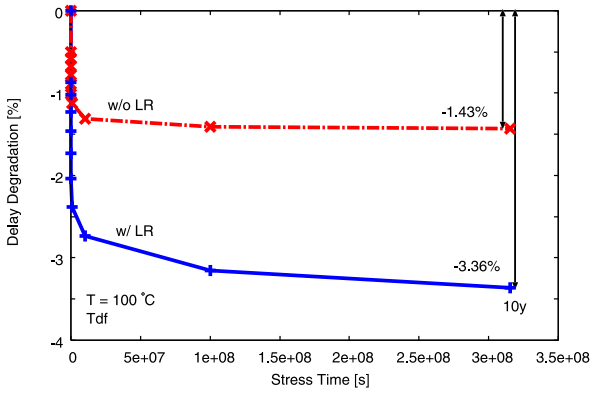

Fig. 8 T_{df} degradation under accelerated NBTI condition at 100°C.

the circuits of Fig. 6 and Fig. 5 under equal conditions, the rise and fall delays of these circuits are close in the initial state. It is achieved by duplicating inverters (M=2) and cascading level restorers. The delay difference at the initial state is within 0.8%. The size of the level restorer transistor should be smaller than the other transistors [17]. The level restorer can be weak to stack PMOS transistors without increasing load capacitance. The purpose of comparing those two circuits is to evaluate difference of FPGAs over general ASICs.

The results of delay degradation analysis are shown in **Fig. 7** and **Fig. 8**. The word LR in those figures is the abbreviation of level restorer. The left side of Fig. 7 shows degradations near $t = 0$. Note that the initial degradations are both 0% on without and with level restorer cases. Degradations at $t = 0$ are 0% in all

the graphs showing time dependent degradations hereafter. The rise time delay (T_{dr}) is increasing when the circuits are degraded by NBTI. Delay increase of the circuit without any level restorer is 1.9 times larger than that of the circuit with level restorers. The fall time delay (T_{df}) is decreasing when the circuits are degraded by NBTI as shown in Fig. 8. Delay decrease of the circuit with level restorers is 2.4 times larger than that of the circuit without any level restorer.

The PMOS transistor in INV1 in Fig. 6 is the most sensitive to NBTI degradation. It is obvious by the sensitivity analysis that examines degradation of individual INV0, INV1 and level restorer. The reason of the highest INV1 sensitivity is due to connection to the output load. If its V_{th} increases, it becomes slower for V_{gs} to exceed V_{th} than the initial condition. The effect results in T_{dr} increase. If its V_{th} decreases, it becomes fast for V_{gs} to exceed V_{th} and the effect results in T_{df} decrease. Those two effects are caused by sensitivity of INV1. The level restorer PMOS easily becomes OFF by the degradation. It becomes ON when OUT falls, and becomes OFF when OUT rises. The level restorer helps OUT to fall under the degradation condition, while it interferes with OUT from rising.

3.4 Analysis of the Effect of Output Loads on NBTI Degradation

We evaluate NBTI degradation on the routing switch (Fig. 6) which connected to fan-out 2, 4 or 8 inverters. The other simulation conditions are same as described in Section 3.3. The purpose is to analyze the effect of the output load on NBTI degradation. The results of delay degradation analysis are shown in **Fig. 9** and **Fig. 10**. Note that delays at the initial state are different as described below.

T_{dr}: FO8 > FO4 > FO2

T_{df}: FO8 > FO4 > FO2

They show the degradations of T_{dr} with fan-out 2, 4 and 8 inverters are 2.59%, 3.46% and 4.85% and those of T_{df} are −3.85%, −3.36% and −2.81% after 10 years. The rise time delay (T_{dr}) is increasing more when the circuit is connected to larger output load. The fall time delay (T_{df}) is decreasing more when the circuit is connected to smaller output load. Because the output load has such effects on NBTI degradation, the circuit connected larger output load is degraded worse than that connected smaller one.

3.5 Compensating Methodology by Sizing of the NMOS Switch

The degradations of T_{df} on routing switches with level restorers of FPGAs (Fig. 6) depend on circuit configurations. It decreases in the case of NMOS in the routing switch which is equal to the size of the standard (1x) inverter. If the size of the NMOS switch becomes larger, T_{df} is increased by the degradation. Delay degradation on INV0 is emphasize by enlarging the size of NMOS. We focus on this characteristic to compensate the delay degradation. If the size of the NMOS switch is optimized, T_{df} does not increase nor decrease. We evaluate the degradation with various widths of the NMOS switches. The other simulation conditions are same as described in Section 3.3. The result is shown in **Fig. 11**. Note

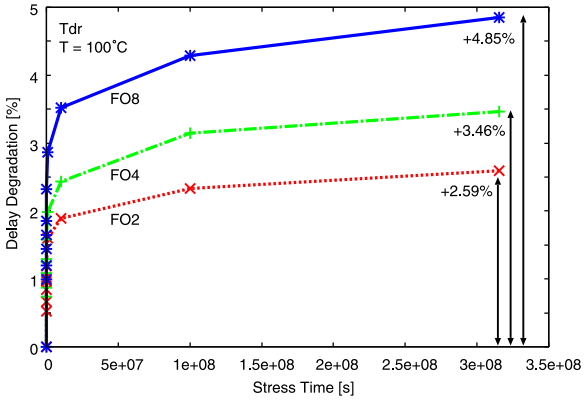

Fig. 9 T_{dr} degradation under accelerated NBTI condition at 100°C on the circuit with fan-out 2, 4 or 8 inverters.

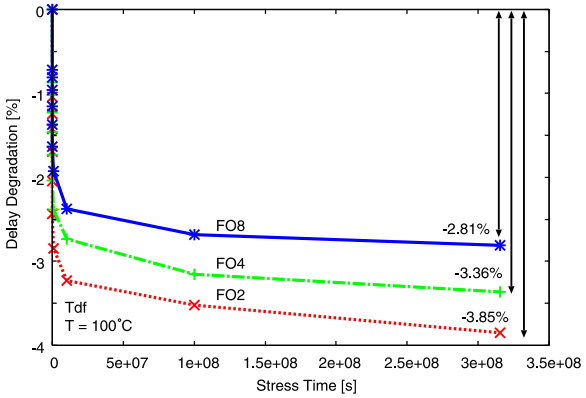

Fig. 10 T_{df} degradation under accelerated NBTI condition at 100°C on the circuit with fan-out 2, 4 or 8 inverters.

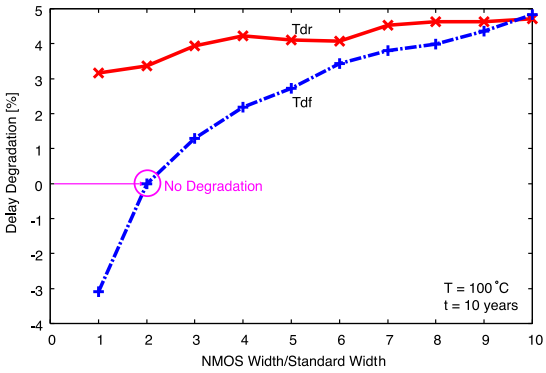

Fig. 11 Degradation under accelerated NBTI condition at 100°C by different NMOS width.

that the X axis denotes the ratio between the NMOS width and the standard NMOS width. It shows T_{df} degradation is 0.00% at 2x size. **Figure 12** shows the degradation with the 2x NMOS width. The degradation of T_{dr} is almost same as that of the circuit with the standard size NMOS switch. The delay degradation of T_{df} after 10 years is 0.00%, while it is −0.284% at $t = 1 \times 10^4$ s, which is much better than that of −3.36% after 10 years.

The rise time delays of INV0 and INV1 are increased by the degradation while the fall time delays are decreased. In the case of the circuit with the standard size NMOS switch, NBTI effect on INV1 is dominant and T_{df} decreases by the degradation. The effect on INV0 is emphasized by the large size NMOS switch. The delay increase on INV0 and the delay decrease on INV1 are balanced at the circuit with the 2x NMOS switch.

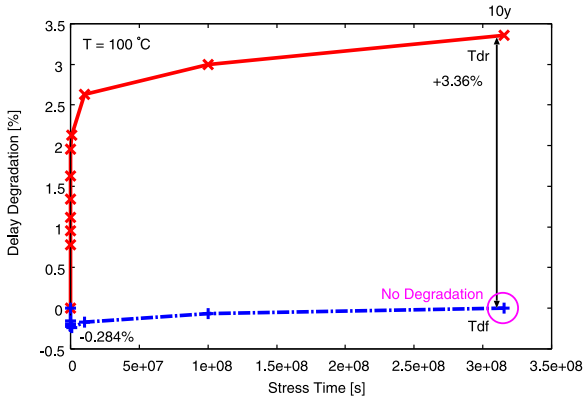

Fig. 12 Delay degradation under accelerated NBTI condition at 100°C with 2x NMOS width to compensate ΔT_{df}.

4. FPGA Routing Structures to Compensate NBTI Degradation

In this section, we show a delay analysis of FPGA routing structures and propose design methodologies to compensate NBTI degradation on FPGA routing structures.

4.1 Analysis of NBTI Degradation on FPGA Routing Structures

We analyze NBTI degradation on a circuit structure in FPGA routing structures, as in **Fig. 13**. It is a multiplexer circuit to connect the logic blocks, I/O or routing networks in FPGAs [18]. One path is selected by values stored by the configuration bit (Config Bit). If no path is selected, the level restorer keeps the output voltage low. We assume 12 metal layer process. The metal1-6, metal7-9, metal10-11 and metal12 layers are used for local metal layers, semi-global metal layers, global metal layers and a top metal layer, respectively. The Wires connect PIs through the metal7 layer and are assumed to be 1 mm long with a π structure as shown in **Fig. 14**. The parameter RBL (Resistance Between Layers) is a resistance between the gate (or the source/drain) and the metal7 layer, IR (Interconnect Resistance) is a resistance of the wire in the semi-global metal layer and IC (Interconnect Capacitance) is the capacitance between the metal7 layer and substrate. These parameters are computed by using 65 nm process data and the wire structure. RBL is given as ohm per via (Ω/via) which shows the resistance between two specific layers. IR and IC are given as ohm per millimeter (Ω/mm) and femtofarad per millimeter (fF/mm). For example, we can compute IR by multiplication of data of IR and the interconnect length. Delay degradation on this circuit is shown in **Fig. 15**. The simulation condition is as same as the one described in Section 3.3. T_{dr} and T_{df} are increased by NBTI. When PMOS V_{th} is increased by NBTI degradation, it becomes slower for an inverter to switch from 0 to 1.

The design methodology proposed in Section 3.5 is not applied for the routing structure since the both rise and fall delays are degraded. But it is because of the 1 mm long wire. We show the delay fluctuation is changed by the wire length.

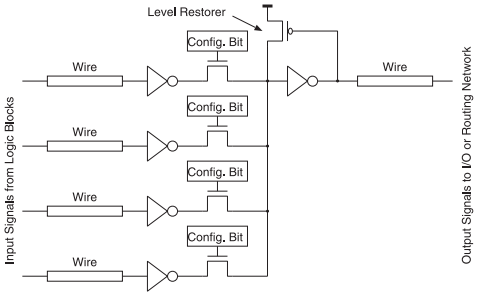

Fig. 13 FPGA routing structure.

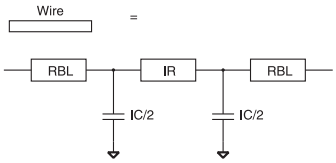

Fig. 14 π wire structure.

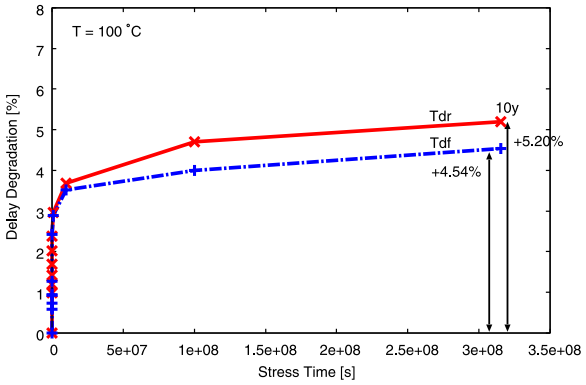

Fig. 15 Delay degradation under accelerated NBTI condition at 100°C on FPGA routing structure.

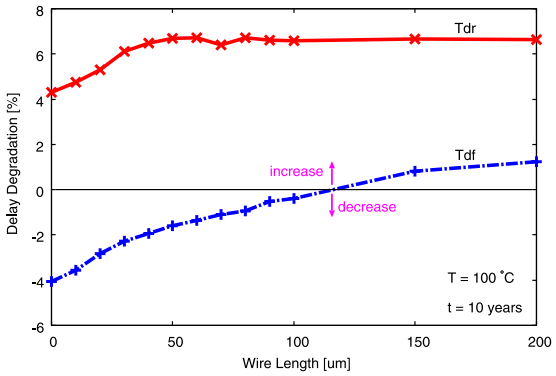

Fig. 16 Degradation under accelerated NBTI condition at 100°C on routing structure by different wire length.

4.2 Delay Compensation by Signal Flipping

The degradations on routing structures of FPGAs in Fig. 13 depend on circuit configurations. It is decreased if the wire length becomes short because the load capacitance is reduced. We evaluate the degradation with various wire lengths. The simulation conditions are same as described in Section 4.1 except for the wire length. The result is shown in **Fig. 16**. It shows the degradation of T_{df} is hidden at 120 μm. The fall time delay is increased on the circuit with wires over 120 μm while it is decreased on that with wires below 120 μm. The degradations of T_{dr} remain unchanged over 100 μm. It also shows the degradation tenden-

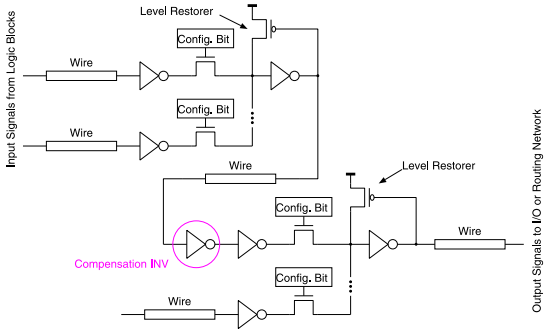

Fig. 17 FPGA routing structure to compensate delay degradation by flipping signals.

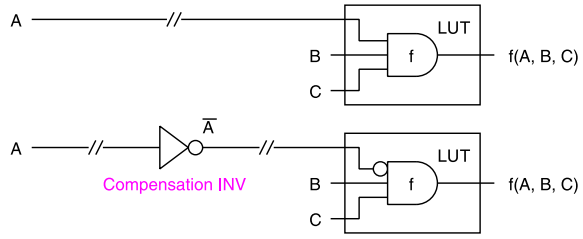

Fig. 18 Logic modification by programming LUT.

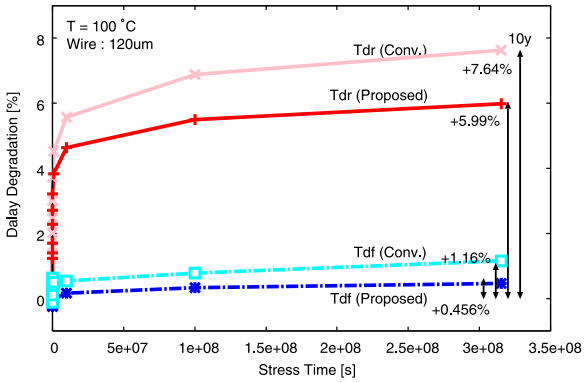

Fig. 19 Delay degradation under accelerated NBTI condition at 100°C on routing structure with and without Compensation INV.

cies can be changed easily by circuit configurations.

We propose the design methodology to mitigate the degradation by averaging them. Because the rise time delays are degraded more than the fall time delays, the total delay degradation can be shorter by inserting the compensation inverter. **Figure 17** shows the proposed structure which alternates the rising signal and the falling signal by an inverter (Compensation INV). It is supposed to be used for the switch matrices of FPGAs. The receiver-side network has to be modifid to invert the logic signal. It can be easily modified by re-programming the LUT as shown in **Fig. 18**. We evaluate its delay degradation. The simulation circuit consists of two routing structures with 120 μm long wires. A circuit with 120 μm long wires is an example to show the compensation result of the proposed technique. The degradation on the structure is shown in **Fig. 19**. The fall time delay varies only slightly after 10 years. The degradation of the rise time delay is reduced to 5.99% from 7.64% without the compensation inverter.

We evaluate and compare the degradation on five variation conditions TT, FF, SF, SS, and FS. T (Typical), F (Fast), and S (Slow) conditions are defined as mean (μ), $\mu - 3\sigma$ (standard deviation), and $\mu + 3\sigma$ on the $V_{\rm th}$ Gaussian destribution. Simulation conditions except the variation are as same as above. The results of 10 years degradation are shown in **Table 2**. Our methodology reduces the delay degradation of $T_{\rm dr}$ on the SS condition from 11.3% to 2.76%. The proposed methodology is effective for devices under the conditions except for the FF condition. However, delays of fresh devices under the FF condition are generally half of that under the SS condition and 2/3 of that under the TT condition. Devices under the FF condition degraded by the NBTI degradation can still operate faster than fresh devices under the other conditions. Therefore, it does not matter that those under the FF condition be applied the proposed compensation technique.

Table 2 Delay degradation under accelerated NBTI condition at 100°C after 10 years on five coditions of routing structure with and without Compensation INV. (T: Typical, F: Fast, S: Slow, For example, SF is NMOS slow and PMOS fast condition.)

Condition	Scheme	Degradation after 10y	
		$\Delta T_{\rm dr}$ [%]	$\Delta T_{\rm df}$ [%]
TT	Conv.	7.64	1.16
	Proposed	5.99	0.456
FF	Conv.	4.98	2.10
	Proposed	5.62	0.855
SF	Conv.	7.76	3.31
	Proposed	7.20	2.84
SS	Conv.	11.3	−2.79
	Proposed	2.76	−3.52
FS	Conv.	7.23	−2.07
	Proposed	−0.888	−2.17

5. Conclusion

In this paper, we analyze NBTI-induced delay degradation on FPGA routing paths and introduce two design methodologies to compensate the degradation. In the case of an independent routing switch, the rise delay time increases by 3.46% and the fall delay time decreases by 3.36% on the 10 years degradation at 100°C. Threshold voltage degradation on the pull-up PMOS (level restorer/half latch) is the main cause of the NBTI-induced delay degradation. The degradation of the fall delay time can be reduced to 0.284% by adequately sizing the NMOS to be used as a switch. The degradation of the rise delay time and the fall delay time on the conventional FPGA routing structure composed of several routing switches and wires are 7.64% and 1.16%, respectively after 10 years at 100°C. We introduce the signal flipping compensate the delay degradation. The rise time delay and fall time delay of the FPGA routing structure is degraded by 5.99% and 0.456% under the TT condition, respectively. The fall time delay degradation on the SS condition is reduced to 2.76% from 11.3% by our methodology.

Our future work is to evaluate the NBTI-induced delay degradation on real FPGA devices.

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