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Effect of Regularity-Enhanced Layout on Variability and Circuit Performance of Standard Cells

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As the minimum feature size shrinks down far below sub-wavelength, Design for Manufacturability or layout regularity plays an important role for maintaining pattern fidelity in photolithography. However, it also incurs overheads in circuit performances due to parasitic capacitance. In this paper, we examine the effect of layout regularity on printability and circuit performance by lithography simulation and transistor-level simulation. It is shown that regularity-enhanced cells provide better Critical Dimension (CD) stability under defocus and lead to delay increase. Then we evaluate the effect of layout regularity by a real chip measurement in 90 nm, 65 nm and 45 nm processes. For example, in a 65 nm process, inverter Ring Oscillators (ROs) that have the smallest poly pitch with dummy-poly insertion exhibits 19% reduction of WID and D2D variation with delay overhead of 2.5%, compared to the ROs without dummy-poly insertion. However, we have observed that the effect of layout regularity varies depending on fabrication processes and circuit structures. It is therefore important to obtain the best trade-off among performance overhead and variability reduction for each process technology.

1. Introduction

Technology scaling of LSI has been a basic principle for speed improvement, power reduction and die-size shrink. However in sub-100 nm era, a number of difficulties arise in performance variability and manufacturability. In the past, there was a clear separation between manufacturing side and design side with a set of design rules as an interface. The manufacturing side has been making an effort to suppress variability and improve yield. However in sub-100 nm era, the design side also has to take manufacturability into consideration. The effort from the designer side, called Design For Manufacturability (DFM), is becoming more important [1)–3)]. One of the techniques to enhance manufacturability by improving printability in a photolithographic process is to employ regularity into physical layout [4),5)]. Regularity-enhanced design is friendly to photolithography. However, design restriction associated with regularity reduces design flexibility and requires extra features such as dummy patterns. From a viewpoint of the circuit performance, regularity-enhanced design has negative impact since extra features require extra area and dummy patterns increase parasitic capacitance. Therefore designers should consider the trade-off between the advantage in printability and the disadvantage in circuit performance.

In this paper, we first examine the effect of layout density and regularity on printability by lithography simulation assuming a 65 nm process. We evaluate gate-poly Critical Dimension (CD) as a function of defocus. It is found that a narrower poly pitch provides better CD stability under defocus condition where the amount of CD deviation becomes small. We then evaluate gate-poly CD under different level of layout regularity where pitch uniformity is disturbed by a pitch break and removal of dummy poly patterns. It is observed that a wider poly pitch increases CD deviation under defocus, and hence it is preferable to insert dummy poly patterns from a standpoint of printability when the separation of poly patterns becomes large. On the other hand, from a standpoint of circuit performance, dummy poly patterns will increase parasitic capacitance which leads to delay increase. We evaluate this performance overhead by transistor-level simulation using NAND2 Ring Oscillators (ROs) as an example. It is found that a RO with dummy poly patterns exhibits 4% delay increase from a RO without dummy poly patterns. The amount of delay overhead for actual circuits, however, should be low due to the existence of fan-out load which is much larger than the parasitic capacitance introduced by dummy poly patterns.

The effect of poly-pattern density and regularity is then examined by test chip measurements. We have designed test structures with arrays of ROs for variability characterization in 90 nm, 65 nm and 45 nm processes. We have observed smaller Within-Die (WID) and Die-to-Die (D2D) variability in circuits with dense and regular poly-patterns, although the amount of improvement varies depending

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on fabrication processes and circuit structures. The amount of delay overhead is around expected values for 90 nm and 65 nm processes, whereas the 45 nm process exhibit larger performance spread which suggests the existence of other sources of CD systematic variation for less regular layout.

The remainder of this paper is organized as follows. In Section 2 and 3, we will discuss the effect of poly-pattern density and regularity on variability and delay using photolithographic and transistor-level simulations. Section 4 explains test structures for variability characterization in 90 nm, 65 nm and 45 nm process and shows measured effect of poly-pattern density and regularity. Finally, Section 5 summarizes this paper.

2. Effect of Layout Regularity on Printability

It is difficult in principle to print a feature smaller than the photolithographic wavelength. Edge placement errors because of interference and diffraction, etc, that is called Optical Proximity Effect (OPE), are becoming more serious. We focus on printability of transistor gate-poly in a photolithography process. Gate length variation largely depends on photolithography process [6], and therefore we can roughly estimate circuit performance variation by gate pattern fidelity.

In this section, we examine the effect of layout density and regularity on printability by lithography simulation [7] assuming a 65 nm process that uses a 193 nm optical source and attenuating Phase Shift Mask (PSM). Optical model parameters are provided from a foundry. For confidentiality reasons, further details cannot be disclosed. We have applied a model-based Optical Proximity Correction (OPC) to assist printability. Please note that a simulated poly pattern in this paper corresponds to a printed photo-resist pattern. Actual polysilicon pattern is formed through etch process based on the printed photo-resist pattern. The post-etch gate length therefore is not identical with the printed gate length since etch-bias exists in the etch process. Nonetheless, we will use the printability of gate-poly patterns for the measure of manufacturability since photolithography is the primary process for shaping gate-poly patterns. Also, the result of photolithography simulation depends on the optical model used in the simulation [8]. The optical model, which includes many parameters such as wavelength, numerical aperture and light source configuration, is specific not only to the technology

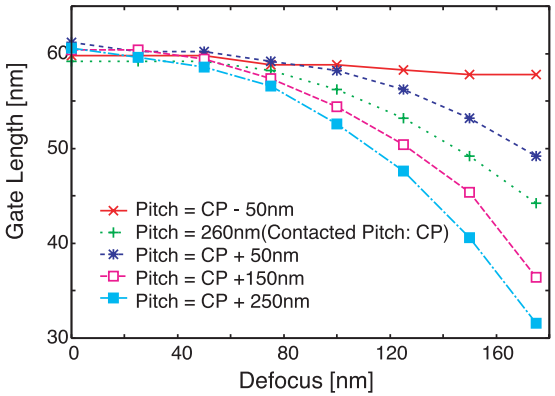

Fig. 1 Effect of various gate pitches to gate length.

nodes but also to the equipments used for photolithograpy process. We have therefore obtained the optical model for a 65 nm process from a foundry.

2.1 Layout Density

It has been said that layout density has a close relation to pattern CD uniformity, called loading effect [9),10]. Loading effect is caused by OPE in photolithography process and non-uniformity of plasma gas density in etch process, etc. It is expected that a distance between adjacent features has a primary effect on CD variation.

We therefore examine the effect of pattern density using a test layout that is a 2-dimensional array of gate-poly patterns spaced in the same pitch. We evaluate printed gate length of the test pattern as a function of defocus. **Figure 1** shows the results for the test layout with different amount of pitches. In all cases, printed gate length decreases as the amount of defocus increases. It is also seen that the amount of pitch, which corresponds to layout density, has a strong effect on CD variability. The narrowest pitch of 210 nm provides the best CD stability under defocus. Wider pitches such as 410 nm and 510 nm result in larger CD variability than that of contacted pitch (260 nm). From this result, it is expected that narrow pitch, that is dense layout, provides a better CD stability under defocus.

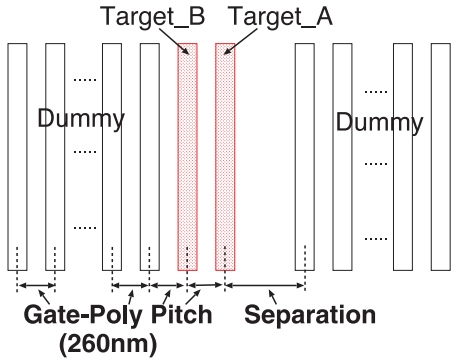

Fig. 2 Test pattern to evaluate the effect of gate poly pitch.

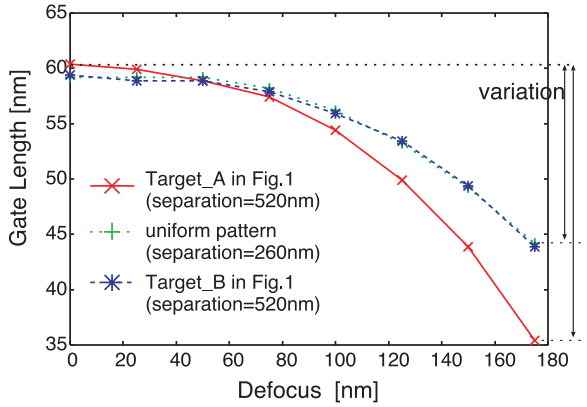

Fig. 3 Simulation results of the effect of pitch irregularity.

2.2 Layout Regularity

Layout regularity is favorable in many manufacturing stages, especially in a photolithography process. In this subsection, we evaluate the effect of layout regularity on printed gate-poly CD using a test layout and actual cell layout.

2.2.1 Pitch Uniformity

We examine the effect of a pitch break with a test structure shown in **Fig. 2**. There are two groups of arrayed polysilicon patterns with the contacted pitch of 260 nm.

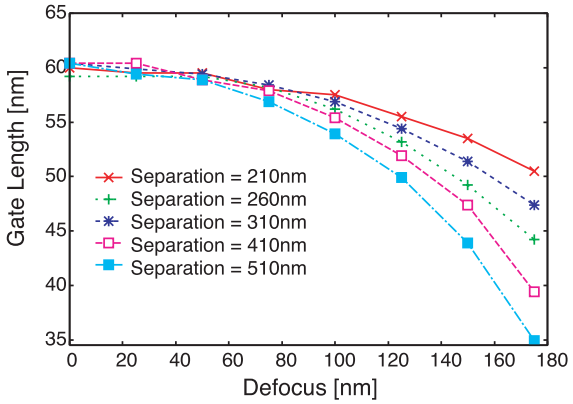

Fig. 4 Simulated gate linewidth of the pattern that faces the separation under different separation length.

First, setting the separation of two groups to the contacted pitch, we evaluate the gate length of the single pitch pattern as a function of defocus by lithography simulations. We then set the separation to 520 nm, which is equivalent to removal of only one feature, and evaluate the effect of a pitch break. The gate length of Target_A and Target_B are shown in **Fig. 3**. As the amount of defocus increases, the gate length gradually decreases. Thanks to the OPC, the gate length of the uniform pattern and that of Target_B are almost identical. However, the gate length of Target_A at the edge of the group exhibits larger fluctuation which indicates degradation in defocus tolerance.

Next, we evaluate the effect of separation length on the gate length of Target_A. **Figure 4** shows the gate length of Target_A as a function of defocus with several values of the separation. It is observed that the larger separation increases CD deviation under defocus, which is similar to the results of the examination in Sec. 2.1. Hence it is preferable to insert dummy gate-poly patterns from a standpoint of printability when the distance between poly patterns becomes large.

2.2.2 Layout Regularity

The width of printed polysilicon patterns, especially at jogs and line ends, is susceptible to variation. If these patterns exist on or near diffusion area, the variability of the poly-pattern directly leads to gate length variation. It is

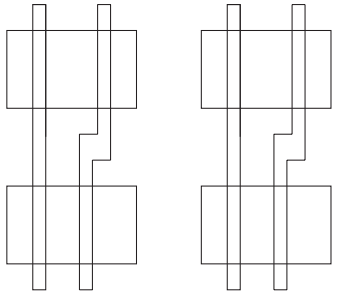

Fig. 5 Layout of NAND2-jog.

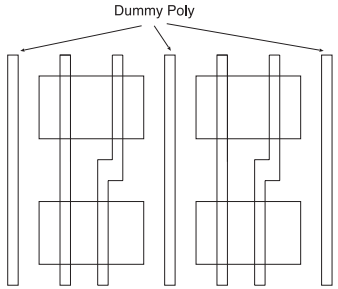

Fig. 6 Layout of NAND2-jog with dummy.

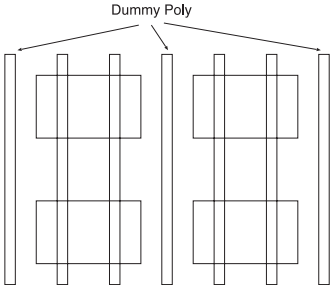

Fig. 7 Layout of NAND2-straight with dummy.

therefore effective to remove jogs and spots where pattern width changes and to keep these spots as far away from diffusion.

From the discussion so far, it is expected that pitch restriction and jog removal are effective to improve robustness to defocus. We estimate regularity-enhancement results in three standard-cell layouts with different levels of regularity by lithography simulation.

2.2.2.1 NAND2 with Different Layout Regularity

We introduce three layouts of a two-input NAND gate. To evaluate the effect of regularity, each layout is configured as follows with the same layout area and routability.

- **NAND2-jog (Fig. 5)** In this cell, no design restriction for regularity is employed. Gate pitch is irregular and jogs are allowed with minimized diffusion area.
- **NAND2-jog with dummy (Fig. 6)** In this cell, dummy polysilicons are inserted so that poly gates of PMOS transistors have a single pitch. Dummy polysilicons are expected to improve printability, although they increase parasitic capacitance.
- **NAND2-straight with dummy (Fig. 7)** In this cell, all the pitches of polysilicon patterns are designed to be identical. Dummy polysilicons are used and the jog of the polysilicon is prohibited.

2.2.2.2 Simulation Setup

It is not favorable to do lithography simulation only one cell separately, because exposed cells could be affected by the neighboring pattern. In the lithography simulation, we make an array of cells in a 3×3 matrix, and evaluate the center cell after exposure. We use the average gate length of each P/N transistors of NAND2 as evaluation measures. Generally, an edge of a printed pattern fluctuates according to its own and surrounding layouts, and therefore gate length varies inside a transistor. We estimate the average gate length as a function of defocus.

2.2.2.3 Results of Lithography Simulation

Figures 8 and **9** show the average gate length of NMOS and PMOS transistors, respectively. P/NMOS average gate length of each layout decreases in accordance with the defocus as indicated in the simulation. Then, regularity-enhanced cells have better gate length stability. For example, at the defocus of 100 nm, PMOS average gate length of NAND2-jog is about 4.0% smaller than that of NAND2-straight with dummy and NAND2-jog with dummy. NAND2-straight with dummy and NAND2-jog with dummy seem almost the same robustness to defocus, this means that dummy pattern insertion has strong effect on pattern fidelity. NMOS gate length deviation of NAND2-jog with dummy and that of NAND2-straight with dummy exhibit similar defocus characteristics when defocus is less than 50 nm. However, the former becomes smaller than the latter when defocus is more than 50 nm, which seems to be caused by closer distance between NMOS polysilicon patterns of NAND2-jog with dummy as suggested by the result of pitch uniformity simulation shown in Fig. 4.

From the discussion above, under the optical model used for the lithography simulation, the separation of polysilicon patterns has a great influence on pattern

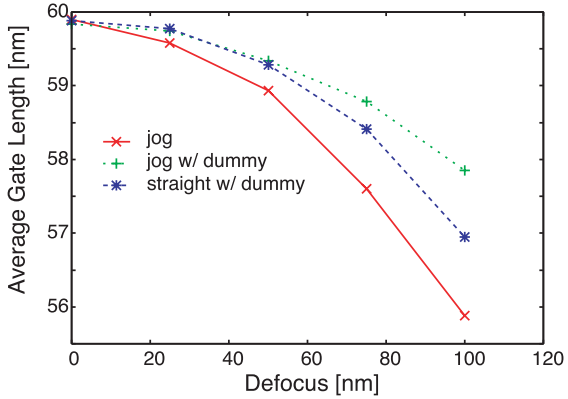

Fig. 8 Average gate length of NMOS of two-input NAND.

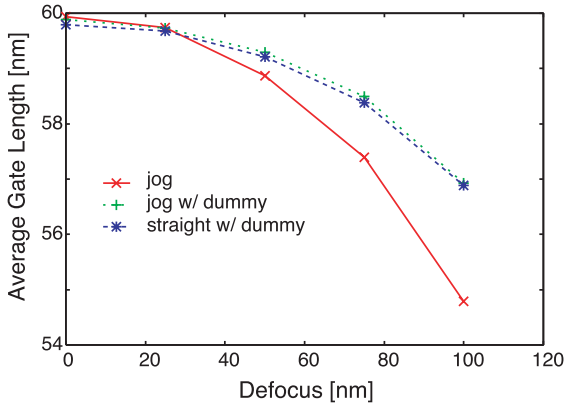

Fig. 9 Average gate length of PMOS of two-input NAND.

fidelity. A wider separation appeared in adjacent NAND2-jog leads to susceptibility to defocus. Dummy pattern insertion for eliminating wider separation improves printability and robustness to defocus.

3. Effect of Layout Regularity on Circuit Performance

Regularity-enhanced cells may have undesirable aspects of area overhead, circuit performance, interconnects flexibility, and so on. In this section, we evaluate circuit delay of regularity-enhanced cells assuming a 65 nm process. Delay of regularity-enhanced cells may increase due to the parasitic capacitance. We evaluate this performance overhead by transistor-level simulation using ROs composed of NAND2 cells shown in the previous section. From simulated oscillation frequencies, we can evaluate the effect of regularity on the performance.

3.1 Simulation Setup

We obtain the circuit delay from a 19-stage RO simulation. We extract a netlist with parasitics from the RO array layout. Moreover, a load capacitance is added to each stage in the RO (**Fig. 10**) that represents an output loading appears in an actual circuit. We simulate the delay of each circuit as a function of load capacitance. The delay is normalized to that of NAND2-jog which is the fastest circuit with the least parasitics.

3.2 Results of Circuit Simulation

Figure 11 shows the simulated delay as a function of load capacitance. The performance of NAND2-jog with dummy RO degrades 2% in maximum and that of NAND2-straight with dummy RO degrades 4% in maximum when no load capacitance is added. In other words, inserting dummy increases delay by 2% and diffusion area expansion increases delay by 2%. In a real circuit other than ROs, each gate would drive more than a single gate. In this process, for example, fan-out of four corresponds to about 5 fF. In that case, performance overhead of NAND2-jog with dummy and NAND2-straight with dummy decreases to 0.5% and 1.5%, respectively.

From the discussion above, the regularity is effective to improve printability, and also at the same time it incurs performance overhead. Therefore it is important to find the best trade-off between printability and performance overhead, which should vary depending on the fabrication process. Next, we evaluate regularity-enhanced cells by real chip measurement.

4. Measurement of Regularity-enhanced Cells

In this section, we examine the effect of poly-pattern density and regularity by test chip measurements in 90 nm, 65 nm and 45 nm processes. First, we explain a test structure for variability characterization. Then we show how layout regularity affects Within-Die (WID) and Die-to-Die (D2D) variability in these

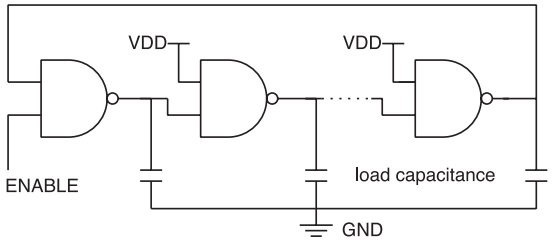

Fig. 10 Concept of ring oscillator circuit considering load capacitance.

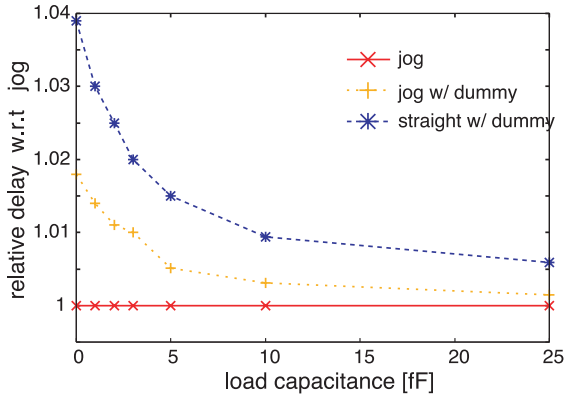

Fig. 11 RO simulation considering parasitic capacitance.

processes.

4.1 Test Structures for Variability Characterization

We have designed a test chip for gate delay variability characterization which contains array of tiles. Each tile consists of varieties of RO units, a decoder and a selector (**Fig. 12**). These ROs have different circuit structures or layouts of logic gates. The controller selects one tile and enables one RO in the tile. Its frequency is measured using an on-chip counter [11]. Number of tiles and chips for each process is shown in **Table 1**. From test chip measurement, we calculate the mean of oscillation frequencies and WID and D2D variability. We use standard deviation divided by the mean (σ/μ) as a measure of variation. Test chips of 90 nm and 65 nm processes are taken from a single wafer, with information on chip location only for 90 nm. For 45 nm process, we have two set of test chips from different lots.

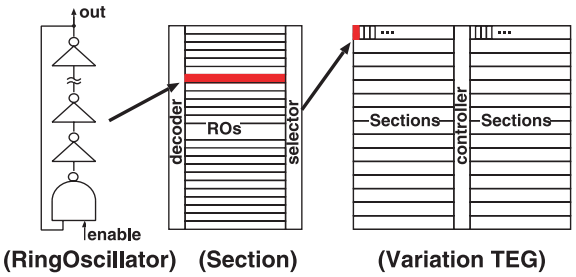

Fig. 12 90 nm TEG structure.

Table 1 Number of test chips and tiles.

technology node	90 nm	65 nm	45 nm
chips	37	20	64
tiles	450	384	12

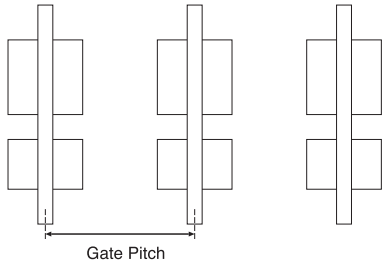

Fig. 13 Layout of Inverter ROs without dummy (wider pitch ROs).

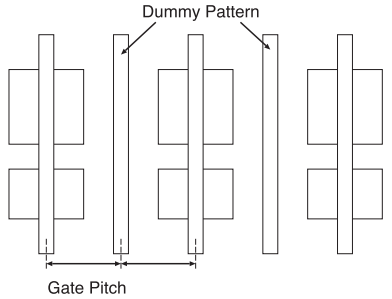

Fig. 14 Layout of Inverter ROs with dummy (narrower pitch ROs).

4.2 Layout Density

In this subsection, we evaluate the effect of poly pitch. We have designed two layouts of inverter ROs: one without dummy poly-patterns between adjacent gates (**Fig. 13**) and the other with dummy patterns in between (**Fig. 14**). The poly pitch of the former layout is exactly twice of the latter layout.

Table 2 summarizes the results of test chip measurement. The value of mean oscillation frequency μ is normalized by the mean oscillation frequency of the

wider pitch RO.

In the 90 nm process, the mean frequency (μ) of narrower pitch ROs (pitch = 390 nm) is 2.8% smaller than that of wider pitch ROs (pitch = 780 nm). There is no clear difference between WID-σ/μ of narrower pitch ROs and that of wider pitch ROs, however, D2D-σ/μ of narrower pitch ROs is smaller than that of wider pitch ROs.

In this process, we have created a wafer-level map of the mean oscillation frequency for each chip (WID-μ) according to chip location (Fig. 15). Each WID-μ value is normalized by the slowest WID-μ so that we can compare the D2D variation between wider and narrower pitch ROs. **Figure 15** shows that each wafer-map has a bowl-like shape where the chip at the center is the slowest and a chip becomes faster toward the edge of the wafer. The height of each bowl corresponds to the range of D2D variation. It is seen that the bowl height of the narrower pitch RO is smaller than that of the wider pitch RO.

In the 65 nm process, the mean frequency (μ) of narrower pitch ROs (pitch = 315 nm) is 2.5% smaller than that of wider pitch ROs (pitch = 630 nm), which is almost identical to the simulated overhead of 2.3% estimated by circuit simulation based on the extracted netlist from actual layout. WID-σ/μ and D2D-σ/μ of narrower pitch ROs are both 19% smaller than those of wider pitch ROs,which indicates that the regularity-enhanced cell can be a design option in this 65 nm process.

In the 45 nm process, we can similarly see that μ and D2D-σ/μ of narrower pitch RO is smaller than those of wider pitch RO. Compared to the other process, this process exhibits larger performance spread between ROs with wider and narrower pitches. For example, the mean frequency (μ) of narrower pitch RO is 11% smaller than that of wider pitch RO in maximum. This performance difference is more than the simulated overhead of 5% originated from the increase in parasitics, which suggests the existence of other source of systematic CD variation for wider pitch layout. For example, it is said that pattern density influences on CD slimming [12]. At this time, exact reason is not identified but the performance variability of ROs with narrower pitch is smaller than that with wider pitch.

4.3 Layout Regularity

In this subsection, we measure ring oscillator frequency consisted of two-inputs

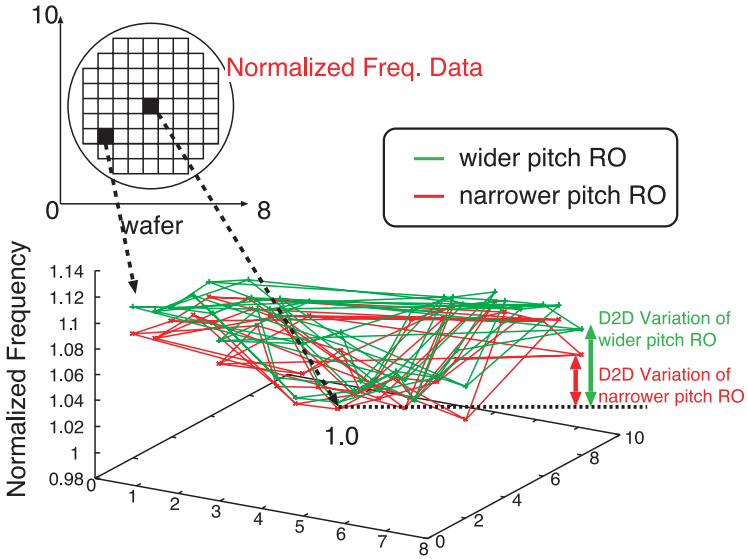

Fig. 15 Wafer mapping of WID-μ of each RO.

NAND cells introduced in the Section 3, that is, three types of two-inputs NAND with different levels of regularity in the 90 nm process. Hereafter, we write RO-jog, RO-jog with dummy and RO-straight with dummy as the ring oscillator made by NAND2-jog, NAND2-jog with dummy and NAND2-straight with dummy in the Sec. 3, respectively. Additionally, we examine similar cells in a 45 nm process: RO-straight with dummy and RO-straight without dummy.

Table 3 summarizes the results of test chip measurement. The value of mean oscillation frequency μ is normalized by the mean oscillation frequency of the fastest RO in each technology node.

Figure 16 shows the distribution of measured WID oscillation frequencies of a test chip for RO-jog, RO-jog with dummy and RO-straight with dummy circuits in the 90 nm process. Since major source of WID variability is random dopant fluctuation in channel region [13], the difference in printability of gate-poly does not leads to large difference in the amount of WID variation. From Fig. 16 and Table 3, WID-σ/μ of RO-straight with dummy and that of RO-jog with dummy

Table 2 Measurement result of INVERTER RO frequency.

	90 nm		65 nm		45 nm LotA		45 nm LotB	
RO stages	19		29		59		59	
pitch [nm]	780	390	630	315	420	210	420	210
μ	1.0	0.972	1.0	0.975	1.0	0.89	1.0	0.95
WID-σ/μ [%]	1.09	1.08	0.969	0.782	1.60	1.16	1.16	1.00
D2D-σ/μ [%]	3.22	2.90	1.54	1.24	6.86	4.67	4.07	3.57

Table 3 Measurement result of NAND2 RO frequency.

	90 nm			45 nm LotA		45 nm LotB	
RO stages	19			59		59	
RO type	jog	jog w/ dummy	straight w/ dummy	straight w/o dummy	straight w/ dummy	straight w/o dummy	straight w/ dummy
μ	1.0	0.976	0.953	1.0	0.90	1.0	0.93
WID-σ/μ [%]	1.20	1.11	1.06	1.16	1.02	0.98	0.98
D2D-σ/μ [%]	3.09	3.04	3.06	5.22	4.24	3.62	3.31

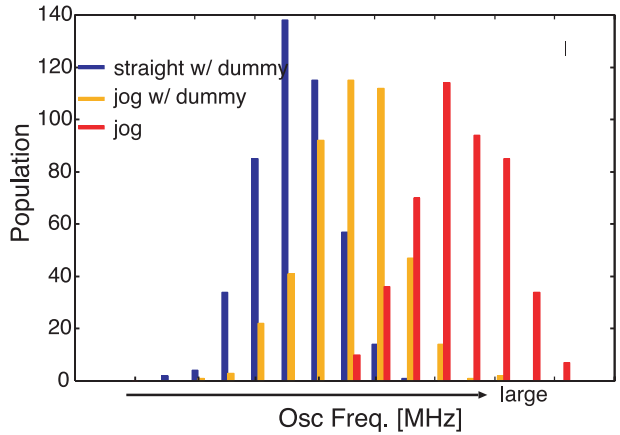

Fig. 16 Measured WID distribution of NAND2-RO oscillation frequency in the 90 nm process

are 12% and 7% smaller than that of RO-jog, respectively. RO-straight with dummy exhibits a smaller WID variation than RO-jog with dummy, whereas NAND2-jog with dummy exhibits a slightly better gate-length stability than NAND2-straight with dummy in the 65 nm photolithography simulation. A possible reason for the discrepancy may include, besides the difference in process technology, layout dependency of gate etch process after the photolithography of poly patterns [9]. From Fig. 16 and Table 3, μ of RO-straight with dummy and that of RO-jog with dummy are 4.7% and 2.4% smaller than that of RO-jog, respectively. The performance overhead observed is similar to that incurred by parasitic increase, as shown in Fig. 11. Table 3 shows that there is no meaningful difference in D2D variation. The strong regularity of single pitch enforcement with dummy insertion has performance overhead while reducing the WID variability moderately.

In the 45 nm process, μ of RO-straight with dummy for lot A is 10% smaller than that of RO-straight without dummy, and 7.0% for lot B. Similar to the inverter ROs in Table 2, it is expected to exist other sources of performance spread than parasitic capacitance associated with dummy patterns. D2D-σ/μ of RO-straight with dummy is 19% smaller than that of RO-straight without dummy for lot A, and 8.6% for lot B.

From those measurements, we confirmed that layout regularity helps to reduce performance variability. At the same time, it incurs performance overhead due to increase in parasitics. It is therefore important to find the best trade-off for each technology node.

5. Conclusion

In this paper, we evaluate the effect of regularity on variation control and circuit performance by lithography and circuit simulation, and test-chip measurements in three technology nodes of 90 nm, 65 nm and 45 nm.

From the results of lithography simulation, regularity-enhanced design, especially narrower pitch layout, clearly improves pattern fidelity under defocus. Dummy pattern insertion for regularity enhancement leads to delay increase, however, which is estimated around 1% in actual circuits with fanout-four loading.

From the variability of measured oscillation frequencies, layout regularity helps to reduce performance variability, with some amount of performance overhead. The amount of variability reduction and performance overhead varies depending on the process technology used. For example, in 65 nm test chips, inverter ROs that have the smallest poly pitch with dummy poly insertion exhibits 19% reduction of WID and D2D variation with delay overhead of 2.5%, compared to the ROs without dummy-poly insertion.

It is interesting to note that a dense regularity-enhanced layout, which is expected to have better printability under defocus, exhibits smaller D2D variability which corresponds to better performance uniformity over a wafer in all processes. At the same time, dummy-poly patterns result in delay increase. It is therefore important to obtain the best trade-off among performance overhead and variability reduction for each process technology.

Acknowledgments The 90 nm and 65 nm VLSI chips in this study have been fabricated through the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with STARC (90 nm and 65 nm), ASPLA Corp.(90 nm), e-Shuttle, Inc.(65 nm), and Fujitsu Ltd.(65 nm). The 45 nm VLSI chip has been fabricated by Renesas Technology Corp.

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