Evaluation of Soft-Error Tolerance by Neutrons and Heavy Ions on Flip Flops with Guard Gates in a 65 nm Thin BOX FDSOI Process

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***Abstract*—We evaluated soft-error tolerance by neutrons and heavy ions on four types of flip flops (FFs) called DFF, guard-gate FF (GGFF), feedback recovery FF (FRFF) and dual FRFF (DFRFF) in a 65nm thin BOX FDSOI. FRFF has a guard-gate structure only in the master latch. GGFF and DFRFF have the guard-gate structure in both of master and slave latches. The guard-gate structure resolves an SET pulse by delaying it through the guard gate. FRFF and DFRFF have smaller area and shorter delay overheads than GGFF. We revealed that the guard-gate structure has high soft-error tolerance by low-LET heavy ions, but the larger-LET ions over 40 MeV-cm^2/mg cause upset even in the guard-gate structures. We revealed that longer delay in the guard-gate can resolve these issues by circuit simulations.**

***Index Terms*—soft error, heavy ion, neutron, FDSOI, flip-flop, low delay overhead, guard-gate structure.**

I. Introduction

Reliability issues have become a significant concern due to soft errors with technology downscaling [1]. Soft errors are one of temporal failures that flip stored values in storage elements such as flip flops (FFs) or SRAMs by neutrons and heavy ions from cosmic rays. When a radiated particle hits transistors, the perturbation in the output node is generated, which is called a single event transient (SET) pulse. A SET pulse will cause a single event upset (SEU).

In the device level, fully-depleted silicon on insulator (FD-SOI) processes have 50-100x higher soft-error tolerance than conventional bulk processes without any performance overhead [2][3]. It is because the buried oxide (BOX) layer prevents charge from being collected from substrate to drain [4]. In the circuit level, several redundant FFs such as triple modular redundancy (TMR) [5] and dual interlocked storage cell (DICE) [6][7] have been proposed for effective countermeasures. However, they have longer delay time, larger area and power consumption than conventional standard FFs. Therefore, FFs with lower overhead and higher radiation hardness must be required. A stacked FF in [8] was proposed as one of non-redundant FFs. It has high soft-error tolerance, smaller area and power consumption compared with redundant FFs. However, even the stacked FF has longer delay time, larger area and power consumption than conventional standard FFs. Reference [9] evaluates performance and soft-error tolerance of DFF and the stacked FF in an advanced 28 nm FDSOI process. The power consumption and C-Q delay of the stacked FF are 1.9x and 1.8x larger than those of DFF.

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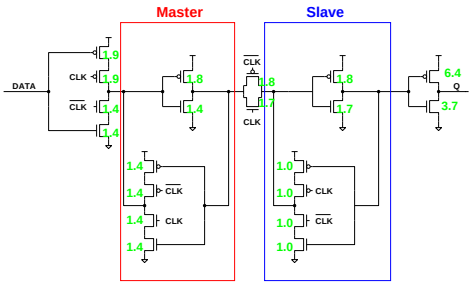


Fig. 1. DFF

The reference evaluated soft-error tolerance by Kr and Xe. The linear energy transfers (LETs) of Kr and Xe are 25 and 50 MeV-cm^2/mg. The LET is the amount of energy that an ionizing particle transfers to the material traversed per unit distance. The stacked FF has 15x and 36x higher soft-error tolerance than DFF by Kr and Xe.

Reference [10] evaluates soft-error tolerance of DFF in a 28 nm and a 65 nm FDSOI process by Ar and Kr. The LETs of Ar and Kr are 15.8 and 40.3 MeV-cm^2/mg. DFF in 28 nm is 18x and 16x higher than that in 65 nm.

In this paper, we measured radiation tolerance of several FFs including conventional and proposed FFs. We explain several types of radiation-hard flip flops evaluated soft-error tolerance in a 65 nm FDSOI process in Section Ⅱ. Section Ⅲ explains experimental setups. Section Ⅳ explains experimental results by neutrons and heavy-ion irradiation. Section V explains the discussion. We conclude this paper in Section Ⅵ.

II. Flip Flops to Evaluate Soft-Error Tolerance

Standard Flip Flop

Figure 1 shows a standard FF called DFF. It has no tolerance against soft errors.

Guard-Gate FF

Figure 2 shows the guard-gate structure that consists of a delay element including two inverters and a C-element [11]. When the value on IN1 node is changed because of SET pulses, the value on IN2 node is delayed by the two inverters. Therefore, the C-element keeps a previous correct input value

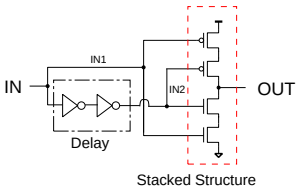


Fig. 2. Guard-gate structure

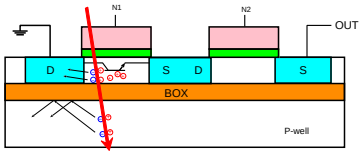


Fig. 3. Stacked structure to suppress a simultaneous upset of the series-connected structure

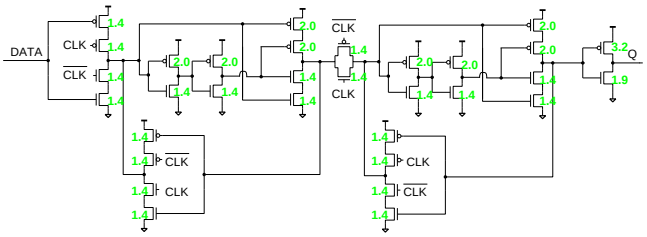


Fig. 4. Guard-gate flip flop (GGFF)

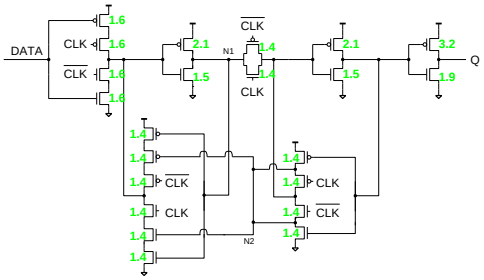


Fig. 5. Feedback recovery flip flop (FRFF)

if the length of the SET pulse is shorter than the delay of the two inverters. The guard gate eliminates all SET pulses which are shorter than the delay of two inverters. The C-element is intrinsically composed of the stacked structure that is strong against soft errors in the SOI process. Series-connected stacked NMOS and PMOS transistors (Fig. 3) are rarely flipped at the same time because their body and diffusion layers are separted by the BOX layer [8]. Therefore, SET pulses from the C-element are suppressed.

Figure 4 shows the guard-gate FF (GGFF) [12]. GGFF has the guard-gate structure in the master and slave latches to prevent an SEU. However, it has larger area and delay overheads than standard FFs because 12 more transistors are added to DFF.

Feedback Recovery FF

Figure 5 shows the proposed feedback recovery flip flop (FRFF) composed of two more inverters than DFF [13]. FRFF has high soft-error tolerance only in the master latch because it embeds the guard-gate structure only in the master latch. Figure 6 shows the latch state at CLK = 1 when the slave latch works as a delay element.

Dual FRFF

Figure 7 shows the proposed dual feedback recovery flip flop (DFRFF) composed of four more inverters than DFF [13].

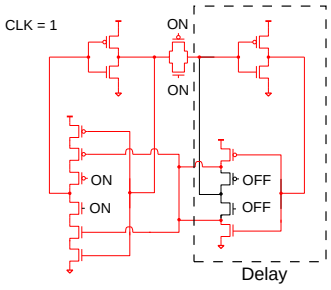


Fig. 6. Latch state at CLK = 1 in FRFF

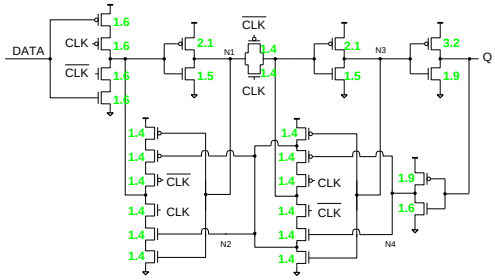


Fig. 7. Dual feedback recovery flip flop (DFRFF)

TABLE I
SIMULATION RESULTS OF AREA, D-Q DELAY, POWER AND NUMBER OF TRANSISTOR OF EACH FF AT V_{DD}= 1.2 V. ALL VALUES ARE NORMALIZED TO THOSE OF DFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF GGFF [13].

FF	D-Q delay	Area	Power	# of Tr.
DFF	1	1	1	24
GGFF	2.20 (1)	1.47 (1)	1.06 (1)	36
FRFF	1.06 (0.48)	1.06 (0.72)	1.03 (0.97)	26
DFRFF	1.08 (0.49)	1.18 (0.80)	1.02 (0.96)	30

DFRFF has high soft-error tolerance in both of the master and slave latches because the guard-gate structure is also embedded in the slave latch. In the slave latch, the output inverter and the feedback inverter work as the delay element of the guard-gate structure.

Table I shows the results of delay time, power consumption at 10% data activity and area of DFF, GGFF, FRFF and DFRFF using circuit simulations at supply voltage ($V_{\rm dd}$) = 1.2 V quoted from [13]. The results include parasitic resistance and capacitance. D-Q delay is the delay time that is the sum of the setup time and C-Q delay time in an FF. The power consumption and D-Q delay of FFs are evaluated by attaching 4 inverters as fanout load. All values are normalized to those of DFF. The values in parentheses are normalized to those of GGFF. The delay time and the area of GGFF are 2.2x longer and 1.4x bigger than those of DFF, but the delay time and the area of FRFF are 52% shorter and 28% smaller than those of GGFF. The delay time and the area of DFRFF are 51% shorter and 20% smaller than those of GGFF.

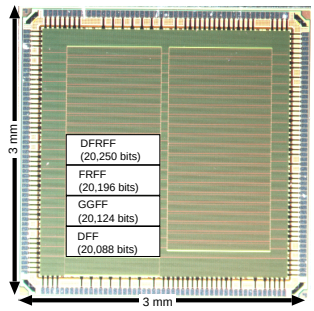


Fig. 8. 65 nm FDSOI chip micrograph that contains 20,088 bit standard DFFs, 20,124 bit GGFFs, 20,196 bit FRFFs and 20,250 bit DFRFFs.

TABLE II
LET, ENERGY AND FLUENCE OF HEAVY IONS.

Ion	Ar	Kr
LET [MeV-cm^2/mg]	17	40
Energy [MeV]	150	322
Fluence [n/cm^2]	1.1×10^6	9.6×10^5

III. Experimental Setup

A test chip was fabricated in a 65 nm thin BOX FDSOI process in order to evaluate soft-error tolerance [14]. Figure 8 shows the chip micrograph that contains 20,088 bit standard DFFs, 20,124 bit GGFFs, 20,196 bit FRFFs and 20,250 bit DFRFFs. All FFs are connected in series to form a shift register [15]. We evaluated soft-error tolerance by neutrons and heavy ions.

Heavy-ion irradiation tests were conducted by Ar and Kr at Cyclotron and Radioisotope Center (CYRIC), Tohoku University, Japan. Figure 9 (b) shows the experimental setup of the heavy-ion irradiation tests. Device under tests (DUTs) are sealed in the chamber in order to keep ion energy. Table II shows linear energy transfer (LET), energy and average fluences of heavy ions. Figure 10 shows the existence probability of heavy ions in outer space [16]. The number of particles with over 40 MeV-cm^2/mg is much less than that with less than 40 MeV-cm^2/mg in outer space [16]. Secondary ions by a neutron the hit to Si is mainly less than 18 MeV-cm^2/mg which is close to LET of Ar [17].

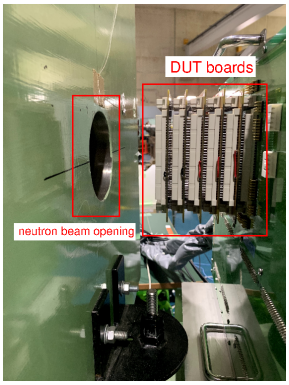
Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1). $V_{\rm dd}$ was 0.8 V and 1.2 V at heavy-ion irradiation. Each irradiation time was for 30 second. The standard voltage in the 65 nm thin BOX FDSOI is 0.8 V. We also measured soft-error tolerance to evaluate supply-voltage dependence at 1.2 V.

Cross Section (CS) is used in order to evaluate soft-error tolerance, which means an area of upsets when a particle passes a circuit block. The soft-error tolerance becomes stronger if CS becomes smaller. Equation (1) is used in order to calculate CS [18].

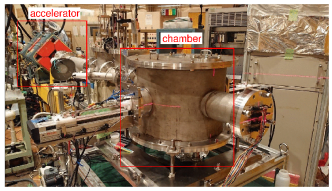
$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\rm error}}{N_{\rm ion}\ N_{\rm FF}} \qquad (1)$$

$N_{\rm ion}$ is the effective heavy-ion fluence per cm^2.

Spallation neutron tests were conducted at the research center for nuclear physics (RCNP), Osaka University, Japan [19]. Figure 9 (a) shows the experimental setup of neutron



(a) Neutron irradiation setup.



(b) Heavy-ion irradiation setup.

Fig. 9. Measurement setup.

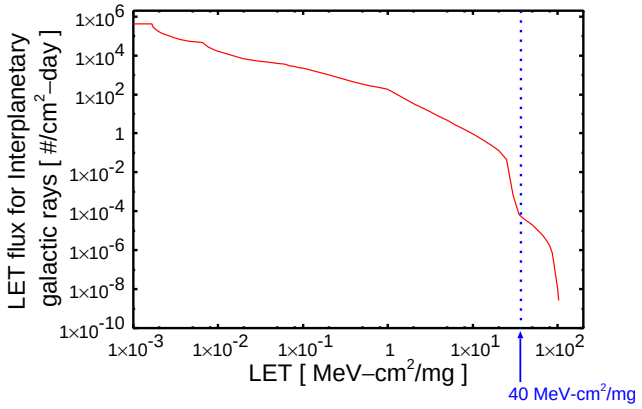


Fig. 10. LET distribution of heavy ions in outer space [16].

irradiation tests. Figure 11 shows the normalized neutron beam spectrum in comparison with the terrestrial neutron spectrum at the sea level in New York City (NYC). The average acceleration factor (AF) is 3.77×10^8 compared with the sea level in NYC. In order to increase the number of upset FFs within a limited time, five stacked DUT boards each of which includes two test chips were exposed to the neutron beam. As a result, 10 chips were measured simultaneously. Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1). $V_{\rm dd}$ was decreased from 0.8 V to 0.6 V at the neutron irradiation because there was no error on DFF even at $V_{\rm dd}$ was 0.8 V. Stored values were shifted every 300 second. Soft-error rates (SERs) are calculated using Eq. (2).

$$SER\ [\mathrm{FIT/Mbit}] = \frac{N_{\rm error} \times 10^9\ \mathrm{hour} \times 1\ \mathrm{Mbit}}{(300\ \mathrm{sec}/3600\ \mathrm{sec}) \times AF \times N_{\rm FF}} \qquad (2)$$

$N_{\rm error}$ is the number of errors, and $N_{\rm FF}$ is the number of FFs.

IV. Experimental Results

A. Heavy-Ion Results

Figures 12 and 13 show the experimental results of the CSs by Ar and Kr at $V_{\rm dd}$ = 0.8 V with error bars of 95% confidence.

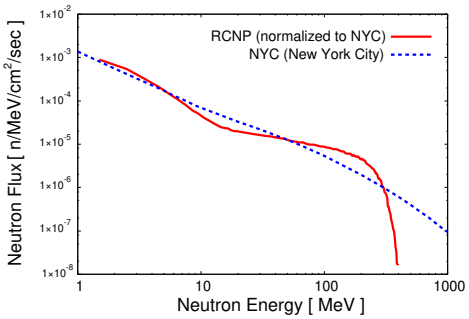


Fig. 11. Normalized energy spectrum of spallation neutron beam at RCNP and neutron at the sea level of NYC.

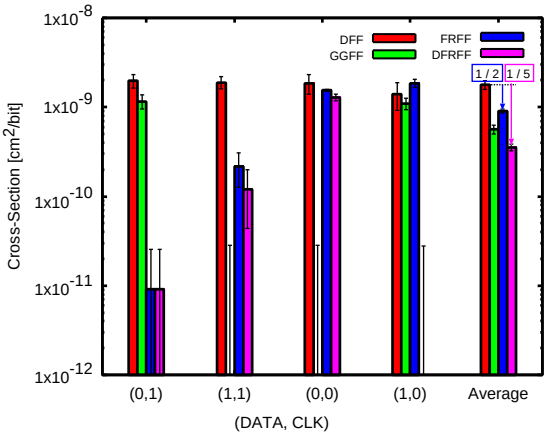


Fig. 12. Experimental results of the CSs by Ar irradiation at $V_{\rm dd}$ = 0.8 V.

The average CSs of FRFF are 1/2 smaller than those of the standard DFF by Ar and Kr. The average CSs of DFRFF are 1/5 and 1/3 smaller than those of the standard DFF by Ar and Kr respectively.

Figures 14 and 15 show the experimental results of the CSs by Ar and Kr at $V_{\rm dd}$ = 1.2 V with error bars of 95% confidence. The average CSs of FRFF are 1/3 and 1/2 smaller than those of the standard DFF by Ar and Kr respectively. DFRFF is weakest against soft errors at (DATA, CLK) = (0, 0) by Ar. The average CSs of DFRFF are 1/20 and 1/6 smaller than those of the standard DFF by Ar and Kr respectively.

The tendency of the results is same even if $V_{\rm dd}$ decreases. The smaller $V_{\rm dd}$ is, the longer the delay time becomes. However, lower $V_{\rm dd}$ makes an SET pulse longer and charge stored in nodes are decreased as supply voltage becomes small [13]. Therefore, the smaller $V_{\rm dd}$ is, the larger CSs becomes.

B. Neutron Results

Figure 16 shows the experimental result of the SERs by neutrons irradiation with error bars of 95% (2σ) confidence. Table III shows the average numbers of upsets on DFF, GGFF, FRFF and DFRFF. The SERs on all FFs are within error bars because there was less than one error in average due to the short measurement time. There was no error on GGFF at all static conditions. SERs on DFRFF only becomes large at (DATA, CLK) = (0, 0). This tendency is similar to the results from Ar. The average SERs of FRFF and DFRFF are 1/3 and 1/5 smaller than that of the standard DFF respectively.

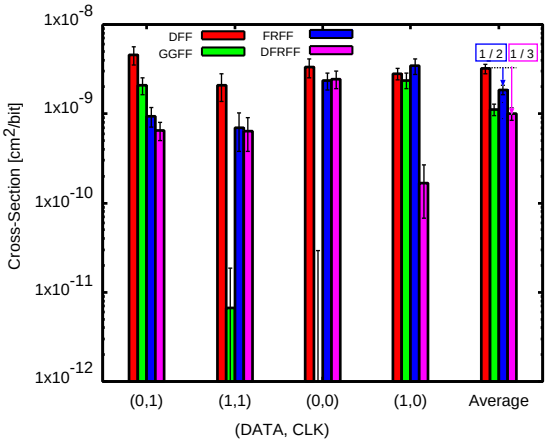


Fig. 13. Experimental results of the CSs by Kr irradiation at $V_{\rm dd}$ = 0.8 V.

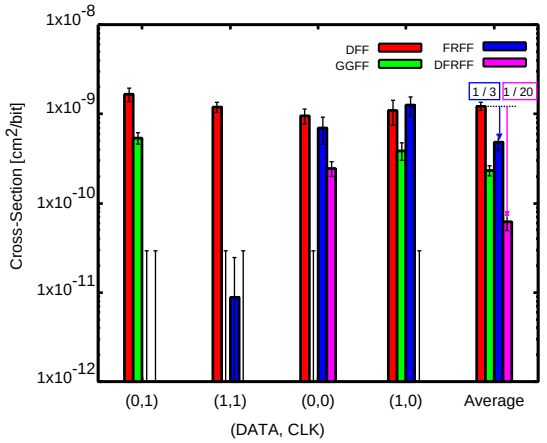


Fig. 14. Experimental results of the CSs by Ar irradiation at $V_{\rm dd}$ = 1.2 V.

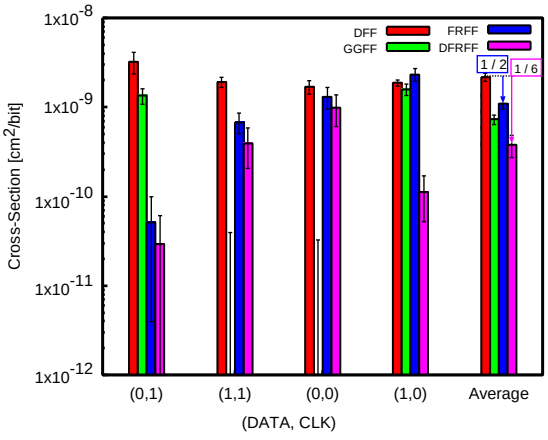


Fig. 15. Experimental results of the CSs by Kr irradiation at $V_{\rm dd}$ = 1.2 V.

V. **Discussions**

The electron mobility is generally larger than the hole mobility [12] [20]. Due to the mobility difference, NMOS transistors are more susceptible to soft errors than PMOS transistors. Therefore, in terms of soft error mitigation techniques, we must take care of NMOS transistors more than PMOS transistors in logic circuits based on a CMOS technology. In the 65 nm technology, the drain-source current of NMOS is 1.35x larger than that of PMOS at the same size. The transistor

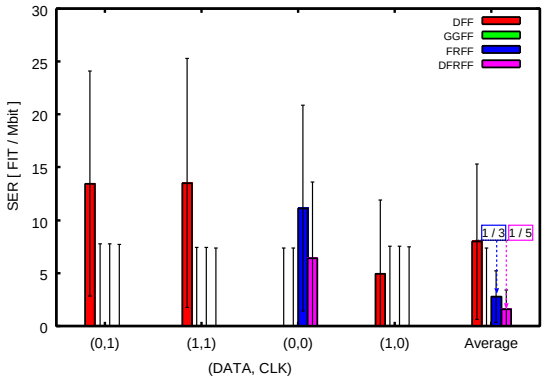


Fig. 16. Experimental results of the SERs by neutron irradiation.

TABLE III
AVERAGE NUMBERS OF UPSETS AND TOTAL NUMBERS OF FFS IN THE 65 NM THIN-BOX FDSOI PROCESS BY α PARTICLES.

chip (FF)	(DATA,CLK)				average
	(0,1)	(1,1)	(0,0)	(1,0)	
DFF	0.16	0.14	0	0.05	0.09
GGFF	0	0	0	0	0
FRFF	0	0	0.14	0	0.03
DFRFF	0	0	0.08	0	0.02

sizes on PMOSs in the inverters of GGFF, FRFF and DFRFF become 1.4x larger than those of NMOSs to equalize the drain-source current. In [21], soft errors caused by Ar and Kr hits on NMOS transistors account for 98% and 90% respectively. Therefore, we assume that SET pulses are generated only from NMOS transistors.

A. NMOS Affected by a Radiation Strike on GGFF, FRFF and DFRFF at Each Condition

From Fig. 12 to 15, GGFF is stronger against soft errors at (DATA, CLK) = (0, 0), (1, 1) than (0, 1), (1, 0). Figure 17 shows the C-element affected by a radiation strike at these conditions. At (DATA, CLK) = (1, 1), (0, 0), the master or slave latches are flipped by a SET pulse from the C-elements. At (DATA, CLK) = (0, 1), (1, 0), they are flipped by a SET pulse from the tristate inverter. The C-element is strong against a SET pulse since two off-state transistors are stacked when two inputs are equal. A SET pulse from the tristate inverter, however, may flip the master or slave latch if the pulse width is more than the delay of the two inverters as the guard gate. The tristate inverter has weaker drive strength than the inverter due to the transistor stacking. The smaller current is, the longer a SET pulse becomes. The smallest CSs at (0, 0), (1, 1) are due to the C-elements, while the larger CSs at (0, 1), (1, 0) are due to the insufficient delay time of the guard-gate structure. The delay time of the guard-gate structure is 33.8 ps in the master latch and 34.8 ps in the slave latch at $V_{\rm dd}$ = 1.2 V.

From Fig. 12 to Fig. 14, FRFF is stronger against soft errors at CLK = 1 than at CLK = 0. These results revealed that the guard-gate structure has high soft-error tolerance. However, CSs on DFRFF only becomes large at (DATA, CLK) = (0, 0). Figure 18 shows the inverter or tristate inverter affected by a radiation strike at all conditions. At (DATA, CLK) = (0, 1) or (1, 0), the master or slave latch becomes strong against a radiation strike since the stacked clocked inverter produces almost no SET pulse due to its stacked structure [22]. On the other hand, at (DATA, CLK) = (0, 0), a SET pulse from the inverter before N3 may flip the latch. In the fabricated DFRFF, the delay time of the two inverters after N3 in the slave latch is insufficient (25.7 ps at $V_{\rm dd}$ = 1.2 V) and increases CS at (0, 0). We should evaluate the delay time composed of guard-gate structure because soft-error tolerance of an FF with guard-gate structure depends on the delay.

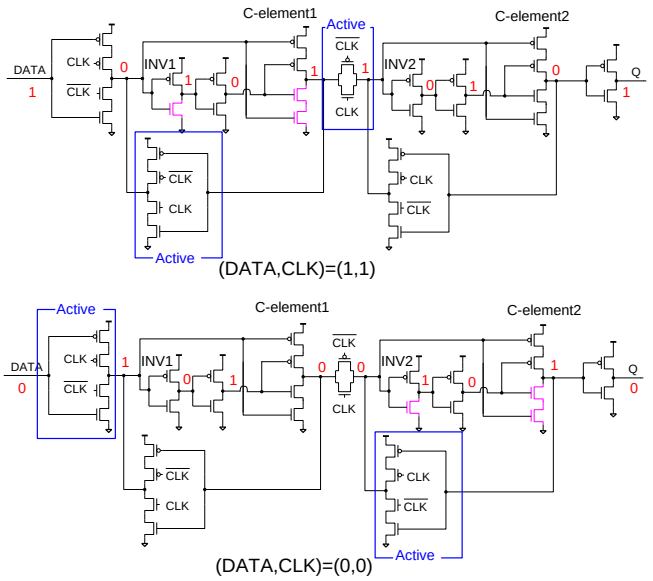


Fig. 17. NMOS transistors sensitive to a heavy-ion hit at (DATA, CLK) = (0, 0), (1, 1) in GGFF.

B. Simulations of Delay Time on Guard-Gate Structure and Dependence on Supply Voltage

The delay times from N1 to N2 in Figs. 5, and 7 are evaluated by circuit simulations when the radiated particle hits the NMOS of FRFF and DFRFF at (DATA, CLK) = (1, 1) as shown in Fig. 18. The delay time from N3 to N4 in Fig. 7 is also evaluated when the radiated particle hits the NMOS of DFRFF at (DATA, CLK) = (0, 0). Table IV shows the results of the delay time. Figure 19 (a) compares CSs and delay time at $V_{\rm dd}$ = 1.2 V. Netlists with parasitic components are used on circuit simulations.

The delay time on DFRFF at (DATA, CLK) = (0, 0) is shortest and the delay time on DFRFF at (DATA, CLK) = (1, 1) is longest as shown in Table IV. DFRFF has the guard gate composed of the output inverter at (DATA, CLK) = (0, 0), and the transistor size of the output inverter is large. The larger the transistor size is, the shorter the delay time becomes. The guard-gate structure can eliminate longer SET pulses caused by a radiated particle as the delay time is longer. The longer the delay time is, the higher soft-error tolerance becomes. Therefore, DFRFF at (DATA, CLK) = (1, 1) is strongest against soft errors among FRFF at (DATA, CLK) = (1, 1) and DFRFF at (DATA, CLK) = (0, 0). DFRFF is weakest against soft errors at (DATA, CLK) = (0, 0). In Fig. 14, there was no error on DFRFF at (DATA, CLK) = (1, 1). The delay

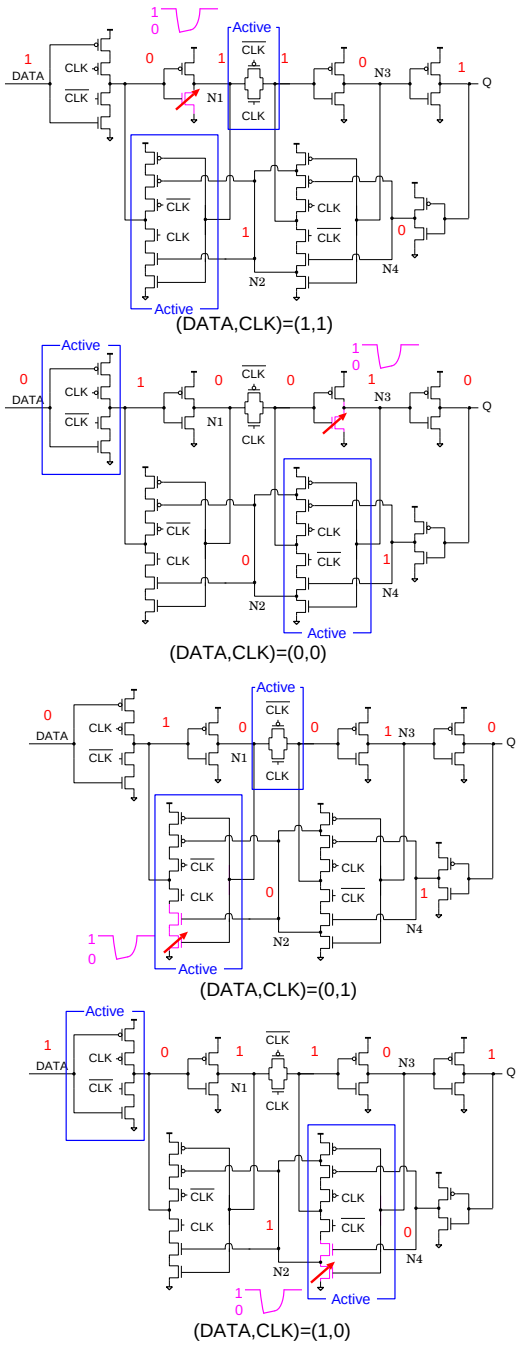


Fig. 18. NMOS transistors marked by the red arrows which are sensitive to a heavy-ion hit at all conditions in DFRFF.

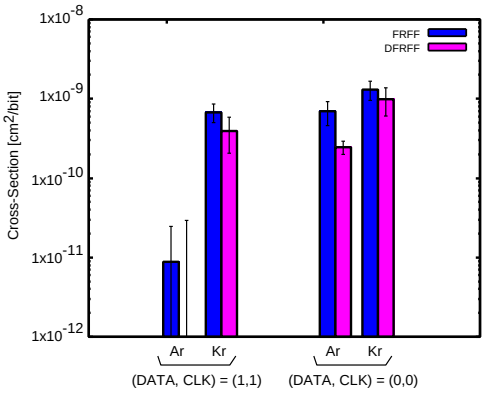
time composed of guard-gate structure is 76.9 ps as shown in Table IV. It can be seen that SET pulses caused by a radiated particle with 17 MeV-cm^2/mg are shorter than 76.9 ps. This tendency of the results are same as measurement results in Figs. 12 and 14.

From Fig. 12 to Fig. 15, FRFF and DFRFF are stronger against soft errors than DFF, while they are weaker against soft errors as the LET becomes larger. The larger LET is, the longer SET pulse becomes. The guard-gate structure could not block SET pulses because Some of them are longer than the delay of two inverters.

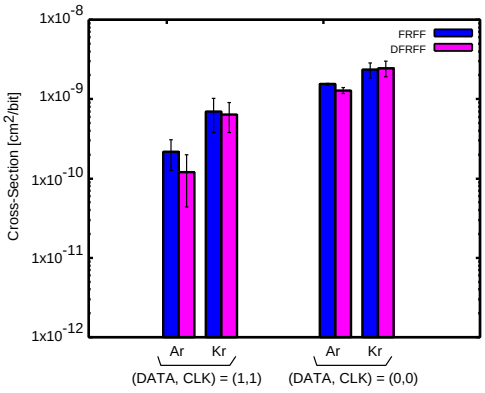
In Table IV, the smaller V_{dd} is, the longer delay time of

TABLE IV
DELAY TIME COMPOSED OF GUARD-GATE STRUCTURE.

		N1 to N2 [ps] (DATA, CLK) = (1, 1)	N3 to N4 [ps] (DATA, CLK) = (0, 0)
1.2 V	FRFF	73.3	n/a
	DFRFF	76.9	25.7
0.8 V	FRFF	159.3	n/a
	DFRFF	163.7	51.2



(a) V_{dd} = 1.2 V.



(b) V_{dd} = 0.8 V.

Fig. 19. CSs by heavy ions of FRFF and DFRFF at two static states.

the guard-gate structure becomes. However, the smaller V_{dd} is, the longer SET pulses become because of lower current to restore SET pulses. From Fig. 12 to 15, DFRFF at V_{dd} = 0.8 V has lower soft-error tolerance than that at V_{dd} = 1.2 V. Therefore, SET pulses prolong much more than the delay time of the guard gate by lowering supply voltage.

Since DFRFF has the guard-gate structure in its slave latch, it has soft-error tolerance at (DATA, CLK) = (0, 0), while FRFF has no guard-gate structure in its slave latch. We assume that DFRFF has higher soft-error tolerance than FRFF at this condition. Table IV shows the results of the delay time at V_{dd} = 1.2 V and 0.8 V. Figure 19 shows CSs by heavy ions of FRFF and DFRFF at two static states when V_{dd} is 1.2 V and 0.8 V. The guard-gate structure keeps delay time long at low V_{dd}, but in Fig. 19, we could not see any difference of CSs on DFRFF and FRFF at (DATA, CLK) = (0, 0) when V_{dd} is 0.8 V. Therefore, most of SET pulses generated by a particle hit are longer than 51.2 ps.

In [13], TCAD simulations revealed that the master latch of FRFF has soft-error resilience against a radiated particle up to 60 MeV-cm^2/mg. DFRFF has soft-error resilience against a radiated particle up to 60 MeV-cm^2/mg at all the static conditions. DFRFF has soft-error tolerance against a radiated particle up to 60 MeV-cm^2/mg even if $V_{\rm dd}$ is changed from 1.2 V to 0.6 V. However, experimental results revealed that the stored values of FRFF and DFRFF were flipped even by a radiated particle with 17 MeV-cm^2/mg. The guard-gate structure has weaker against soft errors by changed from $V_{\rm dd}$ = 1.2 V to $V_{\rm dd}$ = 0.8 V. It is necessary to increase the delay time of the guard-gate structure to eliminate soft errors.

VI. Conclusion

We measured radiation hardness of the standard DFF, GGFF, FRFF and DFRFF in the 65nm thin BOX FDSOI by neutrons and Ar and Kr ions. FRFF has the guard-gate structure only in the master latch. GGFF and DFRFF have the guard-gate structures in both of the master and slave latches. In the experimental results, the guard-gate structure is strong against soft errors by neutrons and heavy ions with LET below 17 MeV-cm^2/mg. However, the larger LET is, the weaker the guard-gate structure becomes against soft errors because higher-LET particles generate longer SET pulses. The guard-gate structure could not block SET pulses because the delay time of the two inverters as a delay element is shorter than SET pulses by higher-LET particles. We concluded that the delay in the guard-gate structures in both of FRFF and DFRFF is shorter than SET pulses generated by higher-LET particles. The guard-gate structures are effective against soft errors in terrestrial region in which secondary ions by neutrons have the LET with less than 18 MeV-cm^2/mg. However, they do not have enough soft-error tolerance in outer space. Guard gates with much longer delay must be required to protect longer SET pulses from heavy ion hits with larger LETs in outer space than secondary ions by a neutron hit in terrestrial region.

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