Analysis of Soft Error Rates in 65- and 28-nm FD-SOI Processes Depending on BOX Region Thickness and Body Bias by Monte-Carlo Based Simulations

Kuiyuan Zhang, Shigehiro Umehara, Junki Yamaguchi, Jun Furuta, and Kazutoshi Kobayashi

***Abstract*— This paper analyzes how body bias and BOX region thickness affect soft error rates in 65-nm SOTB (Silicon on Thin BOX) and 28-nm UTBB (Ultra Thin Body and BOX) FD-SOI processes. Soft errors are induced by alpha-particle and neutron irradiation and the results are then analyzed by Monte Carlo based simulation using PHITS-TCAD. The alpha-particle-induced single event upset (SEU) cross-section and neutron-induced soft error rate (SER) obtained by simulation are consistent with measurement results. We clarify that SERs decreased in response to an increase in the BOX thickness for SOTB while SERs in UTBB are independent of BOX thickness. We also discover SOTB develops a higher tolerance to soft errors when reverse body bias is applied while UTBB become more susceptible**

***Index Terms*— FD-SOI, Monte-Carlo simulation, radiation effects, TCAD.**

I. Introduction

SINGLE Event Upset (SEU) is caused by radiation induced charge collecting at a single sensitive node, such as the drain layer of a single transistor. Radiation-hardened circuits, such as Triple Modular Redundancy (TMR), or Dual Interlocked storage CEll (DICE) [1] have been employed to suppress the effects of multi-node charge collection. Silicon On Thin BOX (SOTB) [2] and Ultra Thin Body and BOX (UTBB) [3] are two FD-SOI processes with a thin BOX layer that can efficiently mitigate the charge collected into a device. Thus, they have higher soft error tolerance than bulk structures. Since FD-SOI requires no channel doping, threshold voltage variations resulting from fabrication process variability are reduced. The supply voltage of SOTB can be decreased to 0.4 V [4]. It is necessary to investigate the soft error tolerance of FD-SOI structure at lower voltages.

The charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. The drift and diffusion, as well as the parasitic bipolar effect (PBE) become dominant when a single event occurs in the circuit [5]. It is difficult to analyze SER while solely depending on circuit-level simulations such as SPICE; it is for this reason that TCAD simulation is indispensable. One drawback however is that there are only direct ionization models in TCAD simulation and more results are needed to perform dependable comparison with neutron- or alpha-induced SERs. Physical simulations such as indirectly ionizing radiation to get a directly ionized model can increase the accuracy of TCAD simulation.

Body biasing is commonly used to reduce power consumption. The charge collection and well potential are also influenced by body bias when a particle hits a device in 130-nm [6] and 65-nm processes [7]. The soft error rates of radiation-hard structures have undergone dramatic changes due to technology downscaling. Thus, it is important to also estimate the soft error rates in 65-nm SOTB and 28-nm UTBB structures resulting from body biasing.

Our goal in this work is to determine the impact that body bias and BOX region thickness had on soft errors rates (SER) using two types of processes. We measured alpha- and neutron-induced SERs of 65-nm SOTB and 28-nm UTBB latches and evaluated the SERs by PHITS-TCAD, a Monte-Carlo based simulation. This simulation is similar to MRED [8], IRT [9] and PHYSERD [10]. PHITS [11] can perform neutron and alpha particle nuclear reactions and therefore it is commonly used to calculate circuit SERs [12], [13]. We compared the SER in FD-SOI device models with varying BOX-layer thickness to find correlations between box-thickness and susceptibility to soft errors.

The rest of this paper is organized as follows: section II introduces the PHITS-TCAD simulation methodology [14]; section III provides a comparison between PHITS-TCAD simulation results and alpha and neutron irradiation test results [15] and details the results obtained depending on thickness of BOX layer and body bias; section IV provides a final summary and conclusion for this paper.

II. PHITS-TCAD Simulation Methodology

A. PHITS-TCAD Simulation

Fig. 1 portrays a flow chart of the proposed SEU simulation. Our calculation model relies on a physics-based simulation

Manuscript received November 8, 2015; revised February 16, 2016 and April 26, 2016 and June 21, 2016 and July 5, 2016; accepted July 6, 2016. Date of publication July 9, 2016; date of current version August 17, 2016.

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Digital Object Identifier 10.1109/TNS.2016.2589268

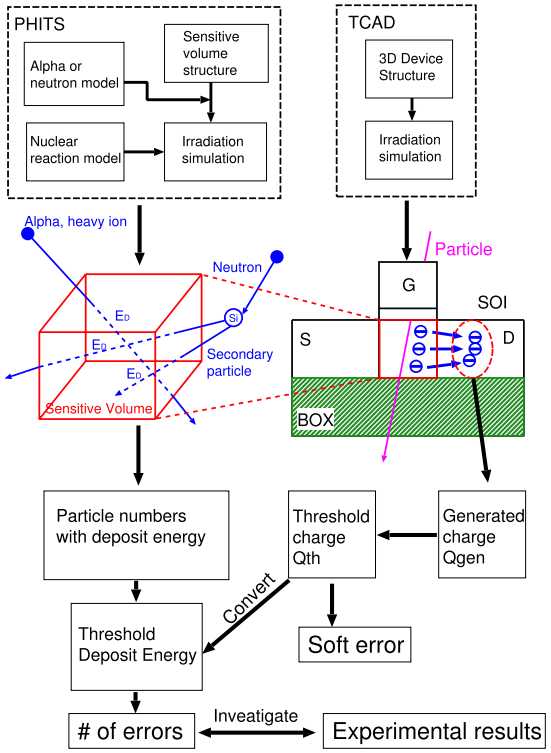


Fig. 1. Flow chart of the Monte Carlo PHITS and TCAD simulation system.

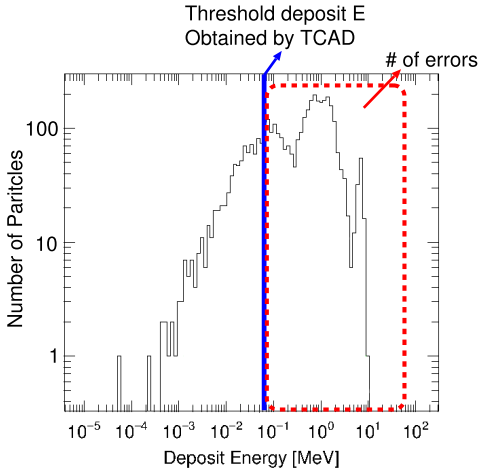


Fig. 2. PHITS calculation of the deposited energy. Each particle, with deposited energy exceeding the threshold energy, is counted as one SEU.

method, the Monte-Carlo simulation code system "PHITS" and an even by event simulation, TCAD, which we use to perform the SER analysis. PHITS simulates the nuclear reaction of an incident particle with constituent atoms in a device, and the sequential charge deposition. PHITS calculates the deposit energy when directed ion particles (heavy ion, alpha particle) or secondary particles crosses the user-defined volume of a device as shown in Fig. 1. The deposit energy (E_{D}) corresponds to the lost energy of the particle. Soft errors occur in a circuit whenE_{D} reaches the threshold value. All calculation modes for this study are refered to [10].

In the TCAD simulation, generated charge (Q_{gen}) is collected into drain by a particle hit as shown in Fig. 1. An SEU

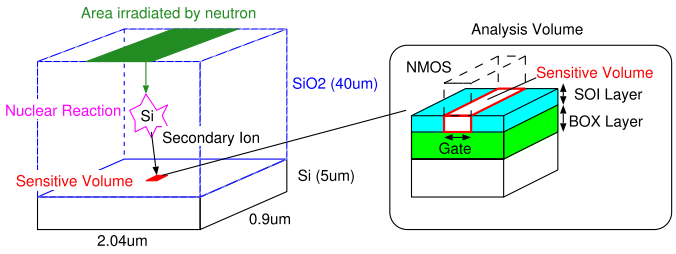


Fig. 3. Configuration of test device structure used in PHITS simulations. The SOI layers under G is regarded as the sensitive volume of the latch according to the TCAD simulation.

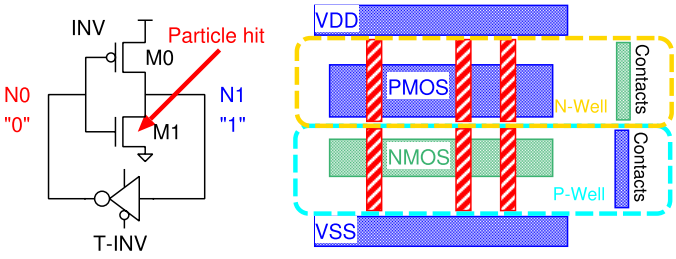
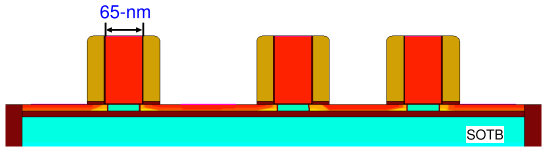
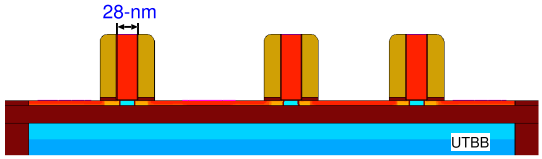


Fig. 4. Circuit and Layout structure of a conventional latch.



(a) The cross-section of 3D NMOS device model in the 65-nm SOTB structure.



(b) The cross-section of 3D NMOS device model in the 28-nm UTBB structure.

Fig. 5. The device-level models.

occurs in the circuit when enough Q_{gen} is accumulated. Q_{gen} which upsets the latch circuit is denoted as threshold charge (Q_{th}) and is used to calculate the threshold E_{D}. Q_{gen} can be converted to E_{D}. In silicon, it takes 3.6 eV energy to create an electron-hole pair, and the charge of an electron is 1.6 x 10^{-19} C. Thus E_{D} of 1 MeV is equivalent to Q_{gen} of 44.5 fC [16].

Fig. 2 shows a PHITS simulation of the relationship between the number of particles and E_{D} in the sensitive volume. The blue solid lines represent the threshold E_{D} which is calculated from Q_{th} obtained by TCAD simulations. Particles in which E_{D} is larger than the threshold E_{D}, causes SEUs (# of errors) as shown in Fig. 2.

B. Simulation Setup

Fig. 3 gives a bird's-eye view of the device structure used in PHITS simulations and Fig. 4 shows an NMOS transistor in latch structure. The red box in Fig. 3 indicates

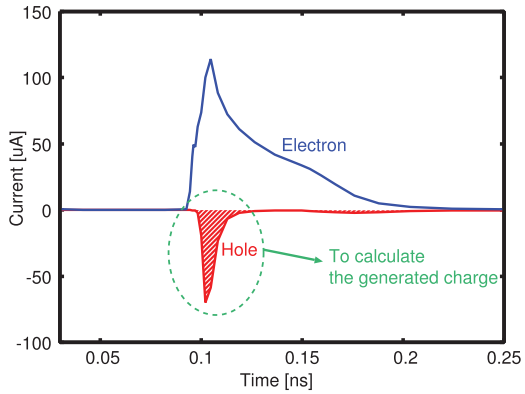


Fig. 6. Current waveforms by a particle hit. Blue current pulse is generated by electron collection, while the red is generated by hole collection. The generated charge collected by drift and diffusion is used to calculate Q_{th}.

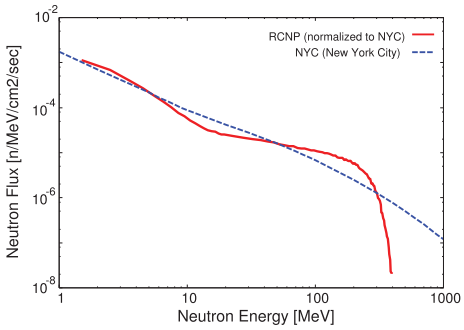
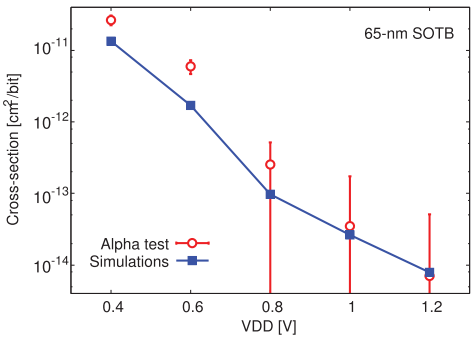
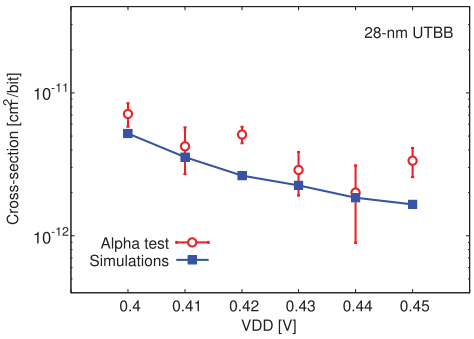


Fig. 7. Energy spectrum of spallation neutron beam.



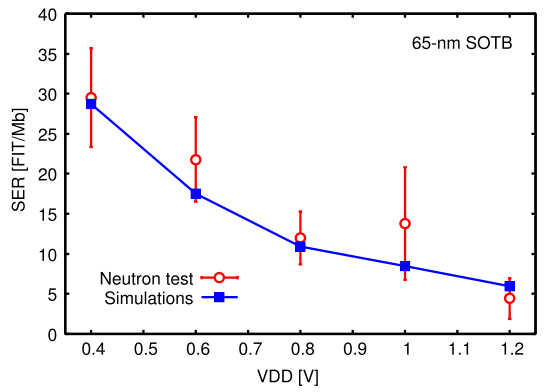
(a) The cross-section in SOTB structure according to the alpha irradiation experiments and simulations.



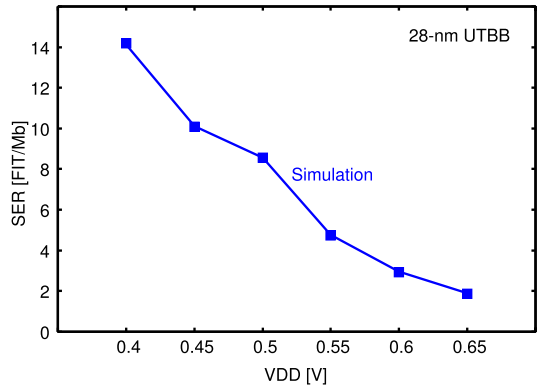
(b) The cross-section in UTBB structure according to the alpha irradiation experiments and simulations.

Fig. 8. Results of alpha irradiation experiments and PHITS-TCAD simulations.

a sensitive volume built based on the layout structures of the test chips. The SOI body under the gate of an inverter is regarded the sensitive volume. In the 65-nm SOTB process,



(a) The SERs of SOTB structure according to the neutron irradiation experiments and simulations.



(b) The SERs of UTBB structure according to the simulations.

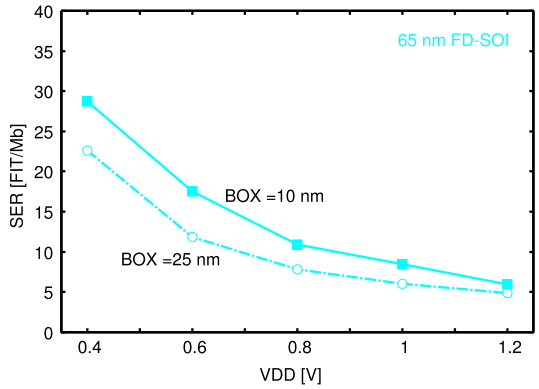
Fig. 9. Results of neutron irradiation experiments and PHITS-TCAD simulations.

the thickness of the thin BOX and SOI layer are 10 nm and 12 nm respectively while in the 28-nm UTBB process they are 25 nm and 7 nm respectively. The same structures are constructed in the TCAD simulations as in 3D device-models. Fig. 5 shows the cross-section of the 3D device NMOS models. The operating characteristics of the TCAD models are optimized to the SPICE model. Sentaurus TCAD is used for all simulations. An ion particle hits the center of the NMOS inverter gate. We use a classical Gaussian shape to account for the radial energy deposition distribution. The radius of the particle is 70 nm. TCAD simulations are performed by decreasing the supply voltages. We increase the linear energy transfer (LET) of the particles until the latch flipped. From this we obtain the Q_{th} for each supply voltage, which is almost equivalent to threshold LET multiplied by the thickness of SOI layer in FD-SOI process. We only consider particles that have a normal distribution in this paper We will discuss the direction and position effects in a future study.

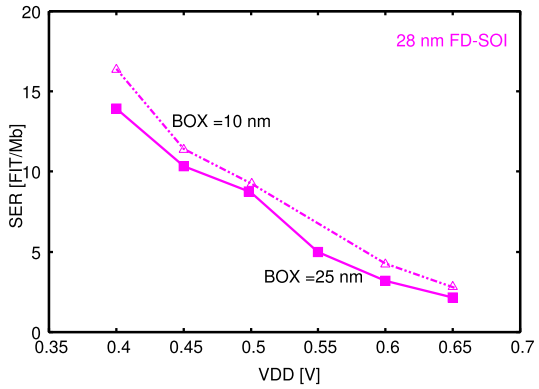
C. Q_{gen} Calculation by TCAD Simulations

PHITS is a Monte Carlo particle transport simulation code that does not consider the parasitic bipolar effect as in TCAD simulations. The charge deposited into the sensitive volume is used to calculate the Q_{gen}.

Fig. 6 shows two current waveforms of NMOS when a particle hits the SOI latch in Fig. 4 by TCAD simulations. The blue waveform is the current pulse by electrons collected



(a) Simulation results of 65-nm FD-SOI. SERs decrease by BOX layer thickened.



(b) Simulation results of 28-nm FD-SOI. SERs increased when the BOX layer got thinner.

Fig. 10. Results of neutron irradiation simulations by PHITS-TCAD tested against BOX layers of varying thickness.

into drain node, while red waveform is current pulse by holes collected into the source node. Blue waveform shows the Q_{crit}. We integrate the red current waveform to calculate the Q_{gen}.

III. Results and Discussion

We analyze the soft error rates of SOTB and UTBB structures according to supply voltages using the proposed PHITS-TCAD simulation and alpha irradiation experiments. A 3 MBq ^{241}Am alpha source of 1 cm^2 is used with an irradiation time of one minute.

Alpha-particle-induced SEU cross-section is calculated as follows:

$$CS_\alpha(\mathrm{cm}^2/\mathrm{bit}) = \frac{\mathrm{N_{error}}}{\mathrm{F}_\alpha \times \mathrm{N_{bit}}} \quad (1)$$

where N_{error} is the number of errors and F_α is the flux of alpha particles. F_α is number of generated alpha particles by alpha source ($3 \times 10^6 \times 60$ s $= 1.8 \times 10^8$)/cm^2 in one minute test time. However, one-half of the alpha-particles do not enter the test device since they are emitted isotropically from the alpha source [17]. Therefore, F_α is 9.0×10^7/cm^2 in experiments and simulations. N_{bit} is the number of bits.

The neutron irradiation experiments were done at Research Center for Nuclear Physics (RCNP) in Osaka Univ. The average accelerated factor of the neutron irradiation test is 3.84×10^8 and neutron spectrum is shown in Fig. 7. Sixteen test chips were measured simultaneously with four minutes of

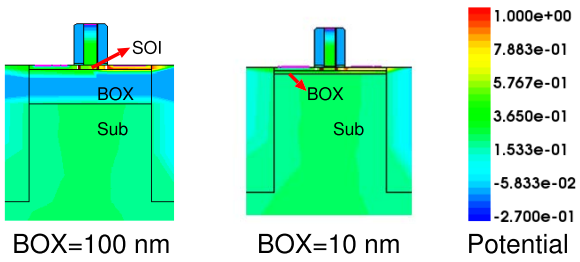
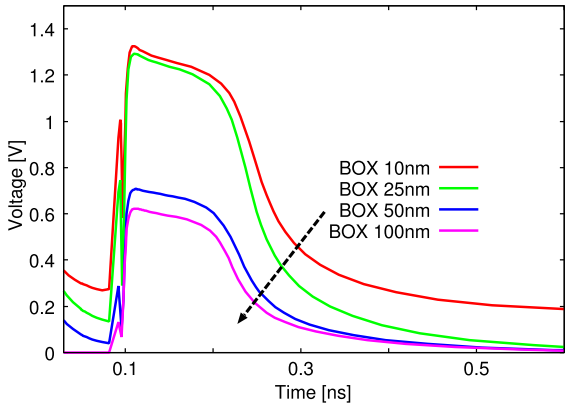
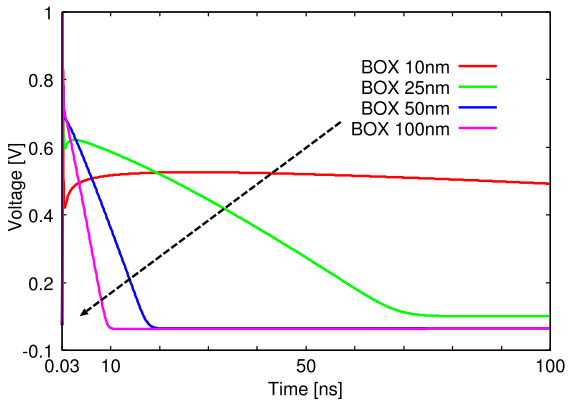


Fig. 11. The potential 10ns later a particle hits. The potential of the 10 nm BOX layer is higher than that of 100 nm thick BOX layer.



(a) The potentials of the BOX layer.



(b) The potentials of SOI layer depending on the thicknesses of BOX layer. It becomes easier to turn on the parasitic bipolar transistor when the thickness of BOX layer is much thinner.

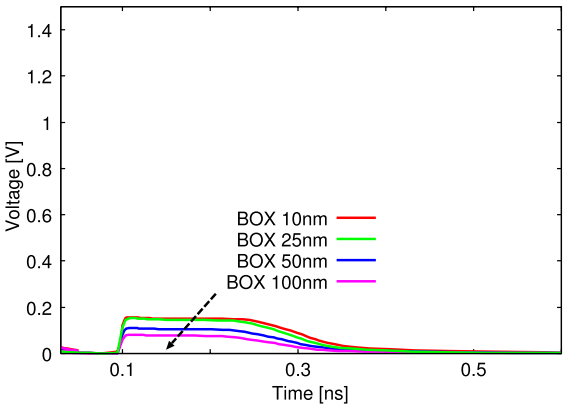
Fig. 12. The potential of BOX, SOI layer by the a particle hits on 65-nm FD-SOI structure.

irradiation allotted to one test. Neutron beams hit the test chips from a normal direction. The experimental setup and results of this section have been previously described in detail [15]. The experimental results of DFF in [15] were compared with the simulated results.

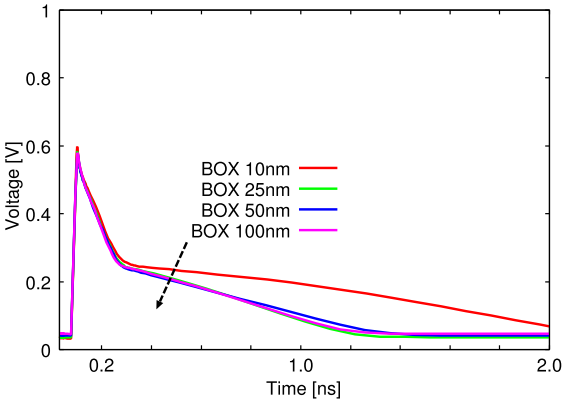
A. Comparison Between Measurement and Simulation

Fig. 8(a) shows the alpha cross-section of the PHITS-TCAD simulations and the experimental results of the SOTB structure. Supply voltage is swept from 1.2 V to 0.4 V.

In this PHITS simulation alpha particles number 1.8×10^8 per 1 cm^2. The area of the flip-flop is 4.08×1.8 μm^2 and the test chip has 1.06 kbit of FFs. The fact that the cross-section

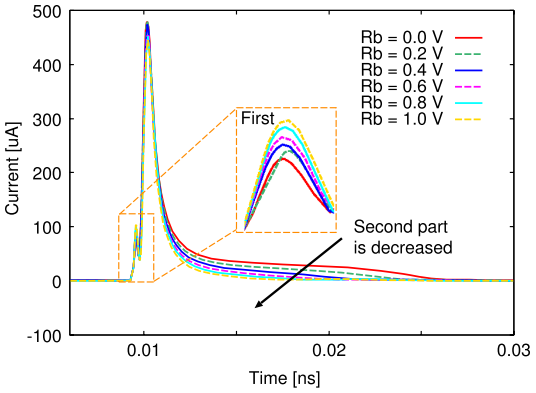


(a) The potentials of the BOX layer.

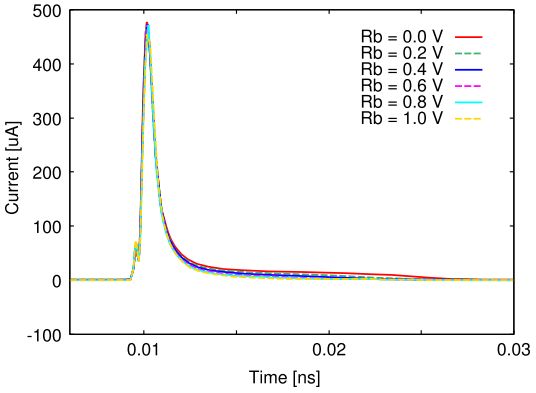


(b) The potentials of SOI layer depending for varying BOX layer thickness. It becomes easier to turn on the parasitic bipolar transistor when the BOX layer is much thinner.

Fig. 13. The potential of BOX, SOI layer by particle hits on 28-nm FD-SOI structure.



(a) The BOX layer is 10 nm thick



(b) The BOX layer is 25 nm thick

Fig. 14. The current waves by a particle hits depending on the reverse body bias on NMOS in the 65 nm FD-SOI structures.

increases when the supply voltage is reduced, suggests that it is easy to upset the SOTB latch by reducing the supply voltage. In this experiment, the SEU cross-sections when the supply voltage is 0.4 V is six times larger than at 1.2 V.

Fig. 8(b) shows the differential alpha cross-section based on the PHITS-TCAD simulations and experiments of the 28-nm UTBB No errors occured in the UTBB structure when the supply voltage exceeded 0.5 V, therefore, we reduce the supply voltage from 0.45 V to 0.4 V in the simulations and experiments. Alpha particles number 10^8 in the PHITS simulation and the area of one flip-flop is $2.04 \times 0.9\ \mu m^2$. The number of FFs in the test chip is 40 kbit.

When supply voltage was reduced from 0.45 V to 0.4 V, the SEU cross-section increased 2.5 times. Alpha test showed that, at this voltage the cross-sections of SOTB and UTBB were 1.33×10^{-11} cm^2/bit and 3.56×10^{-12} cm^2/bit respectively. As the sensitive volume in UTBB is smaller than in SOTB, it reduces the cross-section. The increase in SER observed as supply voltage was lowered from 1.2V to 0.4V.

Fig. 9(a) and 9(b) show the SERs by neutron irradiation experiments and PHITS-TCAD simulation calculated using the following equation:

$$SER_{\mathrm{SEU}}[\mathrm{FIT/Mb}] = \frac{3.6 \times 10^{18} \times \mathrm{N_{SEU}}}{\mathrm{T_{test}} \times \mathrm{AF} \times \mathrm{N_{bit}}} \qquad (2)$$

where N_{SEU} is the number of SEUs, T_{test} is the irradiation test time and AF is the accelerated factor of the neutron beam. However, in the PHITS-TCAD simulation, AF is calculated as:

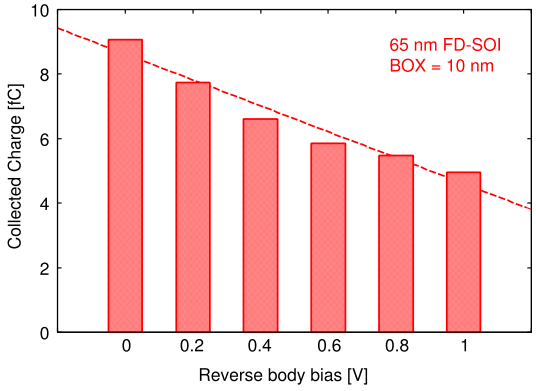
$$AF_{\mathrm{Sim}} = \frac{N_{\mathrm{n}}}{A_{\mathrm{n}} \times F \times T_{\mathrm{test}}} \qquad (3)$$

where A_{n} is the area irradiated by neutron in PHITS. N_{n} is the number of neutrons (10^9 in this study) and F is the neutron flux at sea-level in New York City.

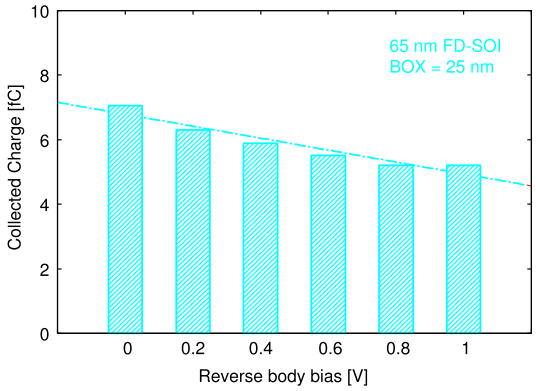
The results from PHITS-TCAD simulations are consistent with the neutron irradiation test results in the 65-nm SOTB (Fig. 9(a)). Neutron irradiation test detected no error in the 28-nm UTBB structure. Therefore, only the simulated results are shown in Fig. 9(b). PHITS-TCAD simulation reveals that the soft error tolerance of 28-nm UTBB is at least two times stronger than a 65-nm SOTB. Since the results of the PHITS-TCAD simulations and measured data correspond, we believe the SERs of several device models can be predicted by PHITS-TCAD simulation.

B. Influence of BOX Region Thickness on Neutron-Induced SER

To assess its effect on SER we adjust the BOX layer thickness in a 65-nm SOTB and 28-nm UTBB. BOX layer and SOI body in 65-nm FD-SOI are 10 nm and 12 nm respectively and 25 nm and 7 nm respectively in 28-nm FD-SOI. We analyze

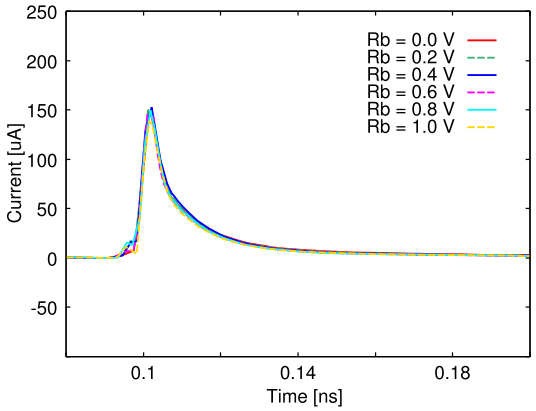


(a) The BOX layer is 10 nm thick

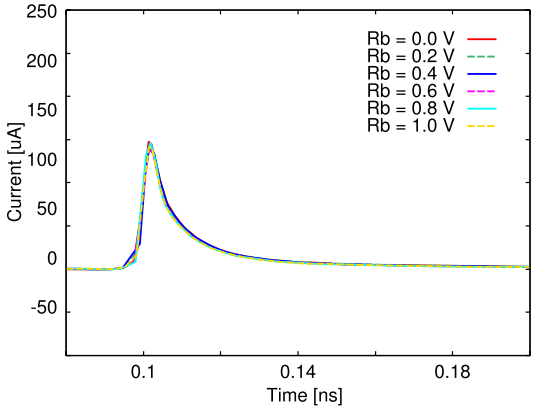


(b) The BOX layer is 25 nm thick

Fig. 15. The collected charge by reverse body bias on NMOS in the 65 nm FD-SOI structures.



(a) The BOX layer is 10 nm thick



(b) The BOX layer is 25 nm thick

Fig. 16. The collected charge by reverse body bias on NMOS in the 28 nm FD-SOI structures.

the SERs by the PHITS-TCAD simulations (Fig. 10) with reducing the supply voltage.

SERs decrease in response to an increase in the thickness of the BOX layer in 65-nm SOTB and 28-nm UTBB structures. The SERs of 65-nm SOTB decrease almost 20% when the supply voltage is at 0.4 V as shown in Fig. 10(a). In general, the occurrence of errors in UTBB structures are low and we observe only a 10% difference between the number of SERs occurring in the thin and thick BOX layer in 28-nm UTBB structure as shown in Fig. 10(b). It is because that only few errors occur in UTBB structure. As the sensitive volume of UTBB is much smaller than SOTB, the PBE becomes weaker in the 28-nm UTBB structure.

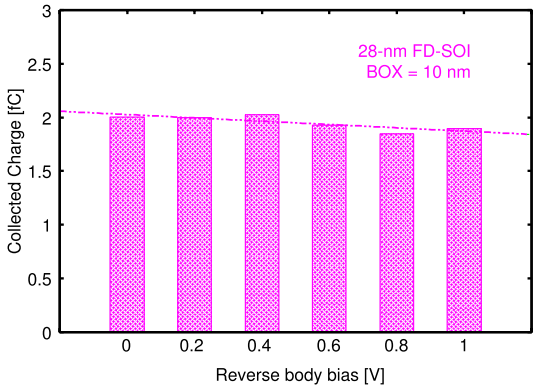
Fig. 11 shows the potential of BOX and SOI layer by a particle according to TCAD simulations. The maximum potential of 10nm BOX layer is 2.1 times higher than that of 100nm BOX layer. LET of the particle is 10 MeV-cm^2/mg. It influences the potential of SOI layer.

Fig. 12 and 13 shows the potentials of BOX and SOI layers by a particle hits in BOX layers of varying thickness in 65-nm and 28-nm SOI respectively. LET of the particle is 10 MeV-cm^2/mg. The BOX (SOI) potentials shown in Figures are average values of all region of BOX (SOI). In 65-nm SOI, the peak value of the BOX layer potential increases steeply, and it becomes difficult to return the SOI potential to 0 V when the BOX layer is much thicker. The electron-hole pairs generated in the substrate easily affects the potential of SOI layer when the BOX layer is thin. It becomes easier to turn on the parasitic bipolar transistor in the SOI layer. Thinner BOX layer in SOI weakens its tolerance for soft errors.

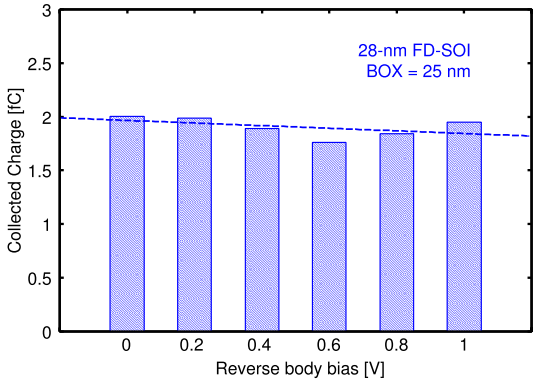
However, in 28-nm, the SOI and BOX layer potential do not increase over 0.6 V by particle hits. They are independent of variations in BOX thickness. Electron-hole pairs becomes harder to generate in 28-nm SOI due to its smaller sensitive volume and higher doping well. This causes the weakness of PBE.

C. Influence of Reverse Body Bias on Neutron-Induced SER

We applied reverse body bias with a LET of 15 MeV-cm^2/mg on the NMOS of the FD-SOI structures. Fig. 14 shows the current waveforms of NMOS in the 65-nm FD-SOI structures. When the BOX layer is 10 nm, the current pulse has two distinct parts: one caused by drift and the other caused by the PEB (Fig. 14(a)) This phenomenon is clearly visible in [7]. The first current pulse is very low because the drift mechanism is suppressed by the BOX layer. The PBE is the main factor of charge collection in the SOTB structure. When the reverse body bias increases in the SOTB structure, it suppresses the elevation of well potential after the particle hits. The PBE is suppressed, causing the second part to

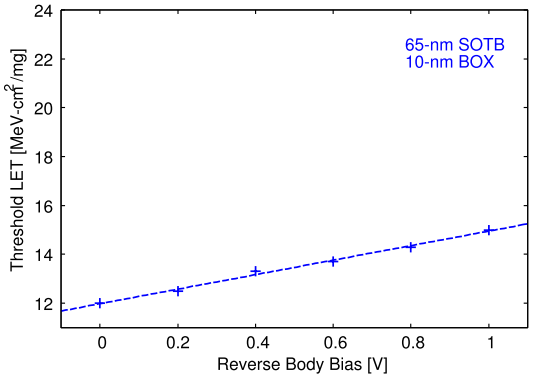


(a) The BOX layer is 10 nm thick

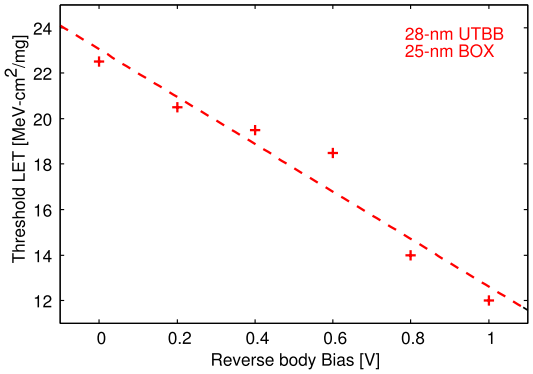


(b) The BOX layer is 25 nm thick

Fig. 17. The collected charge by reverse body bias on NMOS in the 28 nm FD-SOI structures.



(a) In the SOTB structure.



(b) In the UTBB structure.

Fig. 18. The threshold LET influenced by reverse bias on NMOS and PMOS of SOTB and UTBB structures.

decrease by increasing the reverse bias. However, there is no significant change in the pulse waves as shown in Fig. 14(b), when BOX layer thickness is increased to 25 nm.

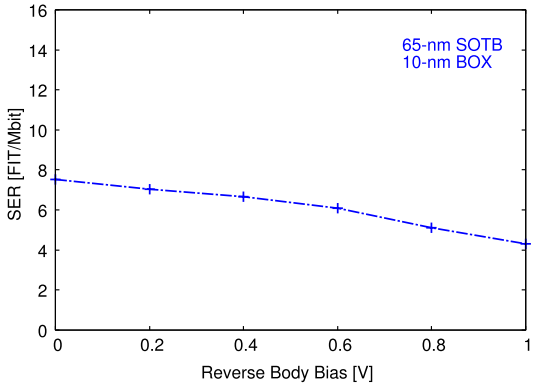
Fig. 15 shows the volume of collected charge of 65-nm FD-SOI structures. We calculated the collected charge by integrating current waveforms. When the BOX layer is 10 nm, the collected charge reduces by 45% when a 1.0 V reverse bias is applied to NMOS as shown in Fig. 15(a). However, the collected charge reduces by 26% as shown in Fig. 15(b), when the BOX layer is increased to 25 nm. This phenomenon occurs because the BOX layer thickens, it becomes increasingly difficult to increase the potential of SOI layer by reverse body bias.

In the 28-nm FD-SOI structure, current waves do not change significantly in BOX layers 10 and 25 nm thick (Fig. 16). Similarly current waveforms do not change significantly when reverse body bias is applied.

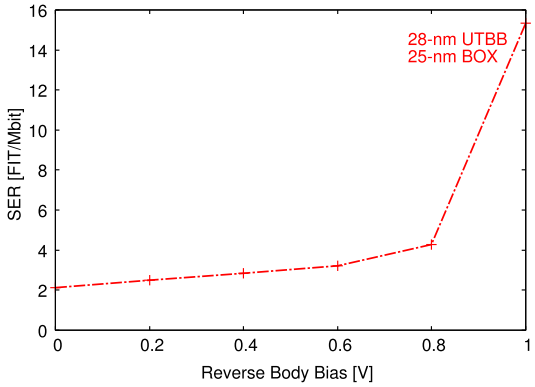
Fig. 17 shows the collected charge for the 28-nm FD-SOI when varying reverse body bias is applied. As can be seen, there is no change in the collected charge under reverse body bias because the sensitive layer volume in a 28-nm process becomes 15% of that in a 65-nm process. The PBE of SOI layer becomes weaker making it harder to turn on the parasitic bipolar transistor. On the other hand, reverse body bias widens the depletion region between N-well and P-well in latches, allowing more charge to be collected into P-well after the particle hit. Thus, there is no decrease in the collected charge.

Fig. 18 shows the change in threshold LETs (the smallest values of LET upsets latches) in response to increases in the reverse body bias on NMOS and PMOS of SOTB and UTBB. The threshold LETs in the SOTB structure increase under reverse body bias (Fig. 18(a)). The PBE become weaker when reverse body bias is applied and it become harder to flip the SOTB latch. However, the threshold LETs of the UTBB structure become lower when reverse body bias is applied on NMOS and PMOS (Fig. 18(b)). This is because the ON current of the transistor becomes lower when reverse body bias is applied making it easy to flip UTBB latches by particle hits. The degradation of performance by reverse body bias occurs in both SOTB and UTBB. However, the affection of PBE in SOTB is stronger than the degradation of performance therefore it causes a reduction in the collected charge.

Fig. 19 shows neutron induced SERs when body bias is applied in SOTB and UTBB structures using PHITS-TCAD simulations. The supply voltage is 1.0 V. In the SOTB structure, the SERs that undergo reverse body bias at 1.0 V reduce to almost half of that at 0 V bias as shown in Fig 19(a). In the UTBB structure, when reverse body bias is applied at 1.0 V SERs increase 8 times more than at 0 V as shown in Fig. 19(b). Transistor performance worsens in UTBB reverse when body bias is applied at high voltage, therefore the SERs increase significantly at 1.0 V. The SERs of 28-nm UTBB increase suddenly when the reverse body bias is 1.0 V. This sudden



(a) The SERs dependent on body bias in SOTB structure



(b) The SERs dependent on body bias in UTBB structure

Fig. 19. The SERs depending on body bias which calculated by PHITS-TCAD simulations.

increase occurs as a result of particles in which D_E exceeded the threshold E value during PHITS simulation.

IV. Conclusion

We analyzed alpha particle and neutron induced SERs in a 65-nm SOTB and a 28-nm UTBB structure using irradiation experiments and PHITS-TCAD Monte-Carlo based simulation. The alpha irradiation test revealed that in a SOTB structure the SEU cross-sections is six times larger at a supply voltage of 0.4 V than at 1.2 V. However, the SEU cross-section increased 2.5 times when supply voltage is reduced from 0.45 V to 0.4 V in the UTBB structure. The cross-sections of SOTB and UTBB are 1.33×10^{-11} cm^2/bit and 6.78×10^{-13} cm^2/bit respectively when the supply voltage is set at 0.4 V.

Results of the neutron irradiation test showed no errors in 28-nm UTBB. PHITS-TCAD simulation show that the soft error tolerance of 28-nm UTBB is at least twice as much as the 65-nm SOTB. The simulation results are also consistent with the neutron irradiation test results.

PHITS-TCAD simulation show that the SERs of 65-nm FD-SOI structure decreases 20% when BOX region thickness is increased from 10 nm to 25 nm. However, the SERs of 28-nm FD-SOI do not change significantly. By applying 1.0 V reverse bias, the SERs in the SOTB structure is reduced by half; however the SERs of UTBB multiplied by eight. Sensitive volume decreases in tandem with technology down-scaling making it more challenging to turn on the parasitic bipolar transistor in 28-nm UTBB structure than in 65-nm SOTB structure.

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