# A Radiation-Hardened Non-redundant Flip-Flop, Stacked Leveling Critical Charge Flip-Flop in a 65 nm Thin BOX FD-SOI Process

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***Abstract*—We propose SLCCFF which is a radiation hardened non-redundant flip-flop for an SOI process. The SLCCFF has the stacked structure to prevent soft errors on SOI processes while maintaining smaller delay and power overhead than conventional stacked FFs. Energy delay product of SLCCFF is 86% of the stacked FF. We fabricate test chip in a 65 nm thin BOX FD-SOI process and measured soft error rates of SLCCFF, stacked FF and standard DFF by neutron irradiation and $\alpha$ particles. Experimental results show that the SLCCFF is about 27x stronger than the standard DFF at 0.4V power supply in the SOTB process. It is about 1080x stronger compared with the standard DFF in the bulk process.**

***Index Terms*—single event effect, soft error, neutron irradiation, FD-SOI, flip-flop.**

## I. Introduction

Radiation-induced soft error is a significant concern for the medical devices, aerospace, and high-performance computers. For the supercomputers, continuous operation time is limited by the soft errors since over 700,000 cores are operated simultaneously [1]. Therefore, radiation-hardened designs are significant for the supercomputers and they need to satisfy high reliability and small overhead of circuit performances. To protect FFs from soft errors, several redundant circuits are proposed such as TMR [2], DICE [3], [4] and BISER [5], [6]. Redundant FFs achieve high soft error mitigation, while they have large power consumption and area overhead. In addition, multiple node charge collection becomes a crucial issue for redundant FFs to keep high soft error mitigation in 65 nm and advanced technology [7], [8], [9].

For the device level radiation-hardened technology, fully-depleted silicon on insulator (FD-SOI) transistors are used to reduce the soft-error-sensitive volume [10], [11]. FD-SOI transistors have buried oxide (BOX) layers are inserted under transistors. BOX layers can block charge collection by drift and funneling. Thus, radiation-induced current glitches on FD-SOI transistors are smaller than those on bulk transistors. However, FD-SOI process does not drastically improve soft error immunity [12], [13]. FD-SOI transistors with circuit mitigation design are required for high reliable LSIs.

In this paper, we proposed non-redundant FF based on the stacked inverter methodology [14]. We evaluate circuit performances on proposed and conventional FFs using circuit-level optimization. We also show the measurement results of the soft error rates on the proposed and conventional FFs by neutron irradiation and alpha-particles. Proposed FF achieves higher operation speed with equivalent soft error resilience compared with conventional stacked FF. This paper is organized as follows. Section II shows proposed circuit structure and comparison results of optimized energy-delay product. In Sect. III, we explain test chip structures fabricated in 65-nm FD-SOI and bulk process, and accelerated test setup for neutron and alpha particles. Accelerated test results are discussed in Sect. IV. In Sect. V, we conclude this paper.

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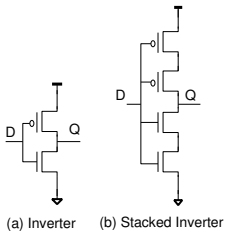


Fig. 1. Stacked inverter.

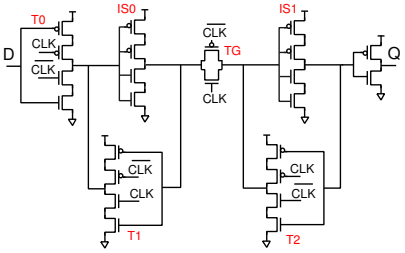


Fig. 2. Conventional stacked FF.

## II. The proposed Circuit Structure and Circuit Performance Optimization

In this section, we explain the detailed structure of the proposed non-redundant FFs and evaluate its delay time and energy consumption from circuit-level simulation.

### A. Radiation-hardened Structure for FD-SOI Process

Fig. 1 shows a stacked inverter which becomes much stronger to soft errors in a FD-SOI process [15]. It is because these stacked FD-SOI transistors are fully separated by shallow trench isolation (STI) and BOX layers. Neither parasitic bipolar action nor charge sharing happens simultaneously among these stacked transistors. In contrast, the stacked inverter in a bulk process does not improve soft error resilience drastically. It is because the charge collection due to drift and funneling is dominant effect for bulk transistors.

Fig. 2 shows a conventional stacked FF which is a transmission-gate D-type flip-flop (DFF) with stacked methodology [15]. The stacked FF has stacked inverters (IS0 and IS1) in the master and slave latches to reduce SEU rate in a FD-SOI process. It can achieve high soft error immunity with

TABLE I
ENERGY, DELAY AND AREA COMPARISON. ALL VALUES ARE NORMALIZED TO THOSE OF DFF.

| | Energy | Delay | Area |
|---|---|---|---|
| DFF | 1.00 | 1.00 | 1.00 |
| SLCCFF | 1.89 | 1.67 | 1.24 |
| Stacked FF | 2.13 | 2.00 | 1.12 |

small area and power overhead compared with redundant FFs. However, the delay time of stacked FF is greater than standard FF since gate capacitance and output resistance of the stacked inverter are twice as big as those of the inverter.

### *B. Proposed Radiation-hardened Structure*

Fig. 3 shows the proposed FF structure named Stacked Leveling Critical Charge Flip-Flop (SLCCFF). The difference between the SLCCFF and the stacked FF is the connection between the stacked inverter (IS0) and the transmission gate (TG). In the SLCCFF, PMOS and NMOS transistors in TG are connected to the intermediate nodes (p and n) instead of the output node (c). In this connection, the stacked inverter IS1 is charged or discharged through two PMOS transistors or two NMOS transistors. Fig. 4 shows simulation waveforms when clock signal is changed to '1'. 20% - 80% rise transition time of the gate voltage on IS1 in the SLCCFF is changed 1.6x more quickly than that in the stacked FF. Therefore, the SLCCFF can achieve smaller Clock-to-Q delay time than the stacked FF. While, SLCCFF keeps equivalent soft error hardness to stacked FF. When a particle is incident on the lower NMOS transistor of IS0, node n can be flipped. However, its flip does not affect node c. It is because that the upper NMOS transistors of IS0 keeps OFF state, and node p can not be flipped by radiation-induced glitch propagated through PMOS and NMOS transistors in TG. The drawback of the SLCCFF is increase of the area overhead since the diffusion of TG and IS0 must be separated.

In order to compare circuit performance, we optimize D-to-Q delay time of the SLCCFF and the stacked FF by the downhill simplex method [16]. In our optimization, transistor sizes of output inverter are fixed to standard inverter size and the transistor sizes of other NMOS transistors are changed separately to minimize ED (Energy Delay) product. While, PMOS transistors keeps p/n ratio with those of NMOS transistors. In circuit level simulation, supply voltage is set to 1.2V and data activity is 10%. The diffusion capacitance is included in our optimization.

Table I shows optimized rise delay and energy of the DFF, stacked FF and SLCCFF calculated from circuit-level simulation. The area of the SLCCFF is 1.1x bigger than that of the stacked FF. However, the delay and the energy of the SLCCFF are 16% and 11% smaller than those of the stacked FF, respectively.

### *C. Structure-modified SLCCFF*

In the previous section, we show the structures of the stacked FF and SLCCFF based on the transmission-gate FF (TG-FF) since TG-FF has the smallest ED product. However,

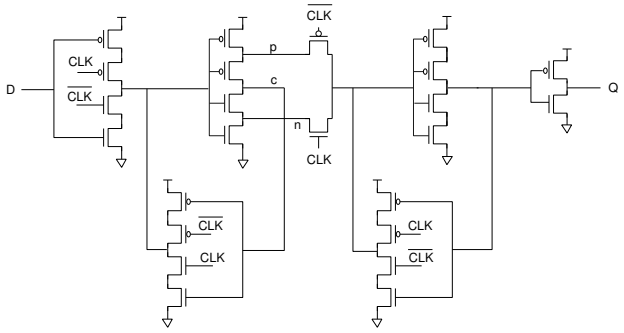


Fig. 3. Proposed circuit structure named stacked leveling critical charge flip-flop (SLCCFF).

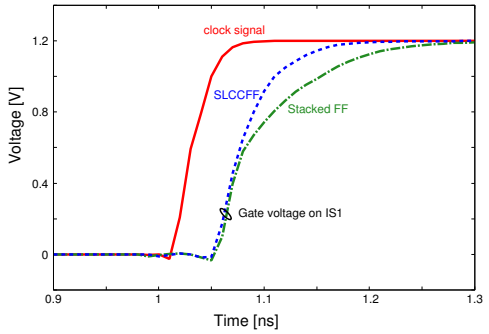


Fig. 4. Simulation waveforms of gate voltage on IS1 when clock signal is changed to '1'.

TG-FF based structures are not suitable for stacked ones since the stacked inverter IS1 is connected to the output inverter. In this section, we discuss structures of the stacked FF and SLCCFF based on the C2MOS FF [17].

Fig. 5 shows SLCCFF based on C2MOS FF in which structure of the slave latch is modified to enhance operating speed. In this structure, load capacitance of TG and IS0 can be reduced since an additional small inverter is inserted before the large output inverter and IS1 can be changed to minimum transistor sizes. The conventional stacked FF are also enhanced by changing the structure of the slave latch. Fig. 6 shows the modified stacked FF which is the fastest stack-based structure except for modified SLCCFF in our simulation results. TG is replaced tristate inverter and connections of the stacked inverters are changed in the same way as shown in Fig. 5.

Modified stacked FF and SLCCFF are also optimized by downhill simplex method. Fig. 7 and Table II shows optimization results. Compared with the stacked FF and SLCCFF in Fig. 2 and Fig. 3, delay and energy overheads of modified stacked FF and SLCCFF are reduced. The modified SLCCFF achieves smaller delay time and energy consumption than the stacked FF. The ED product of the modified SLCCFF is 86% of the modified stacked FF

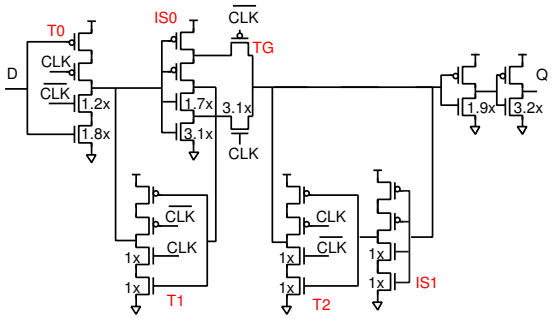


Fig. 5. Modified SLCCFF.

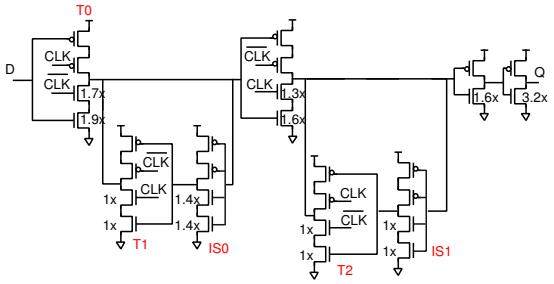


Fig. 6. Modified stacked FF.

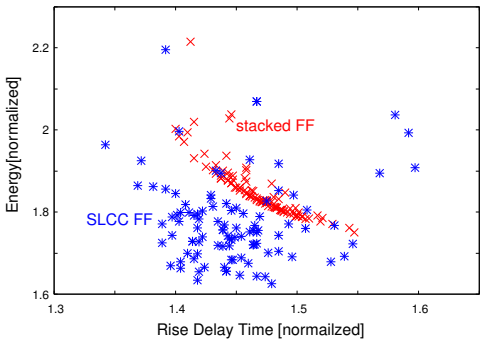


Fig. 7. Optimization results of modified stacked FF and SLCCFF as shown in Fig. 6 and Fig. 5. Energy and Delay values are normalized to those of DFF.

## III. Accelerated Test Setup by Spallation Neutron Beam and $\alpha$ Particles

### A. Test Chip Structure

In order to measure soft error rate by accelerated tests, test chips are fabricated in 65-nm bulk process and thin BOX FD-SOI processes which is named silicon-on-thin-BOX (SOTB) [18]. As shown in Fig. 9, the thicknesses of the BOX layer and body layer are 10 and 12 nm, respectively. Fig. 8 shows a test chip micrograph with a floorplan. The layout designs of the test chips are strictly identical between SOTB and bulk

TABLE II
Energy, Delay, EDP, and Area of modified stacked FF and SLCCFF. All values are normalized to those of DFF.

| | Energy | Delay | EDP | Area |
|---|---|---|---|---|
| SLCCFF in Fig. 5 | 1.67 | 1.41 | 2.33 | 1.29 |
| Stacked FF in Fig. 6 | 1.83 | 1.47 | 2.69 | 1.35 |

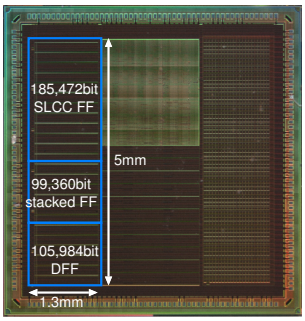


Fig. 8. Chip micrograph and floorplan.

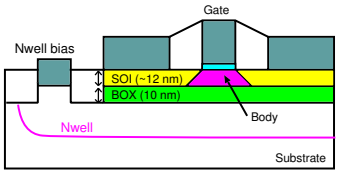


Fig. 9. Transistor structure in the SOTB process.

processes except for BOX layers, while the channel impurity concentrations and threshold voltage of the SOTB transistors are lower than those of the bulk transistors [19]. Test chip has triple-well structure and well-contacts were inserted every 104 $\mu$m. The FF-array part of a test chip is 1.3 mm $\times$ 5.0 mm and contains 105,984 bit of DFFs, 99,360 bit of the unmodified stacked FFs and 185,472 bit of the unmodified SLCCFFs whose structures are shown in Fig. 2 and Fig. 3, respectively. In the test chip, we implement non-optimized stacked FFs and SLCCFFs as shown in Fig. 2 and Fig. 3. In addition, transistor sizes are not optimized in fabricated stacked FFs and SLCCFFs. It is because soft error rate (SER) may be changed by transistor sizes and we focus on the difference of SERs caused by the connection between stacked inverter and transmission gate. All FFs are connected in series to form a shift register.

### B. Experimental Setup

Accelerated tests by spallation neutron beam were performed at the research center for nuclear physics (RCNP), Osaka University [20]. Fig. 10 shows the neutron beam spectrum in comparison with the terrestrial neutron spectrum at the ground level of New York. The average accelerated factor is about $2.9 \times 10^8$. Fig. 11 shows the test setup of the neutron irradiation. In order to increase the number of errors in the limited measurement time, 16 test chips are measured simultaneously.

Soft error rates induced by $\alpha$-particle are measured by a 3M Bq $^{241}\mathrm{A_m}$ source. Fig. 12 shows the test setup of the $\alpha$-particle irradiation. The distance between the $\alpha$ source and the DUT is 0.7 mm. We measured soft error rates when master latches in FFs are hold state (clock signal, CLK is "1"). It is because beam time is limited and the slave latches in stacked FF and SLCCFF have the same structure as shown in Fig. 2 and Fig. 3. Therefore, we only changed stored values (Q) and supply voltage in this measurement.

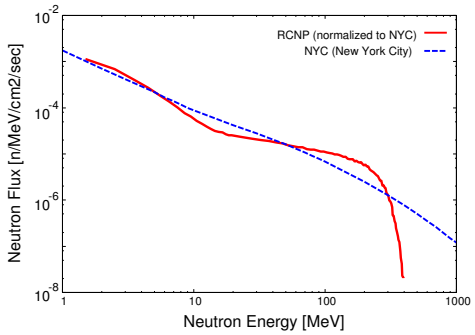


Fig. 10. Energy spectrum of spallation neutron beam normalized to that at the ground level of NYC.

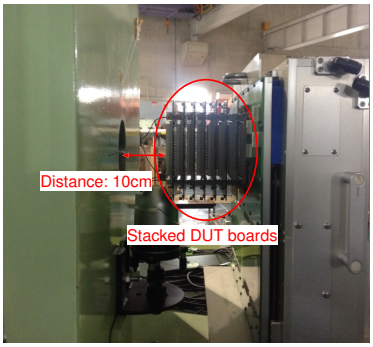


Fig. 11. Radiation test by the spallation neutron beam.

Fig. 13 shows the NMOS transistor which causes a soft error. when Q = "0", the NMOS transistor $N_{\mathrm{T1}}$ and $N_{\mathrm{T1-b}}$ in the tristate inverter is vulnerable to particle hits. In contrast, when Q = "1", the NMOS transistors, $N_{\mathrm{S0}}$ and $N_{\mathrm{S0-b}}$ in the inverter is vulnerable. We assume that NMOS transistors are more vulnerable to particle hits than PMOS transistors [21].

## IV. Evaluation Results of Soft Error Rate induced by Spallation Neutron and $\alpha$-Particle Irradiation

### A. Measurement Results by Spallation Neutron Irradiation

Fig. 14 and Fig. 15 show the measurement results of neutron-induced SERs in the SOTB process when Q = 0 and 1, respectively. SERs of the stacked FF and the SLCCFF are

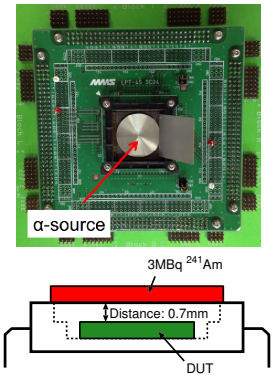


Fig. 12. Radiation test by $\alpha$-particle irradiation.

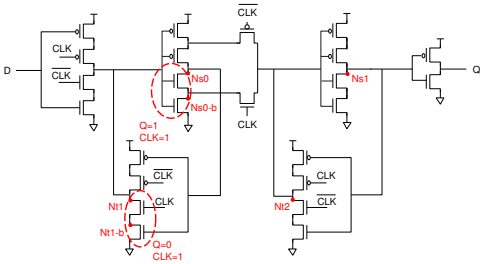


Fig. 13. The NMOS transistors which is vulnerable to a soft error with labeled condition.

smaller than the conventional DFF and they achieve less than 3 FIT/Mbit in all supply voltages when Q = 1. Especially, soft error tolerances of the stacked FF and the SLCCFF are 27x higher than than that of the DFF at 0.4 V. Compared with the stacked FF, the SLCCFF exhibits almost same SERs at any supply voltages and states since the differences of SERs are within error bars. Therefore, the proposed structure does not reduce soft error resilience of stacked scheme and SLCCFF achieves smaller soft error rates than DFF with smaller EDP overhead than the stacked FF. However, the error tolerances of the stacked FF and the SLCCFF may not be sufficiently high when Q = 0 and NMOS transistors of the tristate inverter are vulnerable to soft errors. We assume that they become more robust to soft errors by stacking the tristate inverters, which increases area, delay and power overhead.

In our measurement results, SERs on the DFFs are relatively high at 1.0 V. We assume that the parasitic bipolar effect is suppressed when supply voltage is less than 0.8 V, while critical charge is linearly decreased when the supply voltage is reduced. As a result, SER at 1.0V is bigger than that at 0.8 V and 1.2 V.

Fig. 16 and Fig. 17 show the neutron-induced SERs in the bulk process when Q = 0 and 1, respectively. All FFs have similar soft error rates at every supply voltage. It is because that stacked scheme have no resilience to soft errors in the bulk process. We assume the difference of soft error rate between DFF and stack based FFs is caused by gate capacitance increment.

### B. $\alpha$-Particle Irradiation Test

Fig. 18 – 21 show the measurement results of $\alpha$-particle-induced soft error rates in the SOTB process. Y-axes show error probability with a logarithmic scale. The error probability is calculated from the number of fabricated FFs and the number of FFs flipped by $\alpha$ particle irradiation for the 60 second. Regardless of the (Q, CLK) state, the error probabilities of the stacked FF and the SLCCFF are much smaller than the DFF. When (Q, CLK) = (1, 1) and (1, 0), the error probabilities of the SLCCFF are almost same as that of the stacked FF at low supply voltage. Especially, the error probabilities of the stacked FF and the SLCCFF are less than 1/100 compared with the conventional DFF at 0.4 V. This results are consist with the our neutron results.

In contrast, when (Q, CLK) = (0, 1), the SLCCFF has the smallest SER at any supply voltage, which is not observed in

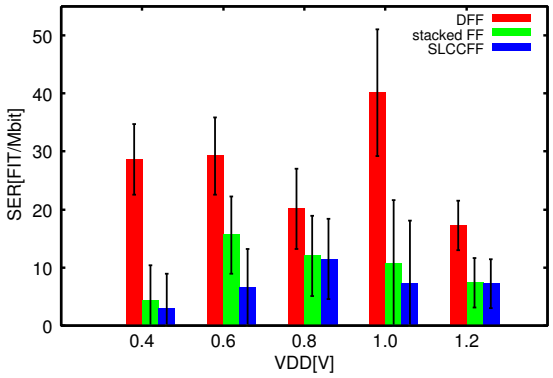


Fig. 14. Measurement results by neutron irradiation in the SOTB process when (Q, CLK)=(0, 1).

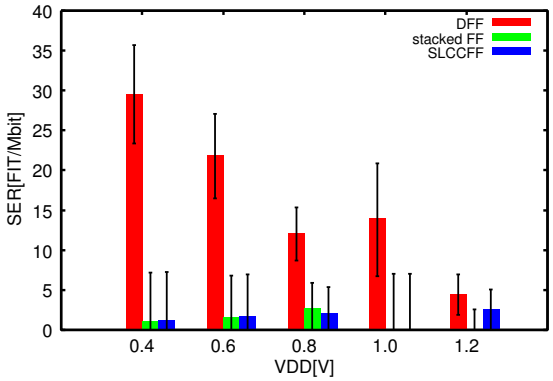


Fig. 15. Measurement results by neutron irradiation in the SOTB process when (Q, CLK)=(1, 1).

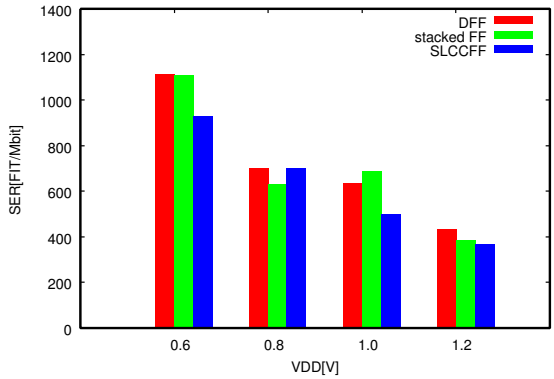


Fig. 16. Measurement results by neutron irradiation in the bulk process when (Q, CLK)=(0, 1).

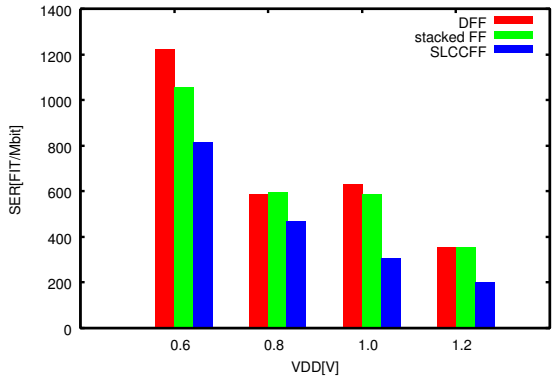


Fig. 17. Measurement results by neutron irradiation in the bulk process when (Q, CLK)=(1, 1).

neutron-induced SER. When (Q, CLK)=(0, 1), it is conceivable that the NMOS transistor $N_{T1}$ in the tristate inverter causes a soft error. However, the circuit structure of the tristate inverter is equivalent between the stacked FF and the SLCCFF. To evaluate soft error rate, we calculate a critical charge of the NMOS transistor $N_{T1}$ using single exponential current source [22]. A single exponential current source attached to the NMOS transistor $N_{T1}$. SPICE simulation results show the critical charge of the stacked FF and SLCCFF are 1.4 fC and 1.0 fC at 0.4V, respectively. As a result, the cause of the difference in the soft error tolerance between stacked FF and SLCCFF when (Q, CLK)=(0, 1) does not observed in circuit-level simulation. We assume that the difference of SER might be caused by the difference of the layout structure between the stacked FF and the SLCCFF. Fig. 22 shows the layout structures of the stacked inverter IS0 and transmission gate TG in the stacked FF and the SLCCFF. In the SLCCFF, transmission gate is separated from the stacked inverter. We assume that charge collection to multiple nodes can be reduced in the SLCCFF. In addition, STI stress and transistor variation may increase and transistor performances are slightly changed. The difference of SERs between the stacked FF and the SLCCFF are clearly observed in alpha tests.

Fig. 23 and Fig. 24 shows the $\alpha$-particle-induced SERs in the bulk process. Y-axes show error probability with a linear scale. In the bulk process, $\alpha$ particle results show the same dependence as neutron results in any stored values.

TABLE III
AVERAGE SERS OF THE DFF, THE STACKED FF AND THE SLCCFF INDUCED BY NEUTRON AND $\alpha$ PARTICLES IN THE 65 NM SOTB PROCESS. SERS ARE NORMALIZED BY THOSE OF THE DFF AT 1.2V.

| | 1.2V | | 0.4V | |
|---|---|---|---|---|
| | neutron | $\alpha$ particles | neutron | $\alpha$ particles |
| DFF | 1.00 | 1.00 | 2.7 | 31 |
| Stacked FF | 0.34 | 0.026 | 0.25 | 0.37 |
| SLCCFF | 0.45 | 0.008 | 0.19 | 0.019 |

### C. Soft Error Rate Comparison

Table III shows the average values of soft error rate when Q = 0 and 1 in the 65 nm SOTB process. When supply voltage is 1.2V, neutron-induced SER is not drastically decreased by the stacked FFs. In contrast, neutron-induced SER is reduced to 9.2% (0.25 / 2.7) when supply voltage is 0.4V. Thus, the SLCCFF and the stacked FF are used for sub-threshold operation at the ground level. On the other hand, $\alpha$-particle-induced SERs of the stacked FF and the SLCCFF are $\sim$3% of SERs of standard DFF at any supply voltage. The SLCCFF have strong mitigation against lower LET radiation.

## V. Conclusion

We propose non-redundant radiation hardened FF named SLCCFF resilient to soft errors in the FD-SOI process for lower energy consumption and smaller delay than the conventional stacked FF. The delay-energy product of the modified

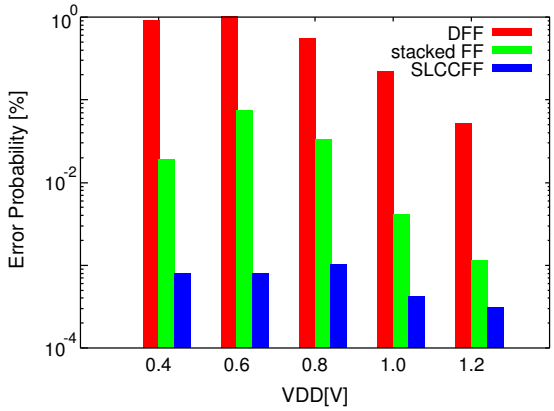


Fig. 18. Measurement results by $\alpha$-particle in the SOTB process when (Q, CLK)=(0, 1).

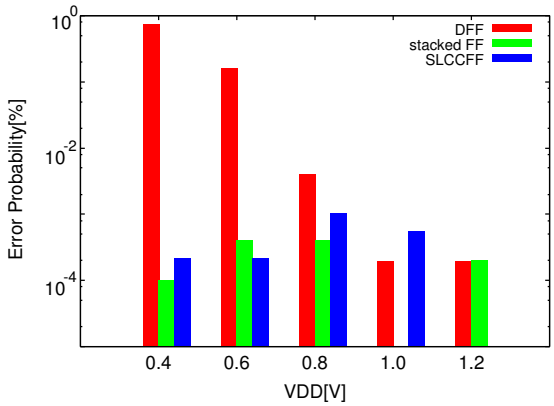


Fig. 19. Measurement results by $\alpha$-particle in the SOTB process when (Q, CLK)=(1, 1).

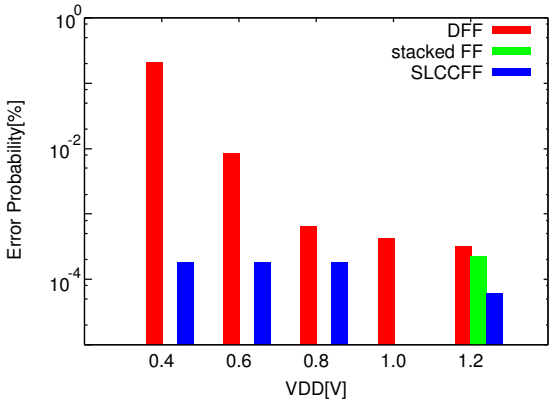


Fig. 20. Measurement results by $\alpha$-particle in the SOTB process when (Q, CLK)=(0, 0).

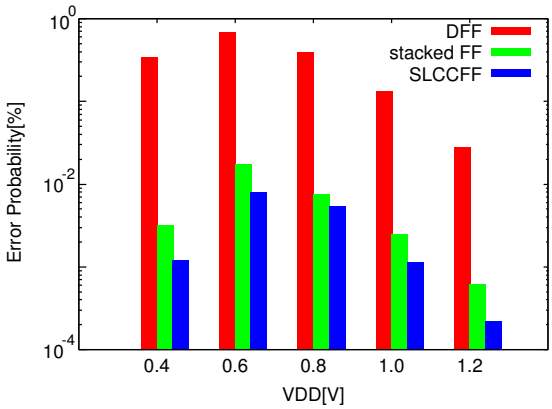


Fig. 21. Measurement results by $\alpha$-particle in the SOTB process when (Q, CLK)=(1, 0).

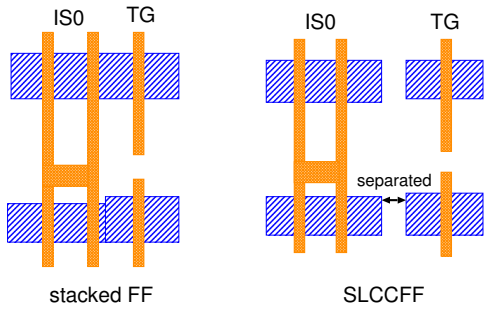


Fig. 22. Layout structures of stacked inverter IS0 and transmission gate TG in the stacked FF and the SLCCFF. IS0 and TG are separated in the SLCCFF.

SLCCFF are 14% smaller than those of the modified stacked FF which is a non-redundant FF.

We also show accelerated test results on the stacked FF and the SLCCFF which are not optimized in order to focus on the difference of SERs due to the connection between stacked inverter and transmission gate. From the spallation neutron irradiation, the SER of the unmodified SLCCFF is 1/27 of the conventional DFF on the 65 nm FD-SOI process. The unmodified SLCCFF achieve equivalent soft error mitigation to the unmodified stacked FF. In addition, from $\alpha$-particle irradiation test, the error probability of the unmodified SLCCFF is less than 1/100 compared with conventional DFF in the SOTB process.

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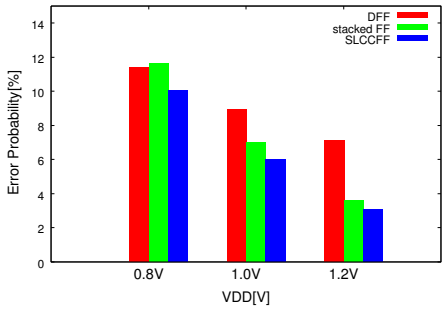


Fig. 23. Measurement results by $\alpha$-particle in the bulk process when (Q, CLK)=(0, 1).

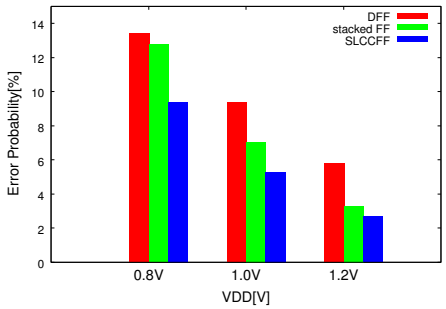


Fig. 24. Measurement results by $\alpha$-particle in the bulk process when (Q, CLK)=(1, 1).


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