Dependence of Cell Distance and Well-Contact Density on MCU Rates by Device Simulations and Neutron Experiments in a 65-nm Bulk Process

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***Abstract*—Technology scaling increases the role of charge sharing and bipolar effect with respect to multiple cell upset. We analyze the contributions of cell distance and well-contact density to suppress MCU by device-level simulations and neutron experiments. Device simulation results reveal that the ratio of MCU to SEU exponentially decreases by increasing the distance between redundant latches. MCU is suppressed when well contacts are placed between redundant latches. Experimental results also show that the ratio of MCU to SEU exponentially decreases by increasing the distance between cells. MCU is suppressed effectively by increasing the density of well contacts.**

***Index Terms*—Device-stimulation, MCU, neutron irradiation, parasitic bipolar effect, soft error.**

I. Introduction

RADIATION induced charge collection at a single sensitive node, such as the drain region of a single transistor, is a possible source of SEU. Radiation-hardened circuits, for instance Triple Modular Redundancy (TMR), Built-in Soft Error Resilience (BISER)[1], Dual Interlocked Storage Cell (DICE)[2], and Error Correction Code (ECC) have been employed to mitigate an SEU. As device dimensions are scaled down, multiple node charge collection has an increasing impact on the response of the circuit [3]. Soft errors have become an increasingly troublesome issue for memories as well as sequential logic circuits.

Recently, the charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. Not only the charge sharing, also the bipolar effect become dominant when a particle hit on latches or flip-flops. It makes radiation-hardened circuit more sensitive to Multiple Cell Upsets (MCUs) [4].

MCU rate depends on cell distance and well-contact density. In order to reduce radiation-induced multiple errors, each vulnerable transistor is placed on different p-well regions or separated over 1.1 μm [5], [6]. The parasitic bipolar effect and the charge sharing also affect SEU [7] and Single Event Transient (SET) pulse widths [8]. Several device simulations results show that charge sharing can be suppressed by high well contact density, or separating the distance between transistors in 130 nm process [9], [10] and 90 nm process [11]. However, the experiments results of these references do not show the relationship between soft error rates and the distance between transistors clearly. The results of 65 nm prcess has not been presented either. To estimate soft-error rates and increase its resilience, it is necessary to measure characteristics of radiation-induced multiple cell upset.

In this paper, we analyze the impact of cell distance and well-contact density on redundant flip-flops by device-level simulations [12] and neutron experiments [13]. All device-level models are constructed in a 65-nm process. Test chips are fabricated in a 65-nm bulk CMOS process and accelerated tests are carried out at Research Center for Nuclear Physics (RCNP).

This paper is organized as follows. Section II shows the impact of cell distance and well-contact density on redundant latches in device-level by device-level simulations. The results by neutron experiments are shown in Section III. We compare the simulations and experimental results in Section IV. Section V concludes this paper.

II. Impact of Cell Distance and Well-contact Density by Device-level simulations

A. Device-Level Simulation Setup

In order to analyze the MCU tolerance of redundant latches, we examined several device-simulations by using the circuit as shown in Fig. 1. The circuit including two unconnected independent latches placed in two adjacent rows in a 65 nm bulk technology which is called redundant latches. The redundant latches are regarded as two latches in a TMR structure. A device simulator Sentaurus from Synopsys is used to do all device-level simulations. We assume that a radiation particle hits the tristate inverter T0 of the NMOS transistor of latch L0 in the odd row. The tristate inverter T1 can also be flipped by charge sharing and bipolar effect between T0 and T1. The layout structure of the redundant latches in two rows is shown in Fig. 2. All of the NMOS transistors are placed in the same P-well. Well contacts are placed side by side in the same well. The output nodes (N_{T0}, N_{T1}) of the tristate inverters T0 and T1 are initially set to "1". Output voltage of the tri-satate inverter is decreased by particle

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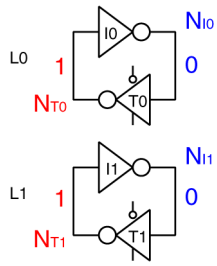

Fig. 1. Redundant latches Two unconnected independent latches).

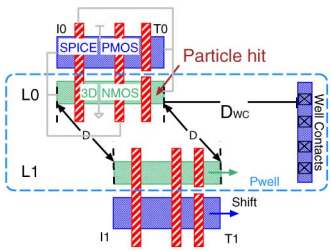

Fig. 2. Layout of two latches in two rows.

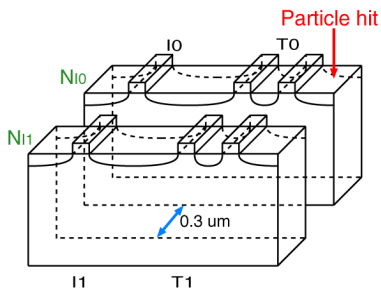

Fig. 3. 3D device-level structure of redundant latches in two rows. A particle hit at the tristate inverter T0.

hits on the NMOS of the tristate inverter. The redundant latches are simultaneously flipped by charge sharing and bipolar effect.

Based on the circuit and layout structures, we construct a 3D device-level NMOS model as shown in Fig. 3. This 3D NMOS model is constructed in a triple well structure. The distance between the well contacts and latches is defined as D_{WC}. D is the distance between redundant latches L0 and L1. D is 0.3 μm when the redundant latches are aligned vertically as shown in Fig. 3. A Gaussian heavy-ion model is used in device simulations. The ion hits T0 at 0.1 ns from the beginning of simulation.

B. Contribution of Cell Distance D to Suppress MCU

Fig. 4 shows the magnitude of collected charge of L0 and L1 when D is increased. D_{WC} is 20 μm. LET values of the ion particle are 10 and 20 MeV $\cdot$ cm^2/mg. The collected charge of L0 increases gradually while the collected charge of L1 decreases by increasing D as shown in Fig. 4. Less charge is collected into L1 as a function of D, for a given LET. Therefore, the charge sharing become weak between redundant latches by longer D. The collected charge of L0 become dominant. It is because less charge is shared by L1.

Fig. 5 shows the drain current of tristate inverters T0 and T1 when the redundant latches are simultaneously flipped. D_{WC} is 20 μm. D is 0.5, 3.0 and 5.0 μm. The waveform of T0 can be

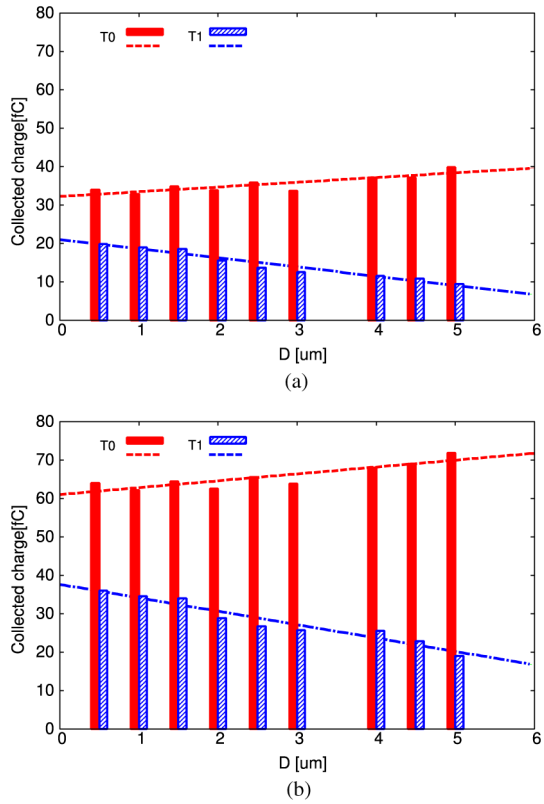

Fig. 4. Collected charge to L0 and L1 by increasing D. $D_{\mathrm{WC}} = 20$ μm. (a) LES $= 10$ MeV $\cdot$ cm^2/mg (b) LES $= 20$ MeV $\cdot$ cm^2/mg.

divided to two parts as shown in Fig. 5(a). The first part is very steep, that can be modeled by a single or double exponential model, while the second part is shallow. From the simulation results, we can obviously recognize that there are two mechanisms that occur in the whole charge collection. After the particle hit, a large amount of electrons are collected in the drain region immediately. The first part appears as a steep current by the drift. After that, holes still remain in the bulk region, which reduces the source-well potential barrier due to the increase in the potential of the P-well. The source injects electrons into the channel which can be collected at the drain. This effect is called the parasitic bipolar effect because the source-well-drain of NMOS transistor acts as an n-p-n bipolar transistor. The shallow current waveform in the latter part is caused by the parasitic bipolar effect.

As D is increased from 0.5um to 5.0 um, the first parts do not change a lot while the shallow parts become wider as shown in Fig 5(a). Fig. 5(b) shows the current waveforms of T1. The slopes are decreasing by increasing D. The current waveforms do not go to peak volume immediately. The charge cloud by particle hit is large. The charge is both collected into L0 and L1 at the same time by drift if L0 and L1 are too close. It makes the current waveform of L1 increase to the peak volume immediately. The charge collection of L1 by drift becomes weaker if D is increased. However, the waveforms become wider. The current waveforms of L1 is less $\mathrm{d}q/\mathrm{d}t$ because of the charge collected into L1 mainly by parasitic bipolar effect. Thus, redundant latches simultaneously flip easier by charge sharing than bipolar effect in 65 nm process.

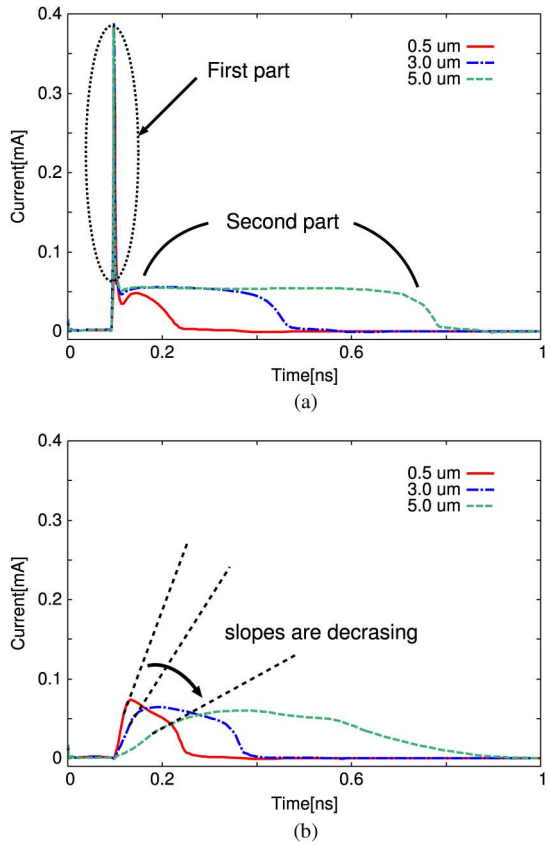

Fig. 5. Transient drain current of T0 (a) and T1 (b) caused by a particle hit at T0 when the redundant latches are simultaneously flipped. D is 0.5, 3.0, 5.0 μm. (a) Drain current waveform of T0 (b) Drain current waveform of T1.

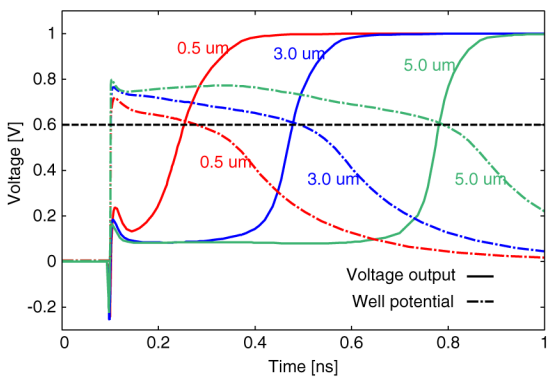

Fig. 6. Voltage outputs of inverter I0 of latch L0 and the well potential under the latch L0 after a particle. D is 0.5, 3.0, 5.0 μm.

Fig. 6 shows the voltage waveforms of inverter I0 of latch L0 and the well potential under L0 after a particle hit on the tristate inverter T0. D is 0.5, 3.0 and 5.0 μm. The voltage waveforms keep low when the well potential is higher than 0.6 V. The voltage waveforms start to go up when well potential decreases below 0.6 V. The flipped voltage waveforms cross the well potential waveforms at 0.6 V. It is because the parasitic bipolar transistor of latch L0 can not turn off until the well potential decreases below 0.6 V.

Fig. 7 shows the minimum magnitude of critical charge of the latches L0 and L1 when the redundant latches are simultaneously flipped. We call this charge as threshold charge. The

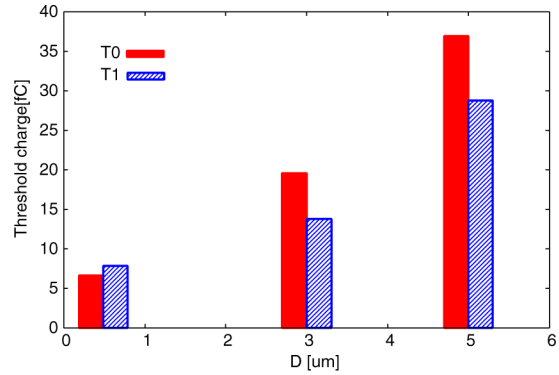

Fig. 7. Threshold charge of L0 and L1 when the redundant latches are simultaneously flipped. D is 0.5, 3.0, 0.5 μm.

magnitude of threshold charge becomes bigger when D is increased. As D is increased, charge sharing between L0 and L1 becomes weaker as shown in Fig. 5. Charge is mainly collected into L1 by the bipolar effect. However, it becomes harder to elevate the well potential under L1 because the latch L1 is placed far away from L0 ($D \gg 0.3$ μm). Thus, LET of the ion particle which simultaneously flips the redundant latches becomes higher. Threshold charge are increased in L0 and L1 by increasing D. Note that just the collected charge of tristate inverter T0 and T1 is shown in Fig. 7. Larger amount of charge is also collected into inverter I0 and I1. Thus, the charge of T1 is larger than T0 when D is 0.5 um. But it does not influence the results of the device simulations.

C. Contribution of Well-contact Position to Suppress MCU

In order to analyze the relationship between well-contact position and MCU tolerance, we place the well contacts adjacent to latches, D_{WC} is shorten to 1.0 μm from 20 μm. LET of the ion particle are 10 and 20 MeV $\cdot$ cm^2/mg. The redundant latches are aligned vertically ($D = 0.3$ μm) in these simulations. The volume of collected charge of L0 and L1 are shown in Fig. 8. When the distance D_{WC} is shorten from 20 μm to 1.0 μm, the magnitude of collected charge of the redundant latches L0 and L1 decreases by 50%. It is because the well potential under latches keeps steady by placing well contacts close to the latches. Bipolar effect under L0 and L1 is suppressed. Thus, less charge is collected into the redundant latches.

Fig. 9 shows the threshold charge of L0 influenced by D_{WC}, when redundant latches are simultaneously flipped. D is 1.0, 2.0 and 3.0 μm. The threshold charge exponentially decreases by increasing D_{WC}. There is a large amount of charge collected into the latch L0 when redundant latches are simultaneously flipped if the well contacts are placed adjacent to redundant latches. It is because the adjacent well contacts stabilize the well potential. The bipolar effect is also suppressed. Higher LET ion particle can are simultaneously flipped the redundant latches. Therefore, MCU tolerance of the redundant latches become stronger by shortened D_{WC}.

When the well contacts are placed between the redundant latches L0 and L1 as shown in Fig. 10, the magnitude of collected charge is shown in Fig. 11. the collected charge of L0 and L1 decreases by about 60% and 90% respectively compared

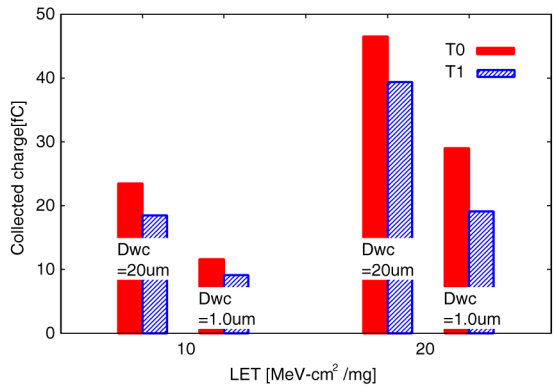

Fig. 8. Collected charge of the redundant latches L0 and L1 influenced by D_{WC}. LET is 10 and 20 MeV $\cdot$ cm^2/mg.

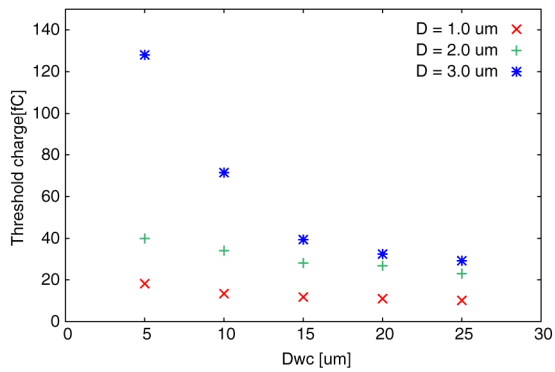

Fig. 9. Threshold charge of L0 by increasing D_{WC} when redundant latches are simultaneously flipped.

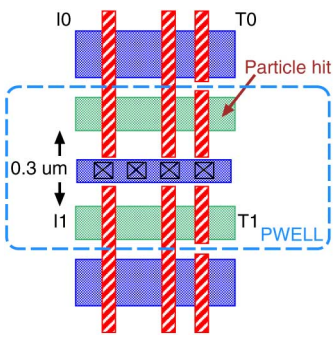

Fig. 10. The layout structure in which well contacts are placed between the redundant latches.

to the collected charge when D_{WC} is 20 μm, even if the redundant latches are aligned vertically. In this case, generated charge under the latch L0 can not cross over the well contacts to the L1 side. Thus the charge sharing between the redundant latches is almost prevented. Also the bipolar effect is suppressed effectively, because the well contacts between the redundant latches suppress the well potential elevation.

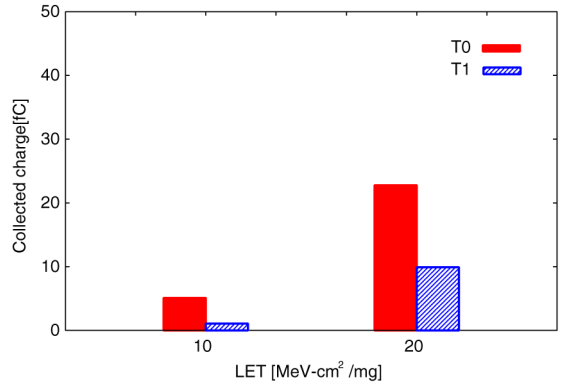

Fig. 11. Collected charge of L0 and L1 when the well contacts are placed between the redundant latches.

TABLE I
PARAMETERS FOR SER ESTIMATION

F (n·cm^{-2}s^{-1})	5.65×10^{-3}
Q_s (fC)	5.72
K	2.2×10^{-5}

D. Soft Error Rate Calculation

Eq. (1) [14] is used to calculate SER in FIT (Failure In Time, number of errors/10^9 hours).

$$N_{\mathrm{SER}}(Q_{\mathrm{crit}}) = F \times A \times K \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_s}\right) \quad (1)$$

where F is the high-energy neutron flux and A is the drain area of transistors related to soft errors. K is a fitting parameter. Q_s is called "charge collection efficiency" that strongly depends on doping and supply voltage [15]. We use the parameter values as in Table I. We use a fitting line to scaled Q_s based on the Q_s of 350 nm and 100 nm as [14] to 65 nm.

MCU rate is calculated by the threshold (minimum) charge of latch L0 at which the redundant latches are simultaneously flipped. D_{WC} is the distance between the redundant latches and well contacts as in Fig. 2. The distances between redundant latches D which we use for device simulations are shown in Table II. D_{WC} is 20 μm. The threshold charge Q_{crit} and the ratios of MCU to SEU are also shown in Table II. Fig. 12 shows the ratio of MCU to SEU influenced by D on redundant latches from device simulations when D_{WC} is 20 μm. Note that the ratio of MCU to SEU which is lower than 0.1% are not shown on Fig. 12. According to the device-simulation results as shown in Table II, the ratio of MCU to SEU exponentially decreases by increasing D. If the well contacts are placed between redundant latches, they are simultaneously flipped when LET is 35 MeV $\cdot$ cm^2/mg, and the threshold charge is 45.7 fC. The ratio of MCU to SEU decreases to 0.073%.

III. Impact of Cell Distance and Well-Contact Density on Redundant FFs by Neutron Experiments

The experimental results of neutron-induced MCU on D-FFs are described in this section. We use four different shift registers

TABLE II
QCRIT AND THE RATIO OF MCU TO SEU BY DEVICE SIMULATIONS WHEN D_{WC} IS 20 μm

D	Q_{crit}	MCU/SEU [%]
0.5	8.31	50.18
0.6	9.95	37.70
1.0	11.3	29.70
1.5	17.2	10.59
2.0	26.9	1.94
2.5	30.9	0.97
3.0	32.4	0.74
4.0	51.5	0.026
4.5	61.5	0.0046
5.0	75.4	0.0004
Fig. 10	45.7	0.073

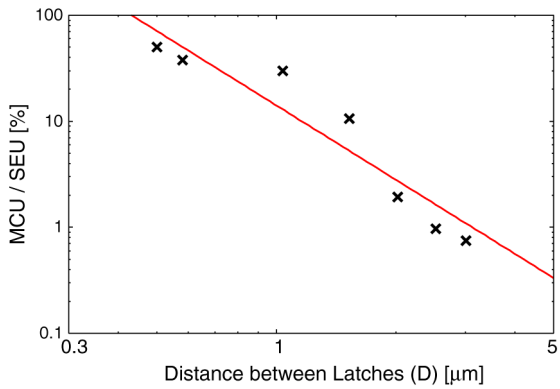

Fig. 12. The ratio of MCU to SEU by increasing D when $D_{\mathrm{WC}} = 20$ μm.

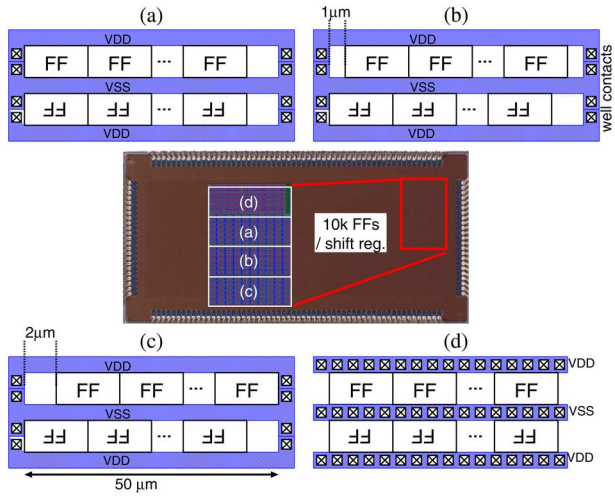

Fig. 13. Chip micrograph and conceptual layout structures of four different shift registers on the test chip.

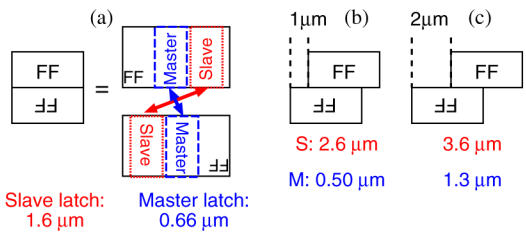

Fig. 14. Distance between master or slave latches on shift register (a)-(c) in Fig. 13.

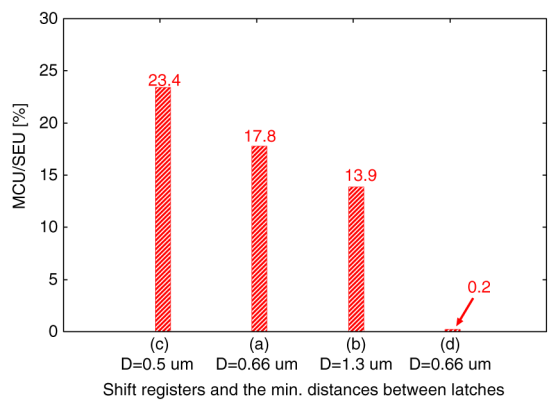

Fig. 15. The ratio of MCU/SEU according to the min. disatance between latches by experiments.

to estimate soft error rates on redundant flip-flops [13]. The dependence of MCU rates on the distance of FFs and well-contact density is also shown in this section.

A. Test Chips

In order to measure the soft error rates, we fabricated a 65 nm bulk CMOS test chip as shown in Fig 13. Four different shift registers. Each shift register includes 10k FFs. All shift registers are constructed by FFs and clock buffer chain [16]. These FFs are constructed in the same layout structure except for well contacts. The distance between the two rows in registers (a)-(c) are 0 μm, 1 μm, and 2 μm as shown in Fig. 13. These shift registers are used to estimate the cell-distance independence MCU rates. Fig. 14 shows different distances between slave latches and between master latches according to flip-flop placements.

The well contacts of the shift registers (a)-(c) are inserted every 50 μm. In order to obtain dependence of MCU rates on well-contact density, we fabricated well-contact arrays under the power and ground tap of the shift register (d) as shown in Fig. 13. The well-contact density is 60x higher than the others.

B. Experimental results analysis

The spallation neutron irradiation experiments were carried out at RCNP. In order to increase error counts, 28 chips is measured at the same time using stacked DUT boards. We use an engineering LSI tester to control DUTs and collect shifted error data. Fig. 15 shows the ratio of MCU to SEU according to the minimum distance by experiments. The ratio of MCU to SEU is reduced from 17.8% to 0.2% by inserting well-contact arrays under supply and ground rails of FFs, even if the minimum distance is the same. Therefore, we can improve soft-error resilience of the redundant FFs by increasing well contacts between redundant latches. It also shows that in the fabricated technology, almost all MCU is caused by the parasitic bipolar effect since it is caused by well-potential perturbation [17].

TABLE III
THE RATIO OF MCU TO SEU INFLUENCED BY D_{WC} ACCRODING TO THE DEVICE SIMULATIONS

D	D_{WC} [μm]					
	2.75	5.00	10.0	15.0	20.0	25.0
	MCU/SEU [%]					
0.5	4.57	26.28	43.63	46.38	48.79	49.65
0.6	2.31	22.31	28.18	33.56	37.70	45.74
1.0	0.0042	8.89	20.57	27.69	29.70	36.63
1.5	–	0.42	7.08	9.37	10.59	13.52
2.0	–	0.20	0.57	1.60	1.94	3.84
2.5	–	–	0.045	0.51	0.97	1.57
3.0	–	–	–	0.22	0.74	1.32
4.0	–	–	–	0.0017	0.026	0.32
4.5	–	–	–	–	0.0046	0.02
5.0	–	–	–	–	–	0.0038

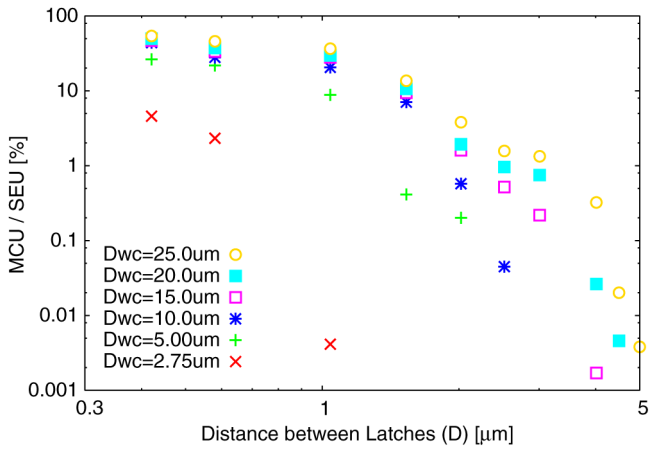

Fig. 16. Distance-dependence of the ratio of MCU to SEU by device-simulations in different D_{WC}.

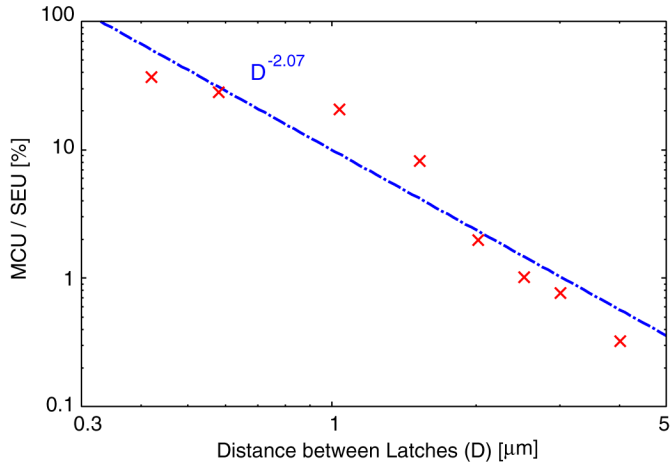

Fig. 17. Distance-dependence of the ratio of MCU to SEU by device simulations.

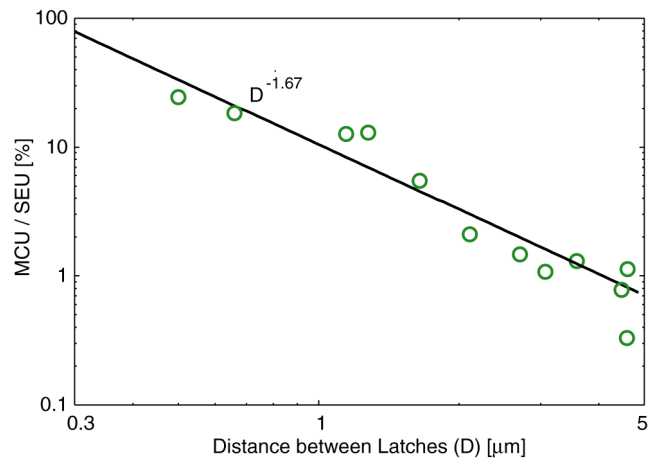

Fig. 18. Distance-dependence of the ratio of MCU to SEU by neutron experiments.

IV. COMPARISON OF DEVICE-LEVEL SIMULATION RESULTS AND EXPERIMENTAL RESULTS

FFs are placed every 5 μm on the measured chips. In order to get device-simulation result with higher accuracy, we use different (D_{WC}) as shown in Table III for calculating the ratio of MCU to SEU. Note that the ratios of MCU to SEU below 0.001% are not shown in the table. The distance-dependence of MCU / SEU by device simulations are shown in Fig. 16. Even if the ratios of MCU to SEU are different when we use different D_{WC} in device-simulations, all of the ratios decrease as shown in Fig 16.

We assume average values of all MCU / SEU for different D_{WC} in Table III from device-simulations is the MCU / SEU rate at each D. The average ratios of MCU to SEU are shown in Fig. 17. Fig. 18 shows the distance-dependence of MCU / SEU on FFs which is obtained from the shift registers (a)-(c). The ratio of MCU to SEU (y-axis) is obtained from measurement results. The ratio of MCU to SEU exponentially decreases influenced by $D^{-1.67}$ (D is the distance between redundant latches) and fitting line shows that it is almost 100% when $D < 0.3$ μm. The master and slave latches in the FF have different structures. However, the ratio of MCU to SEU by neutron experiments is distributed along the same straight line. Therefore, the MCU / SEU does not depend on the drive strength and load capacitance.

It is obviously shown that the ratios of MCU to SEU by device simulations and experimental results exponentially decrease by increasing the cell distance D. The fitting line exponentially decreases influenced by $D^{-2.07}$ by device simulations. Note that the fitting line is over 100%, it is means the ratio of MCU/SEU is 100% when D is shorter than 0.3 μm. According to the results of experiments and simulations, we must implement redundant FFs whose latches are separated by 4 μm from each other, in order to achieve 100x higher soft-error tolerance in redundant FFs than in non-redundant FF. It consumes huge area or complicated design procedures and these drawbacks become dominant by the process scaling.

Only one MCU is observed when the well contacts are placed between flip-flops by neutron experiments. Thus, MCU is suppressed by placing well-contact array under the supply and ground rail. However, the well potential is fixed in this layout structure. This kind of structure can not be used if the well potential is changed to mitigate variations or to control performance and leakage.

There is only heavy ion model which is used in the device-simulations. Mostly, it is difficult to compare the results between device-simulations and neutron experiments. We examined device-simulations agree with the conditions of neutron experiments as possible as we can. The device-simulation results coincide with the experimental results very well in this work. We reveal that the MCU / SEU rates can be calculated by simple device-simulations.

V. Conclusion

Based on the results of device simulations, we show that charge sharing and bipolar effect are two main factors when MCU occur in redundant latches. MCU is suppressed when the distance between the redundant latches (D) is increased. Total collected charge of L0 and L1 decreases by 50% by placing the well contacts adjacent to the redundant latches at which the distance between well contacts and redundant latches D_{WC} is 1.0 μm. Total collected charge of L1 reduces by 90% when the well contacts are placed between redundant latches. The ratio of MCU to SEU decreases to 0.073% in this kind of layout structure. According to the results of neutron experiments and device simulations, the ratio of MCU to SEU exponentially decreases by increasing the distance of latches D. The fitting lines are influenced by $D^{-1.67}$ and $D^{-2.07}$ by experiments and simulations respectively. Experimental results also show that MCU rates drastically reduce by inserting well-contact arrays under supply and ground rails. The number of MCU reduces to one. We use several simple device simulations to estimate the MCU tolerance of redundant latches. The results of device simulations almost coincides with the neutron experiments.

References

[1] S. Mitra, M. Zhang, S. Waqas, N. Seifert, B. Gill, and K. Kim, "Combinational logic soft error correction," in *Proc. IEEE International Test Conf.*, Oct. 2006, pp. 1–9.

[2] D. Krueger, E. Francom, and J. Langsdorf, "Circuit design for voltage scaling and SER immunity on a quad-core itanium processor," *Proc. Int. Solid-State Circuits Conf.*, pp. 94–95, Feb. 2008.

[3] B. Olson, D. Ball, K. Warren, L. Massengill, N. Haddad, S. Doyle, and D. McMorrow, "Simultaneous single event charge sharing and parasitic bipolar conduction in a highly-scaled SRAM design," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2132–2136, Dec. 2005.

[4] G. Gasiot, D. Giot, and P. Roche, "Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2468–2473, Dec. 2007.

[5] T. Uemura, Y. Tosaka, H. Matsuyama, K. Shono, C. Uchibori, K. Takahisa, M. Fukuda, and K. Hatanaka, "SEILA: Soft error immune latch for mitigating multi-node-SEU and local-clock-SET," in *Proc. Int. Rel. Phys. Symp.*, May 2010, pp. 218–223.

[6] D. Krueger, E. Francom, and J. Langsdorf, "Circuit design for voltage scaling and SER immunity on a quad-core itanium processor," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2008, pp. 94–95.

[7] K. Zhang, R. Yamamoto, J. Furuta, K. Kobayashi, and H. Onodera, "Parasitic bipolar effects on soft errors to prevent simultaneous flips of redundant flip-flops," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2012, pp. 5B.2.1–5B.2.4.

[8] N. Atkinson, A. Witulski, W. Holman, J. Ahlbin, B. Bhuva, and L. Massengill, "Layout technique for single-event transient mitigation via pulse quenching," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, pp. 885–890, Jun. 2011.

[9] J. Black, A. Sternberg, M. Alles, A. Witulski, B. Bhuva, L. Massengill, J. Benedetto, M. Baze, J. Wert, and M. Hubert, "HBD layout isolation techniques for multiple node charge collection mitigation," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2536–2541, Dec. 2005.

[10] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge collection and charge sharing in a 130 nm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3253–3258, Dec. 2006.

[11] D. Hansen, E. Miller, A. Kleinosowski, K. Kohnen, A. Le, D. Wong, K. Amador, M. Baze, D. DeSalvo, M. Dooley, K. Gerst, B. Hughlock, B. Jeppson, R. Jobe, D. Nardi, I. Ojalvo, B. Rasmussen, D. Sunderland, J. Truong, M. Yoo, and E. Zayas, "Clock, flip-flop, and combinatorial logic contributions to the SEU cross section in 90 nm ASIC technology," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3542–3350, Dec. 2009.

[12] K. Zhang and K. Kobayashi, "Contributions of charge sharing and bipolar effects to cause or suppress MCUs on redundant latches," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2013, pp. SE.5.1–SE.5.4.

[13] J. Furuta, K. Kobayashi, and H. Onodera, "Impact of cell distance and well-contact density on neutron-induced multiple cell upsets," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2013, pp. 6C.3.1–6C.3.4.

[14] P. Hazucha and C. Svensson, "Impact of CMOS technology scaling on the atmospheric neutron soft error rate," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2586–2594, Dec. 2000.

[15] P. Hazucha, C. Svensson, and S. Wender, "Cosmic-ray soft error rate characterization of a standard 0.6 um CMOS process," *IEEE J. Solid-State Circuits.*, vol. 35, no. 10, pp. 1422–1429, 2000.

[16] J. Furuta, C. Hamanaka, K. Kobayashi, and H. Onodera, "Measurement of neutron-induced SET pulse width using propagation-induced pulse shrinking," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2011, pp. 5B.2.1–5B.2.5.

[17] T. Nakauchi, N. Mikami, A. Oyama, H. Kobayashi, H. Usui, and J. Kase, "A novel technique for mitigating neutron-induced multi-cell upset by means of back bias," in *Proc. Int. Rel. Phys. Symp.*, May 2008, pp. 187–191.