A Low-Power and Area-Efficient Radiation-Hard Redundant Flip-Flop, DICE ACFF, in a 65 nm Thin-BOX FD-SOI

K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera

***Abstract*—In this paper, we propose a low-power area-efficient redundant flip-flop for soft errors, called DICE-ACFF. Its structure is based on the reliable DICE (Dual Interlocked storage CEll) and the low-power ACFF (Adaptive-Coupling Flip-Flop). It achieves lower power at lower data-activity. We designed DICE-FF and DICE-ACFF using 65 nm conventional bulk and thin-BOX FD-SOI (Silicon on Thin-BOX, SOTB) processes. Its area is twice as large as the conventional DFF. As for power dissipation, DICE ACFF achieves lower power than the conventional DFF below 20% data activity. When data activity is 0%, its power is half of the DFF. As for soft error rates DICE ACFFs are 1.5× better than conventional DICE FFs based on circuit-level simulations to estimate critical charge. No SEU is observed on the DICE ACFF by α-particle and neutron irradiations on the bulk and SOTB chips. From neutron irradiation results, the soft error rate of the DFF of the SOTB chip is 1/15 compared with that of the bulk chip.**

***Index Terms*—Dual-interlocked storage cell (DICE), FD-SOI, flip-flop, low-power, radiation-hard design.**

I. Introduction

CONTINUOUS process scaling down to nanometers makes LSI unreliable to soft errors. High performance computers (HPCs) are struggling with the power wall. Power consumption eliminates performance of HPCs. They are also very sensitive to soft errors since several thousand CPUs have to keep on running without any error for a few days. Soft errors are caused by a particle hit. Neutrons are coming from cosmic ray and alpha particles are from radioactive impurities embedded in packages, bonding wires and so on. Memory cells or latches are flipped if some amount of charge is generated due to particle hits. To reduce soft error rates, various redundant flip-flop (FF) structures are proposed, for example, TMR (Triple Modular Redundancy) [1] and DICE (Dual Interlocked storage CEll) [2]. They employ various radiation-hard techniques, but large area and power overheads are required.

In this paper, we propose a low-power area-efficient redundant flop-flop for soft errors, called DICE ACFF. Its structure is based on the reliable DICE and the low-power ACFF (Adaptive-Coupling Flip-Flop) [3]. From the aggressive process downscaling, short channel effects (SCEs) are becoming one of the dominant issues. To reduce leakage due to SCEs, FinFETs and FD-SOI (Fully-Depleted Silicon On Insulators) are two potential candidates. In general, FD-SOI improve soft-error sensitivity since sensitive volume is drastically reduced by the BOX (Buried OXide) layers under the thin transistor region. To compare the soft-error immunities, we fabricated two types of chips from the exact same layout patterns using a conventional bulk process and a Silicon-on-Thin-BOX (SOTB) in 65 nm [4], [5].

This paper is organized as follows. Section II explains the structure of the proposed DICE ACFF in detail. Section III describes the test chip fabricated to measure power and soft error rates of several non-redundant and redundant FFs. We explain how to evaluate soft error rates by charge sharing from circuit-level simulations in Section IV. Section V describes simulation and measurement results. Finally, we conclude this paper in Section VII.

II. DICE-ACFF

Fig. 1(a) shows the proposed low-power area-efficient redundant radiation-hard FF, called DICE-ACFF. Its structure is based on the reliable DICE FF (Fig. 1(b)) and the low-power ACFF [3] (Fig. 2).

The DICE structure mitigates soft errors by duplicating latches implemented by the half C-element and the clocked half C-element as shown in Fig. 1(c). The input and output signals of these half C-elements have cross-coupled connections to be automatically recovered from a flip on a single node. On the other hand, redundant FFs such as TMR, BISER [6] and BCDMR [7] mitigates soft errors by majority voting among three storage cells, in which a flipped node is left until the next clock signal is injected to supply an unflipped new value. Compared with these majority-voter-based structures, the DICE structure is area-efficient since latches are not triplicated but duplicated.

ACFF connects inverters for input, master and slave latches by PMOS or NMOS pass transistors. Conventional FFs based on transmission gates (called TGFF hereafter) use two phases of

Manuscript received September 27, 2013; revised February 03, 2014; accepted April 15, 2014. Date of publication June 25, 2014; date of current version August 14, 2014. This work was done in the "Ultra-Low Voltage Device Project" of LEAP, funded and supported by METI and NEDO. This work was also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc., Cadence Design Systems, Inc., and Mentor Graphics, Inc.

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Digital Object Identifier 10.1109/TNS.2014.2318326

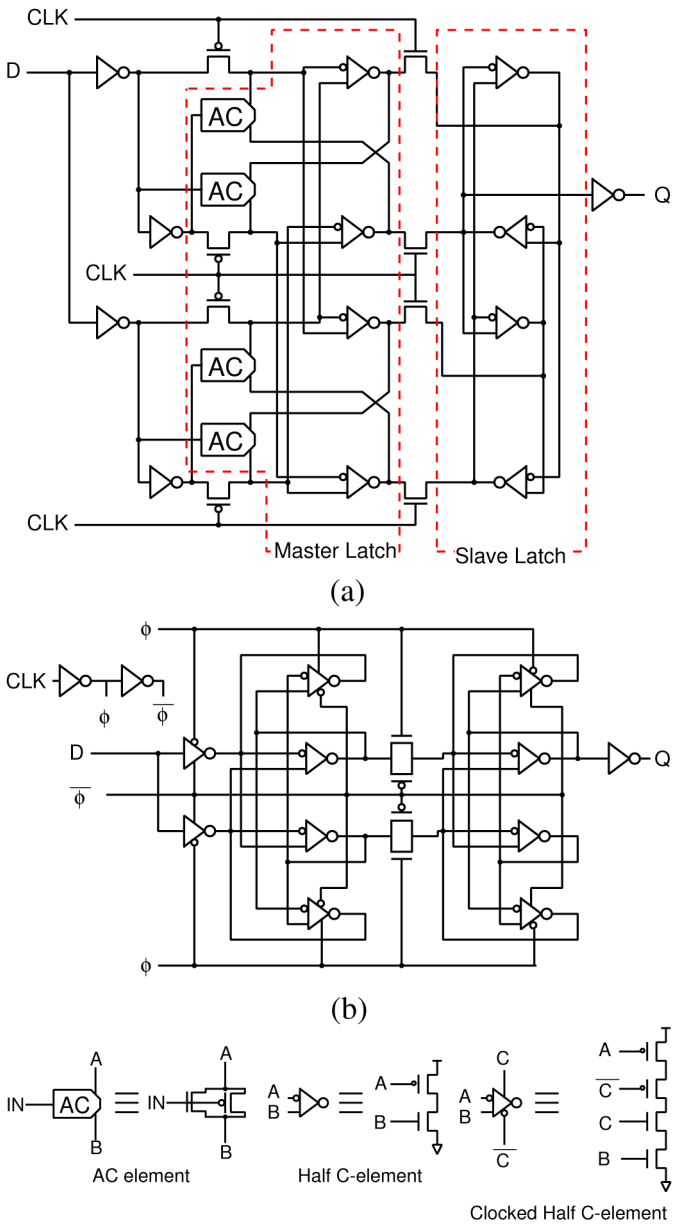

Fig. 1. Schematic diagram of DICE ACFF (a), DICE FF (b) and the detailed schematics of AC, half-C and clocked half-C elements (c).

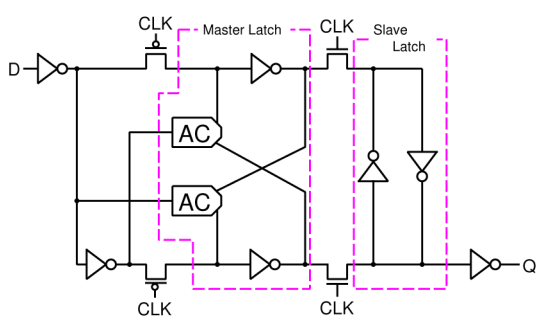

Fig. 2. Schematic diagram of ACFF.

clock signals CLK and $\overline{\text{CLK}}$. ACFFs, however, are operated by a single phase clock signal, which eliminates local clock buffers

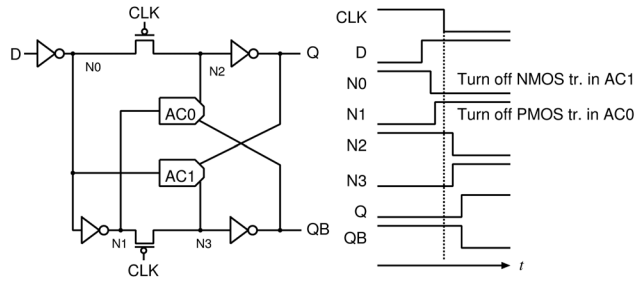

Fig. 3. How AC elements works when the stored value Q is changed from 0 to 1.

dissipating idle power when the activity of the input signal (the data activity, α) is low. In the conventional FFs, the power dissipation of clock buffers is dominant if α is low. The AC elements as shown on the left side of Fig. 1(c) composed of a CMOS pass gate are required to overwrite the master latch connected to the input inverters through PMOS pass transistors. They weaken the connection between the cross coupled inverters when the input and overwritten values are different. Fig. 3 explains how the AC element works when changing the stored value (Q) from 0 to 1. After CLK becomes low, the nodes N2 and N3 should change the stored values. The two AC elements AC0 and AC1 promote these value changes by turning off appropriate MOS transistors. As described in Fig. 3, the NMOS transistor in AC1 turns off in order to assist N3 to flip from 0 to 1. Without the AC elements, the output of cross-coupled inverters prevents these two nodes to flip. When the master latch value is transferred to the slave latch, the AC elements isolate the cross-couple connection in the master latch to make it easier for the master latch to overwrite the slave value.

The proposed DICE ACFF is implemented by combining these two structures, DICE and ACFF. In the master latch, inverters in the ACFF structure are replaced by half C-elements in the DICE structure. The structure of the slave latch is almost equivalent. The half C-elements are duplicated and they are cross-coupled in the same manner as the original DICE. The connection between the master and slave latches is done by four NMOS transistors instead of two CMOS pass gates in the conventional DICE. The slave latches in the DICE-ACFF are composed of four half C-elements instead of combinations of two half C-elements and two clocked half C-elements in the original DICE FF. The AC-elements assist the operation when the master latch overwrites the slave value as the same manner as the original ACFF.

BCDMR ACFF [8] is another redundant FF based on BCDMR and ACFF as shown in Fig. 4. There is no local clock buffer because of its ACFF-based structure, which makes it lower-power at the lower data activity. It is one of the triplicated redundant FFs by voting two redundant latches and one keeper in the master or slave latch. Due to the triplicated structure, its area overhead is bigger than the DICE ACFF. If one of the redundant latches is flipped, the keeper keeps the correct value since the C-element becomes high impedance. Even if the keeper is flipped, the C-element can overwrite the flipped value. In the half C-element and the clocked half C-element used in DICE, the output becomes an intermediate level due

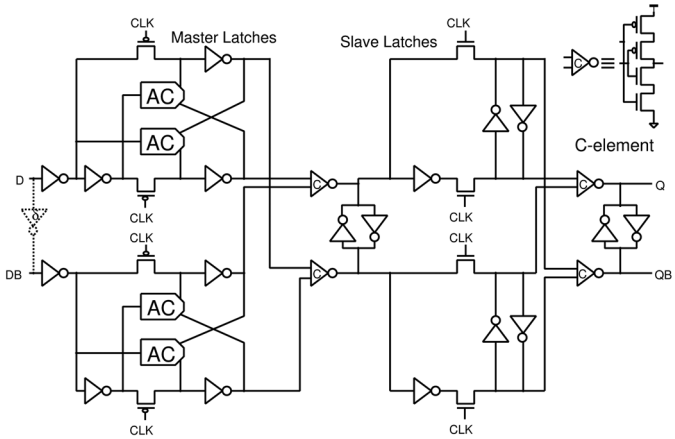

Fig. 4. Schematic diagram of BCDMR ACFF [8].

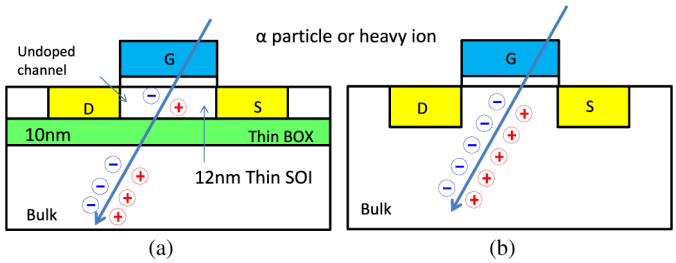

Fig. 5. SOTB (a) and conventional bulk (b) structures.

to the contention between PMOS and NMOS transistors when logic values of the two inputs are different. The contention is quickly resolved by its automatic recovery from a flip without any clock. But in the BCDMR structure, the contention is resolved after the next clock. To reduce the unwanted short-circuit current from the contention, the C-element as shown at the top-right in Fig. 4 is used instead of the half C-element.

III. FF Array Chip in a 65 nm Thin-BOX FD-SOI Process

We have implemented a chip, including the DICE FF and DICE-ACFF arrays with other non-redundant and redundant FFs in a 65 nm thin BOX FD-SOI process called SOTB [4]. Fig. 5 compares SOTB (a) and the conventional bulk (b) cross sections. SOTB guarantees low-voltage operations by undoped transistor channels to reduce variability of transistor characteristics from dopant fluctuations [5], [9]. In addition, the back-gate bias voltage can be controlled through the thin BOX layer. It can be forward biased ($V_{\rm bs} > 0$ on NMOS) when high-performance operations are expected, while it can be reverse biased for sleep or low-power operations. In the bulk structure, the forward bias voltage is limited to around 0.5 V in order not to turn on the PN junction between P-well and N-well. In the SOTB structure, backgates of transistors are isolated by the BOX layer. Further forward bias such as 1.0 V can be applied to enhance the performance [10].

Two types of chips are fabricated by the SOTB and bulk processes. Note that these two are fabricated by the exact same layout patterns besides thin BOX layers on SOTB.

Fig. 6 shows the chip micrograph and cell layout patterns. We have implemented seven FF arrays, including ACFFs, TGFFs,

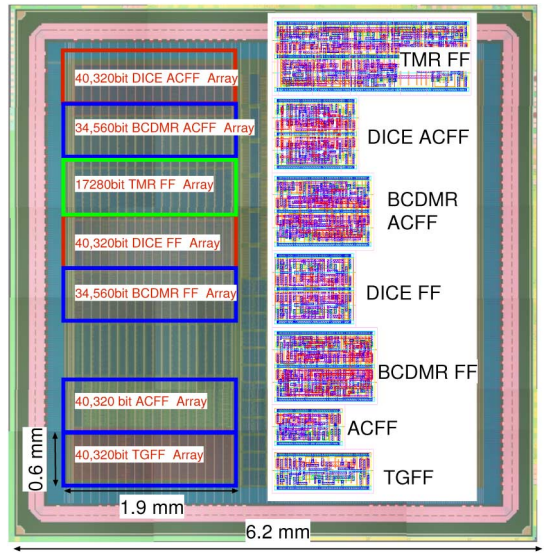

Fig. 6. Chip micrograph and cell layout patterns.

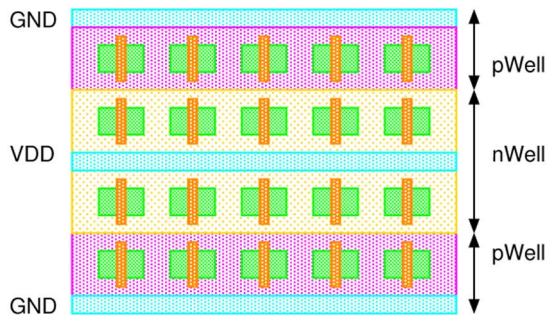

Fig. 7. Double Height Cell (DHC) structure.

DICE FFs, DICE ACFFs, BCDMR FFs, BCDMR ACFFs and TMR FFs. TGFF is a conventional DFF using transmission and tristate gate. Non-redundant FFs such as ACFFs and TGFFs are implemented in a single row, while the other five redundant ones are implemented in two rows as the double height cells (DHCs) as shown in Fig. 7 [11]. All redundant FFs are implemented using the DHCs by sharing PMOS (N-well) regions, which is much stronger to soft errors than sharing NMOS regions [12]. It is partly because major carriers of NMOS are electrons whose mobility is much faster than holes. NMOS regions are much more sensitive than PMOS regions.

The area of DICE ACFF is almost twice as large as TGFF but only 1.05× bigger than the conventional DICE FF. The detailed comparison of the cell areas is described later in Section V-B.

When initializing data in all FF arrays on measurements, all FFs are connected in series as a shift register. On measurements by α particles or neutron irradiation by applying clock signals, several FFs are connected in a loop to trap flipped values in the FF array while applying clocks [7] as shown in Fig. 8. Table I lists the total number of FFs in each array and the number of FFs in a local loop unit ($N_{\rm LLU}$). Note that $N_{\rm LLU}$ is different with each array to equalize macro sizes to 0.6 mm × 1.2 mm. Wider FFs such as TMR have smaller $N_{\rm LLU}$.

The LLU structure is convenient to measure power dissipation according to the data activity α. If FFs in an LLU is initial-

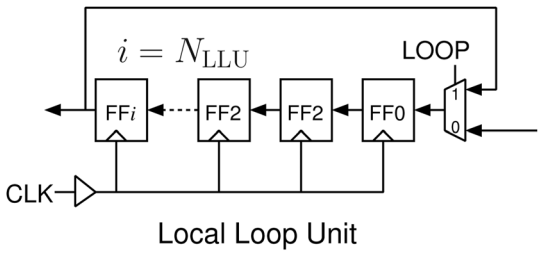

Fig. 8. Local loop to trap flipped values inside the loop while applying clock.

TABLE I
NUMBER OF FFS IN AN LLU (N_{LLU}) AND THE TOTAL NUMBER OF FFS IN EACH ARRAY

FF	N_{LLU}	Total number of FFs
DICE ACFF	14	40,320 ($18 \times 160 \times 14$)
BCDMR ACFF	12	34,560 ($18 \times 160 \times 12$)
TMR FF	6	17,280 ($18 \times 160 \times 6$)
DICE FF	14	40,320 ($18 \times 160 \times 14$)
BCDMR FF	12	34,560 ($18 \times 160 \times 12$)
ACFF	14	40,320 ($18 \times 160 \times 14$)
TGFF	12	40,320 ($18 \times 160 \times 14$)

ized as the checkerboard patterns, we can measure power dissipation at $\alpha = 100\%$. When a single FF is initialized to 1 and other FFs are to 0, α becomes $2/N_{\mathrm{LLU}}$.

IV. ESTIMATION OF SOFT ERROR RATES BY CIRCUIT-LEVEL SIMULATIONS

Stored values in FFs are flipped if the generated charge by a particle hit exceeds a certain threshold value, which is called Q_{crit}. In redundant FFs such as DICE, two nodes must be flipped simultaneously.

The probability of two simultaneous hits on redundant nodes by different particles are negligible. We assume that a single particle hit flip multiple redundant nodes and generated charge from a single particle is shared by these redundant nodes. As shown in Fig. 7, the implemented DICE ACFF shares a PMOS region. We ignore simultaneous flips by NMOS transistors since they are separated by the PMOS region. It separates the redundant nodes not to flip simultaneously by charge sharing and parasitic bipolar effects. The PMOS region drastically reduces the possibilities of successive hits of secondaries by the node separation. The PMOS region increases the distance between redundant nodes at least 2.0 μm in the 65 nm process. Therefore, we only evaluate Multiple Cell Upsets (MCUs) in the PMOS region by charge sharing. Parasitic bipolar effects and successive hits of the secondaries in the PMOS region are ignored to simplify the computation of soft error rates only by the circuit-level simulations. Eq. (1) is an empirical equation (not physically-based) to compute soft error rates (SERs) by terrestrial neutrons [13], [14], [15].

$$N_{SER}(Q_{\mathrm{crit}}) = F \times K \times A \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}\right) \qquad (1)$$

in which, F is a neutron flux in the terrestrial region (0.00565 n/cm^{2}s), K is a constant value of 2.2×10^{-5}, and A is the total drain area connected to the node. Q_{s} is a value that can be determined by process parameters. From 65 nm neutron irradiation results in [8], Q_{s} in NMOS is 6.92 fC and that in PMOS is 3.40 fC.

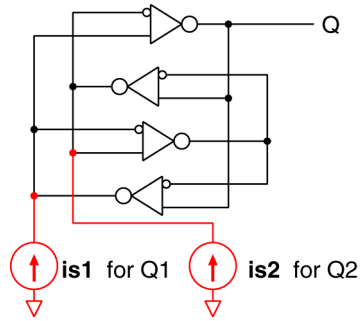

Fig. 9. Two single exponential current sources (is1 and is2) attached to two nodes of the latch.

In order to compute MCUs by a single particle hit, we use charge collection ratio according to the distance from the particle hit point. From the heavy ion results in [16] for 130 nm process, charge collection efficiency (E) is exponentially reduced by the distance x between the drain and the particle hit point expressed by the following equation.

$$E_{\mathrm{n}}(x) = 0.285\exp(-1.12x): \quad \text{for NMOS} \qquad (2)$$

We consider MCU by the charge sharing in the bulk process to apply Eq. (2) to the 65 nm process. Note that we use Eq. (2) without any modification from 130 nm results, which is unvalidated for 65 nm process. In addition to that, the SOI process has much less charge collection efficiency that cannot be handled by Eq. (2).

In non-redundant FFs such as TGFFs, a single-exponential current source is enough to evaluate Q_{crit}. In the triplicated structure such as TMR or BCDMR, two storage elements such as latches or keepers does not influence with each other. Two successive simulations with one single-exponential current source are enough to compute Q_{crit}.

In the DICE structure, however, two single-exponential current sources must be attached on the circuit-level simulations as shown in Fig. 9 since two redundant storage elements are cross-coupled. Two independent current sources Q1 and Q2 are attached to two nodes that can flip the stored value, which is called a critical pair. By changing the amount of charge on Q1 and Q2, a Shmoo-like error map is depicted in Fig. 10.

Fig. 11 shows how to compute soft error rates (SERs) from the critical charge of two transistors in a critical pair of a redundant FF. It is flipped when drain nodes of these two transistors are simultaneously flipped. In the DICE FF, two nodes attached the current sources is1 and is2 in Fig. 9 form one possible critical pair. From Eq. (2), we can compute $Q'_{\mathrm{critA}}(x) = Q_{\mathrm{critA}}/E_{\mathrm{n}}(x)$ and $Q'_{\mathrm{critB}}(d-x) = Q_{\mathrm{critB}}/E_{\mathrm{n}}(d-x)$. The larger value $Q_{\mathrm{mcrit}}(k)$ between these two Q'_{crit} values can be considered as the critical charge in the region k.

By assigning $Q_{\mathrm{mcrit}}(k)$ to Q_{crit} and the area of the region k to A in Eq. (1), $N_{\mathrm{SER}}(k)$ is computed in the region k. By

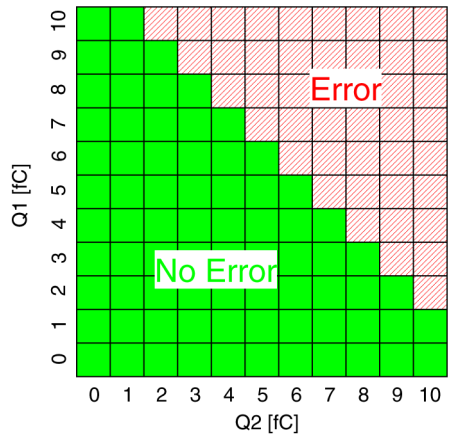

Fig. 10. Error map for DICE structure.

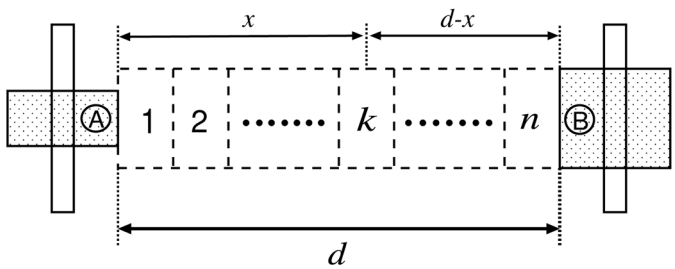

Fig. 11. How to compute SERs of the critical pair transistors A and B.

summing these values from all the region, we can obtain the total SER N_{TSER} of the critical pair as follows.

$$N_{\mathrm{TSER}} = \sum_{k=1}^{n} N_{\mathrm{SER}}(k) \tag{3}$$

V. Simulation and Measurement Results Related to Power and Delay.

We compare the proposed DICE ACFF in terms of power, area, delay, ADPP (Area, Delay and Power Product) with TGFF, ACFF, DICE FF, BCDMR FF, BCDMR ACFF and TMR FF.

A. Power Dissipation by Data Activity

We evaluate power dissipation by circuit-level simulations and measurements. In the circuit-level simulations, we bundle 8 FFs with a clock buffer as shown in Fig. 12. It is because FFs based on the ACFF dissipates less power due to its clock-buffer-less structure. Fig. 13 show power dissipation according to the data activity α from circuit-level simulations with SOTB parameters.

The power dissipation of DICE ACFFs becomes lower than TGFFs when α is below 20%. In general ASICs, the activity ratio α is from 5% to 15% [3]. The proposed DICE ACFF always operates at lower power under the condition. The power dissipation at $\alpha = 10\%$ is 77% of TGFF.

Fig. 14 shows power dissipation from measurements of the SOTB chip. The y axis is the power dissipation per each FF in

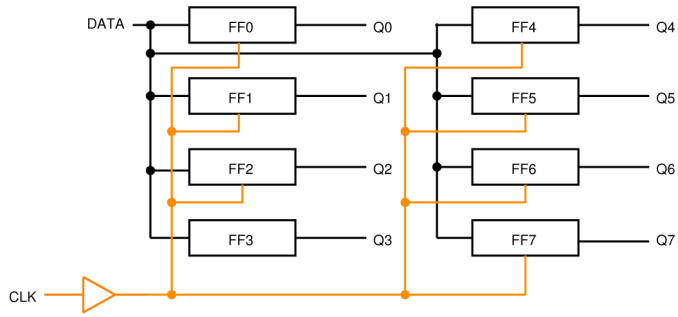

Fig. 12. Simulated circuit structure to compute power dissipation.

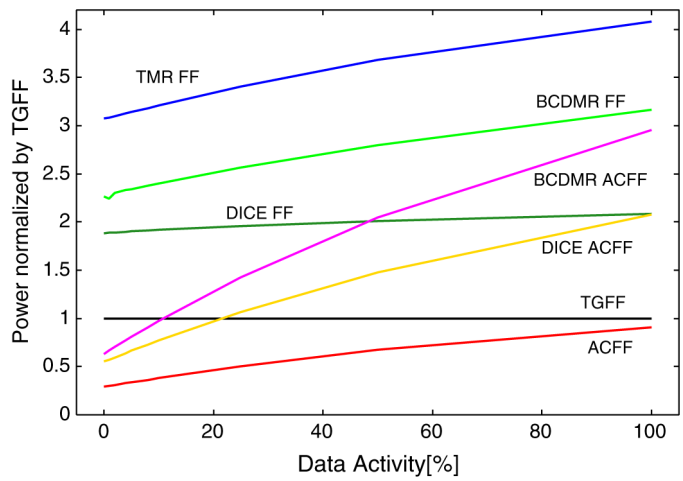

Fig. 13. Simulated power dissipation normalized by the power of TGFF with SOTB parameters.

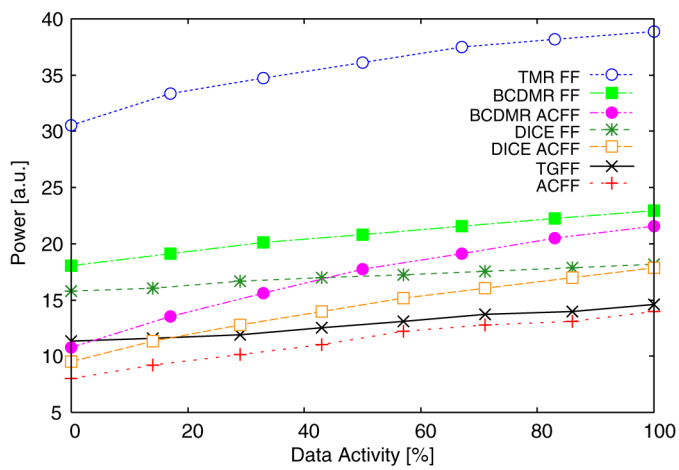

Fig. 14. Measured power dissipation of the SOTB chip.

arbitrary units. The y axis is not normalized by the power of TGFF. It is because the N_{LLU} is different from each FF array. The data activity α is changed by the initial FF values in the local loop unit as described in the previous section. The power dissipation simulations agree very well with the measurements.

The bulk and SOTB chips are fabricated from the exact same layout pattern besides the BOX layer, but the threshold voltages (V_{TH}) of transistors are different. The SOTB transistors

TABLE II
AREA, POWER AND DELAY VALUES AT $\alpha = 10\%$ OF FFS NORMALIZED BY TGFFS. (POWER AND DELAYS FROM CIRCUIT-LEVEL SIMULATIONS WITH SOTB PARAMETERS.)

FF	Area	Power	average delay	rise delay	fall delay
TGFF	1.00	1.00	1.00	1.00	1.00
ACFF	0.76	0.456	0.49	0.43	0.55
DICE FF	2.00	2.28	1.29	1.43	1.18
DICE ACFF	2.10	0.716	0.86	0.73	0.97
BCDMR FF	2.50	2.403	1.75	1.51	2.03
BCDMR ACFF	2.40	0.911	1.15	1.21	1.11
TMR FF	5.20	3.21	1.52	1.55	1.52

have lower $V_{\rm TH}$ than the bulk transistors. To equalize the performance of the bulk and SOTB chips at $\rm VDD = 1.2$ V, the reverse body bias of -2.1 V is applied to both NMOS and PMOS transistors of the SOTB chip. The power dissipation of the SOTB chip at the -2.1 V reverse body bias is 69% of the bulk chip. The reason why the SOTB power is lower than bulk is mainly due to the lower junction capacitance of the SOTB transistors.

B. Area, Delay and Power Product

Table II lists area, power at $\alpha = 10\%$ and delay with SOTB parameters when the process corner is typical, the supply voltage is 1.2 V and the temperature is 25°C. Note that the definition of the delay is CLK to Q estimated from circuit-level simulations with extracted stray capacitance. In the slave latches of ACFF, DICE ACFF and BCDMR ACFF, there is one inverter for output from clock-controlled pass transistors between master and slave latches, while there are two series inverters in the slave latches of TGFF and DICE FF. Thus the CLK-to-Q delay becomes longer in TGFF and DICE FF. In BCDMR ACFF, the C-element and the keeper make delays longer. Delays of those FFs become longer as the following order.

$$D_{\rm ACFF} < D_{\rm DICEACFF} < D_{\rm TGFF} < D_{\rm BCDMRACFF} < D_{\rm DICEFF} < D_{\rm TMRFF}$$

Table III shows the ADPP. Delay and power values are obtained from circuit-level simulations with SOTB parameters. At $\alpha = 0\%$, the ADPPs of DICE ACFF and TGFF are equivalent. As α increases, the ADPP of DICE ACFF increases compared with that of TGFF. But the ADPP at $\alpha = 10\%$ is still only 39% bigger than that of TGFF. The proposed DICE ACFF is efficient in terms of area, power and delay.

VI. SIMULATION AND MEASUREMENT RESULTS OF SOFT ERRORS

We have two measurement results, one by α particle and the other is by spallation neutron beam. Here we reveal these two results in detail with the results from simulations.

A. Soft Error Rates from Simulations

Table IV lists neutron SERs in FIT (Failure in Time) /Mbit from circuit-level simulations at $V_{\rm DD} = 1.2$ V as explained in Section IV. It shows the highest SERs obtained from all possible

TABLE III
$\rm Area \times Delay \times Power$ OF FFS NORMALIZED BY CONVENTIONAL TGFFS ACCORDING TO THE DATA ACTIVITY α. (POWER AND DELAYS FROM CIRCUIT-LEVEL SIMULATIONS WITH SOTB PARAMETERS.)

FF	α=0	α=10	α=25	α=100
TGFF	1.00	1.00	1.00	1.00
ACFF	0.12	0.15	0.21	0.38
DICE FF	4.48	4.95	5.05	5.39
DICE ACFF	1.00	1.39	1.93	3.75
BCDMR FF	9.92	10.5	11.2	13.9
BCDMR ACFF	1.74	2.68	3.92	8.15
TMR FF	24.3	25.4	26.9	32.2

TABLE IV
SERS OF FFS COMPUTED BY EQ. (1) FOR A 65 NM BULK TECHNOLOGY. ($Q_{\rm crit}$ IS ESTIMATED BY CIRCUIT-LEVEL SIMULATIONS WITH BULK PARAMETERS.)

FF	SER [FIT/Mbit]	SER/TGFF	1/(SER/TGFF)
TGFF	379	1.0	1.0
ACFF	285	0.75	1.3
DICE FF	1.22	0.0032	310
DICE ACFF	0.82	0.0022	460
BCDMR FF	0.17	0.00045	2200
BCDMR ACFF	0.16	0.00042	2400

stored values and clock states. As shown in the table, TGFF and ACFF have several hundreds FIT/Mbit due to their non-redundant structures. The proposed DICE ACFF has the 1.5× lower SER than DICE FF which relationship is equivalent to that between ACFF and TGFF. DICE ACFF has a lower SER than DICE FF mainly because the higher critical charge and the longer distance between the nodes in the critical pairs.

BCDMR ACFF has approximately 5× lower SER than DICE ACFF. It is mainly because of its area penalty. As the distances between critical pairs become shorter, the values of $Q_{\rm crit}$ also becomes smaller according to Eq. (2). The main purpose of the DICE ACFF is to achieve lower power and lower area penalty. As in Table II, BCDMR ACFF is 14.3% bigger than DICE ACFF. The ADPP of DICE ACFF is always lower than that of BCDMR ACFF at any data activity α. It means that DICE ACFF achieves lower power, shorter delays and smaller area at the expense of the 5× higher SER than BCDMR ACFF.

B. α Irradiation

We measure soft error probabilities by an α particle source (3 MBq $^{241}\rm Am$), which is mounted on the top of the DUTs as shown in Fig. 15. The distance between the die and the α particle source is approximately 0.7 mm. Tables V and VI show the number of errors from 300 sec. α particle irradiation without applying any clock during irradiation. The error probability of TGFF is higher than that of ACFF, which is consistent with the simulation results in Table IV. All the implemented FFs are positive-edge triggered. Thus the master latches are in the hold state when $\rm CLK = 1$, while the slave latches are in the hold state when $\rm CLK = 0$. The error probability of ACFF is much smaller when $\rm CLK = 1$ than $\rm CLK = 0$. As shown in Fig. 2, ACFF has the master latch including the AC element, while the slave latch consists of simple cross-coupled inverters. The AC elements are inserted between the cross-coupled inverters in the master latch, which prevent the flip of the master latch. As the same manner,

TABLE V
BULK IRRADIATION RESULTS AT VDD = 1.2 V WITH NO BODY BIAS. NUMBER OF ERRORS FROM 300 SEC. α PARTICLE IRRADIATION AND ERROR PROBABILITIES DEFINED AS THE RATIO BETWEEN THE NUMBER ERRORS AND TOTAL NUMBER OF FFS

		ACFF	TGFF	TMR FF	BCDMR FF	BCDMR ACFF	DICE FF	DICE ACFF
# of Errors	CLK=0	1,911	4,672	1,053	10	15	0	0
	CLK=1	59	7,887	944	9	3	0	0
Total # of Errors		1,970	12,559	1,997	19	18	0	0
Total # of FFs		40,320		17,280	34,560		40,320	
Error Proba-bility	CLK=0	4.7%	11.5%	6.1%	0.03%	0.04%	0	0
	CLK=1	1.5%	19.6%	5.5%	0.03%	0.01%	0	0
	Average	3.1%	15.6%	5.8%	0.03%	0.03%	0	0

TABLE VI
SOTB IRRADIATION RESULTS AT VDD = 1.2 V WITH −2.1 V REVERSE BODY BIAS ON BOTH N-WELL AND P-WELL BY 300 SEC. α PARTICLE IRRADIATION

		ACFF	TGFF	TMR FF	BCDMR FF	BCDMR ACFF	DICE FF	DICE ACFF
# of Errors	CLK=0	3	0	0	0	0	0	0
	CLK=1	0	57	0	0	0	0	0
Total # of Errors		3	57	0	0	0	0	0
Total # of FFs		40,320		17,280	34,560		40,320	
Error Proba-bility	CLK=0	0.01%	0	0	0	0	0	0
	CLK=1	0	0.14%	0	0	0	0	0
	Average	0.005%	0.07%	0	0	0	0	0

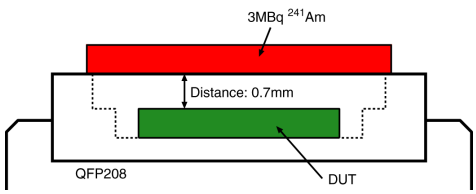

Fig. 15. Test setup of the α particle irradiation.

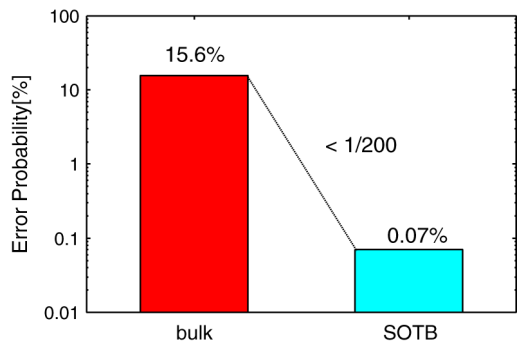

Fig. 16. Comparison of error probability of TGFFs between bulk and SOTB at VDD = 1.2 V by α particle irradiation without applying clock.

the master latch of the DICE ACFF with the AC element is much stronger than the slave latch without it. No error is observed by α particle irradiation in the DICE ACFF.

In the DICE structure, a flipped node by an α hit automatically goes back to its original state soon after. The multiple hit on a DICE FF does not cause any error. Thus we observe no errors on DICE FFs and DICE ACFFs.

If multiple α particles hit two latches on a TMR FF, its output is flipped since we apply no clock during irradiation. The error probability of TMR FFs is higher due to the higher error probability on the TGFF. The error probability of TMR FFs (P_{TMR}) is computed from Eq. (4) using the error probability of TGFFs (P_{TGFF}).

$$P_{\mathrm{TMR}} = 3P_{\mathrm{TGFF}}^2 - 2P_{\mathrm{TGFF}}^3 \tag{4}$$

The first term $3P_{\mathrm{TGFF}}^2$ is the probability of all combinations of simultaneous flips of two FFs among three FFs in the TMR FF. The second term subtracts the probability twice when all three FFs are simultaneously flipped.

When $P_{\mathrm{TGFF}} = 11.5\%$ (CLK = 0 in Table V), P_{TMR} is computed as 3.6% which is almost equivalent to the value of 6.1% in Table V.

Fig. 16 compares the error probabilities of TGFFs between the bulk and SOTB chips. The probabilities of TGFF, 0.07% on the SOTB chip is almost 1/200 compared with 15.6% of the bulk chip. The error probability of SOTB is smaller than bulk by two orders of magnitude. We observe no error on the redundant FFs in the SOTB chip. The SOTB process gives very high soft-error tolerance due to its lower sensitive volume.

C. Neutron Irradiation

Neutron irradiation experiments were carried out by the spallation neutron beam at RCNP (Research Center for Nuclear Physics) of Osaka University [17]. The average accelerated factor is 4.77×10^8 compared with the ground level of Tokyo. Table VII shows the number of errors, measurement hours, number of FFs and SERs in FIT/Mbit by applying 35 MHz clock on all the measured FFs. They are initialized to all 0 before irradiation. We observe no errors in all redundant FFs on both bulk and SOTB chips. No error is observed in ACFFs by SOTB. As for TGFF, the SER of SOTB is 1/15 smaller than that of bulk as shown in Fig. 17.

VII. CONCLUSION

We propose a low-power area-efficient redundant flip-flop, called DICE ACFF. Its structure is based on reliable DICE and

TABLE VII
NEUTRON IRRADIATION RESULTS BY APPLYING 35 MHZ CLOCK

	# of observed errors	Irradiation time	# of FFs	SER [FIT/Mbit]
TGFF(bulk)	194	19h	40,320	554
ACFF(bulk)	93	19h	40,320	266
All Redundant FFs (bulk)	0	19h	-	0
TGFF(SOTB)	7	11h	40,320	35
ACFF(SOTB)	0	11h	40,320	0
All Redundant FFs (SOTB)	0	11h	-	0

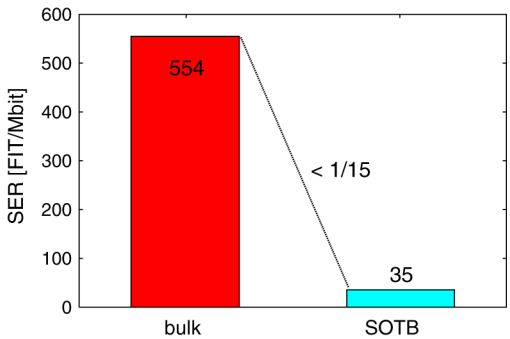

Fig. 17. Comparison of SER in FIT/Mbit of TGFFs between bulk and SOTB at $\mathrm{VDD} = 1.2$ V by neutron irradiation applying 35 MHz clock.

the low-power ACFF. It achieves low-power at lower data-activity. If data activity is lower than 20%, its power is lower than conventional DFF based on transmission gates (TGFF). Conventional ASICs have 5% to 15% data activity. DICE ACFFs always achieve lower power than TGFFs in these regions. Its area overhead is 2.1× of the TGFF and 1.05× of the conventional DICE FF. The DICE ACFF is superior to the DICE FF in power, area and soft error resilience. We have implemented arrays of DICE ACFFs and DICE FFs and other redundant and non-redundant FFs in both 65 nm bulk and SOTB processes. The error probability of low-power ACFF by α particle irradiation is 1/5 compared with that of TGFF in the bulk process. From neutron irradiation, ACFF by SOTB has no error as same as all the redundant FFs on bulk and SOTB. ACFF can be applied for low-power consumer products for non-critical usages on bulk and for critical usages on SOTB. We observe no error on DICE FF and DICE ACFF by α particle irradiation for 300 sec. All redundant FFs have no error by neutron irradiation. The SOTB process gives very high soft-error tolerance due to its lower sensitive volume.

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