# An Area-efficient 65 nm Radiation-Hard Dual-Modular Flip-Flop to Avoid Multiple Cell Upsets

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***Abstract*—**

**A layout structure to avoid upsets due to Multiple Cell Upsets (MCUs) is proposed for rad-hard dual-modular Flip-Flops (FFs) called BCDMR (Bistable Cross-coupled Dual-Modular Redundancy) by separating critical components. We have fabricated a 65 nm chip including 30 kbit dual-modular FF arrays on twin-well and triple-well structures. High-energy broad-spectrum neutron irradiations reveal that no soft error is observed up to 100 MHz in the twin-well, but some errors are observed in the triple well. The triple-well structure is sensitive to MCUs because the p-well potential can be easily elevated.**

***Index Terms*—Radiation-hard design, Multiple Cell Upset(MCU), flip-flop, 65 nm bulk CMOS, dual-interlocked storage cell (DICE), built-in soft-error resilience (BISER), bi-stable cross-coupled dual-modular (BCDMR)**

## I. Introduction

Aggressive process scaling makes the probability of multiple cell upsets greater. The physical dimensions of an SRAM cell or a Flip-Flop (FF) are about equal to the physical dimensions of layout area effected by a particle strike[1]. Seifert et.al. [2] reveals that the probability of Multiple Cell Upsets (MCUs) compared with Single Event Upsets (SEUs) is 10% in a 65 nm process. MCUs are one of critical issues to diminish soft-error resiliency of rad-hard designs. If two FFs are flipped on a triple-modular redundancy (TMR) design, the wrong flipped value is regarded as a correct one. MCUs are very likely happened on TMR when redundant FFs are closely placed.

We have proposed Bi-stable Cross-coupled Dual-Modular (BCDMR) FFs [3] based on BISER (Built-In Soft Error Resilience) [4]. These dual-modular FFs are robust to soft-errors by SEUs to keep a correct value by redundant latches and keepers. It is also robust to a SET (Single Event Transient) pulse injected from its input (D) by placing delay elements in order to avoid both redundant latches to capture the error pulse. The dual-modular FFs require only a single delay element, while conventional TMR (Triple-Modular Redundancy) FFs require two delay elements. Area-overhead due to delay elements can be smaller on the dual-modular FFs than on the TMR FF.

BCDMR FFs are insensitive to MCUs caused by a SET pulse from C-elements[5] and achieve much better soft error resiliency than BISER by alpha-particle irradiations[3]. On the other hand, neutron irradiations show that soft error rates of BCMDR is almost equivalent to BISER and is just 10x stronger than non-redundant D-FFs. We assume that such low error tolerance is due to MCUs since the 1/10 error rates can be computed from 10% MCUs rates of D-FFs in a 65 nm process.

We have fabricated another chip in a 65 nm bulk CMOS process including the revised version of the BISER and BCDMR FFs. It has an enhanced layout structure to separately place critical components against MCUs. High-energy broad-spectrum neutron irradiations show that the proposed enhanced layout structure have no errors at 100 MHz clock frequency while the conventional BISER structure have 44 FIT/Mbit at the same clock frequency. The main contributions of this paper are to propose a robust redundant FF layout structure to avoid MCUs and to show the actual measurement results of a 65 nm chips by neutron irradiations.

This paper is organized as follows. Section II shows the reason why redundant FFs are very sen-

sitive to MCUs. Section III explains the BCDMR FF in detail. We propose a robust layout structure of the redundant FFs in Sect. IV. The measurement results by neutron irradiations are shown in Sect. V, which is followed by the conclusion.

## II. Vulnerability against SET Pulse of Redundant FFs

### A. SET Pulse between Master and Slave Latches

Several experimental results shows that SET pulses from combinational circuits are distributed from several ps to 1,000 ps[6], [7], [8]. If the clock pulse width is close to the SET pulse width, a SET pulse asserted between the master and slave latch causes an SEU. The upper part of Fig. 1 shows a simplified schematic diagram of a master-slave edge-triggered FF. An inverter is inserted as an aid to explain vulnerability against a SET pulse. The source of the SET pulse can be any component in the master latch directly connected to the slave latch. The bottom part of Fig. 1 shows the transient output Q by four different SET pulses from P0 to P3. The first pulse P0 is injected during the transparent (trans.) state of the slave latch. Although P0 is propagated to Q, it is still a SET pulse that can be filtered by masking effects or delay elements in front of master latches in the next stage to be connected after combinational logics. The second pulse P1 is during the latch state, which is never transmitted to Q. The third pulse P2 is generated between the latch and trans. state. It is almost same as the P0 case. The last pulse P3 causes an SEU in SL since it starts during the trans. state of SL and continues to the latch state.

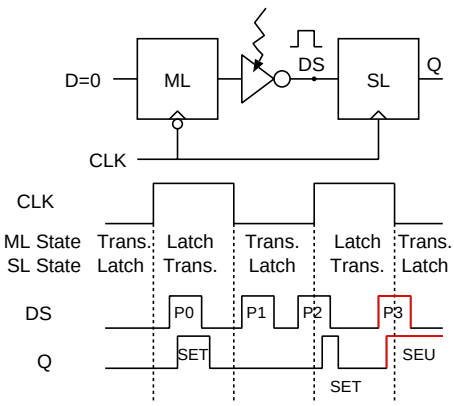
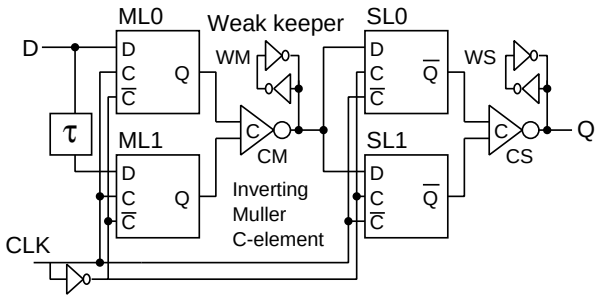
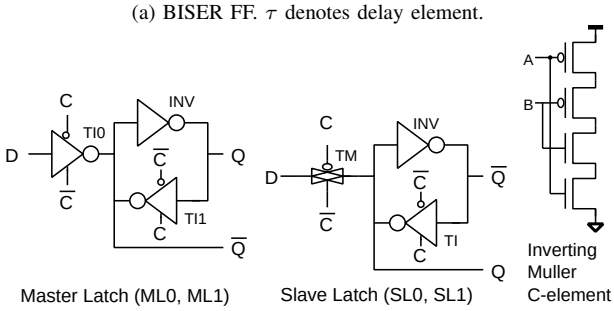



Fig. 1. Simplified schematic diagram of a master-slave positive-edge-triggered FF(upper) and four SET pulses (P0-3) from inverter.




(a) BISER FF. $\tau$ denotes delay element.




(b) Schematics of components in BISER.

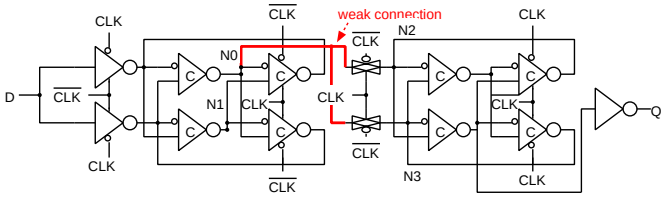
Fig. 2. BISER FF and schematics of components.

The possibility when such a SET pulse is asserted during the positive clock edge can be ignored when the clock pulse width is sufficiently larger than the SET pulse. But it can not be ignored when it is close to the SET pulse width. For example, if the clock frequency is 1 GHz and the SET pulse width is 100 ps, the possibility that the SET causes an SEU is roughly 10%. Therefore the SER (Soft Error Rate) of redundant FFs with the structure of Fig. 1 is reduced to 1/10 of non-redundant FFs.

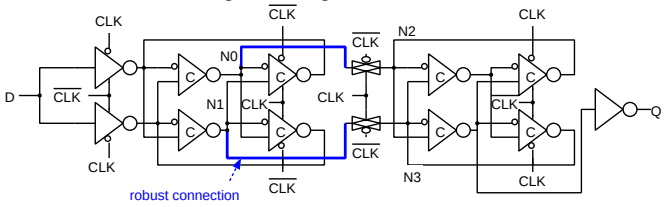
### B. Vulnerability in BISER and DICE Structures

Fig. 2 (a) shows the schematics of BISER[4]. The BISER structure consists of master and slave parts, each of which consists of a pair of latches, an inverting Muller C-element and a weak keeper. Fig. 2(b) shows schematics of master/slave latches and the C-element. If one of the latches is flipped due to an SEU, the output of the C-element becomes high-impedance and the weak keeper keeps the correct value. An SEU on weak keepers or a SET pulse from the C-element cannot flip the output value of the C-element permanently since the C-element driven by the pair of latches strongly keeps its stored value and the flipped value is quickly restored. The output of the C-element, however, is connected to both of two slave latches. A SET pulse from WM or CM may flip the pair of slave latches simultaneously.

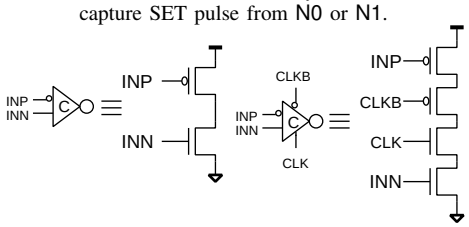
A SET pulse between master and slave latches also invokes similar vulnerabilities on DICE (Dual-




(a) Vulnerable DICE FF structure in which two nodes N2 and N3 may capture SET pulse from N0.




(b) Robust DICE FF structure in which only one node N2 or N3 may capture SET pulse from N0 or N1.




(c) Schematics of components in DICE.

Fig. 3. Two possible DICE FF structures.

Interlocked storage CEll) latches[9]. If two input ports of slave latches are connected to a single output port of the master latch, the slave DICE latch may be flipped by a SET pulse from the master latch. Unfortunately, these vulnerabilities are rarely mentioned because almost all experiments are done without giving any clock to FFs. Fig. 3 shows two possible DICE FF structures to connect master and slave latches. In Fig. 3 (a), two nodes (N2, N3) of slave latches are connected to N0. It is similar to the BISER structure. When a SET pulse is injected at N0, these two nodes N2, N3 may be affected. On the other hand, Fig. 3 (b) is robust since these two nodes are separately connected to N0 or N1. A SET pulse from the master part only affects a single node of the slave part.

## III. Bi-stable Cross-coupled Dual-Modular (BCDMR) Flip-Flop

### A. Structure of BCDMR FF

The BCDMR FF in Fig. 4 [3] is developed to mitigate the vulnerability against the SET pulse from the master part on the C-element and weak keepers to duplicate C-elements. The SET pulse on the C-element only influences one of slave latches.

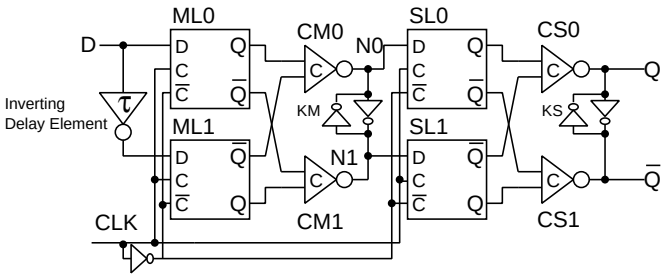



Fig. 4. BCDMR (Bi-stable Cross-coupled Dual-Modular ) FF.

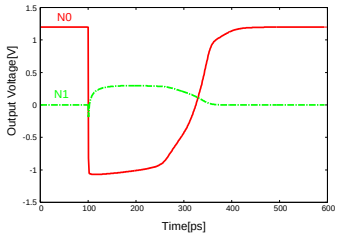



Fig. 5. Effect of SET pulse at N0 to N1 in the BCDMR FF by circuit-level simulation.

The weak keeper is renamed just the keeper. It does not have to be weak because the two C-elements rewrite the keeper complementary from two nodes. Fig. 5 shows a circuit-level simulation result when a particle hit on the node N0 in the BCDMR structure. The node N0 is completely flipped, while the node N1 is almost stable. The error pulse on N1 is only captured by one of slave latches (SL0). Thus the BCDMR FF is very robust to a SET pulse on the C-element. Compared with the original BCDMR structure in [3], the delay element $\tau$ is inverted. Two master/slave latches stores opposite values. It is mainly to enhance the symmetry of the schematic and layout structures.

A SET pulse on the C-element inverts a slave latch when it is injected across the negative edge of CLK (P3 in Fig. 1). But it does not perturb the

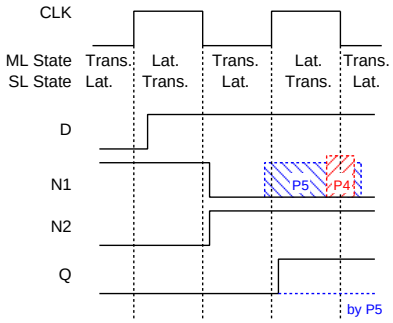



Fig. 6. SET pulse on the C-element that perturbs the output Q.

TABLE I
AREA, DELAY, POWER AND AREA-DELAY-POWER (ADP) PRODUCT OF REDUNDANT FFS NORMALIZED BY THOSE OF D-FF

| | BISER | BCDMR | TMR |
|---|---|---|---|
| Area | 2.74 | 2.84 | 3.47 |
| Delay | 1.56 | 1.38 | 1.39 |
| Power | 2.27 | 2.29 | 2.70 |
| ADP | 9.70 | 8.97 | 13.0 |

output Q if the width of the pulse is not so long as in P4 in Fig. 6. The output Q is already flipped by the positive edge of CLK just before P4. Thus the keeper in the slave latch KS already stores the correct value before P4 is injected. The SET pulse P4 actually flips SL0, while the output of CS0 does not changes. The output Q stays 0 if a SET pulse is enough long like P5 crossing both the positive and negative edges of CLK. That possibility, however, is very low due to the following two reasons.

1) The output Q is only invalid when the input D changes just before the SET pulse. If D is stable, the SET pulse P5 does not perturb Q since KS already stores the correct value.
2) Longer pulses are very rare. Assuming the clock frequency is 1 GHz, an SET pulse over 500 ps may cause an error. From the measurement results in [8], pulse distributions are different with the density of tap cells (substrate or well contacts) which stabilize well potential. The pulses over 500 ps are 12% and 1.0% of the total with the distances of tap cells of 28 $\mu$m and 5 $\mu$m, respectively. The density of tap cells can drastically reduce longer SET pulses.

If we assume that the average switching activity of FFs is 10% and the tap distance is 5 $\mu$m, the possibility to collapse the BCDMR FF by SET pulses at 1 GHz (1,000 ps) equivalent to the longest SET pulse from the measurement can be roughly computed by the following equation. $E_{\mathrm{BCDMR}} =$ [Switching Activity] $\times$ [Pulse rates $>$ 500 ps] $\times$ [Possibility crossing pos. and neg. clk edges.] $= 10\% \times 1.0\% \times \frac{500\ \mathrm{ps}}{1000\ \mathrm{ps}} = 0.05\%$

The possibility of 0.05% (=2000x) becomes the upper bound of the error resiliency of the BCDMR FF caused by an SET pulse injected to slave latches compared with D-FFs.

Table I shows area, delay, power and area-delay-power (ADP) product of the BISER, BCDMR and conventional TMR as in Fig. 8 normalized by those of D-FF. As for area and power, BCDMR is slightly worse than BISER. But BCDMR achieves the smallest ADP product of all.

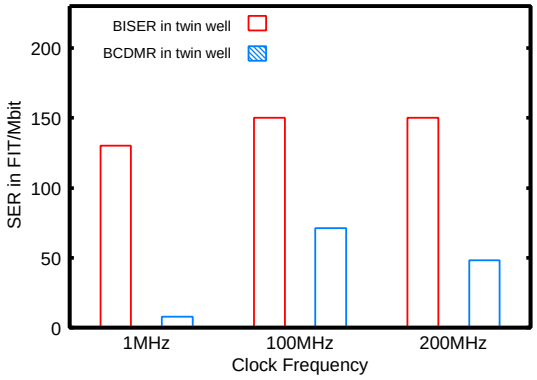



Fig. 7. SERs in FIT/Mbit by the neutron irradiation results of the DMR FFs of the layout in Fig. 12.

TABLE II
SERS IN FIT/MBIT BY THE NEUTRON IRRADIATION RESULTS OF THE BISER AND BCDMR FFS OF THE LAYOUT W/O CONSIDERING MCUS AS SHOWN IN FIG. 12.

| | Clock Freq. | | |
|---|---|---|---|
| | 1 MHz | 100 MHz | 200 MHz |
| BISER FFs | 130 | 150 | 150 |
| BCDMR FFs | 8 | 71 | 48 |
| D-FFs | 1,031 (no clock is applied) | | |

### *B. Experiment Results from the Layout without considering MCUs*

Fig. 7 and Table II shows the error rates in FIT/Mbit by the high-energy broad-spectrum neutron source at RCNP (Research Center for Nuclear Physics), Osaka University[10]. The average accelerated factor is $3.8 \times 10^8$x of the ground level of Tokyo. The SER values in FIT/Mbit are converted to those at the ground level. DUTs (Device Under Tests) including 30,240$\times$13-bit FFs in the twin-well structure were exposed to the neutron beam for 100 minutes. It reveals that SER of D-FFs is 1,031 FIT/Mbit which is almost same as those of SRAMs. But SERs of BISER and BCDMR are almost 1/10 of the D-FFs and has almost no frequency-dependence. We assume that the reason why the redundant FFs are not insensitive is the

MCU between redundant components. These redundant FFs malfunction if two of three memory elements (two latches and one keeper) are flipped. High-energy neutrons from the high-energy broad-spectrum neutron beam has higher possibility of MCUs than alpha particles. To enhance error resilience of the redundant FFs, MCUs on redundant components must be removed.

## IV. Layout Structure to Avoid MCUs in Redundant FFs

The neutron irradiation results reveal that MCUs in redundant FFs are a dominant factor in a current deep-submicron process. To protect redundant latches or FFs from MCUs, the group of circuit components that cause an upset must be placed as far apart as possible. Hereafter, we call them critical components. Firstly we explain the definition of the critical components using TMR FFs. Then the revised layout structures are introduced to avoid MCUs in redundant FFs.

### A. Critical Components in Redundant FFs

Redundant FFs are very robust to soft errors if redundant components do not flip at the same time. Due to the aggressive process scaling, redundant components are placed very close to one another. Fig. 8 shows a general TMR FF composed of master/slave parts and a voter. If the two latches in the master or slave part are flipped at the same time, the voter produces a wrong value as shown in red characters in Fig. 8. If the flipped components are located in different parts, the voter remains unchanged. Fig. 9 and 10 show two floorplans of TMR. The upper one places slave and master parts side-by-side separately, while the lower one interleaves latches in both parts. When a particle hits on a latch, the nearby latch has the highest possibility to be flipped at the same time. If the flipped latches belong to the other part as in Fig. 10, the voter never produces a wrong value. It is better to interleave master and slave latches in order to prevent MCUs between two latches in the same part. In the TMR FF, a pair of latches in the same part becomes a critical component.

Table III shows the MCU rates of a non-redundant D-FF array by spallation neutron irradiation, in which all FFs are adjacently placed as in

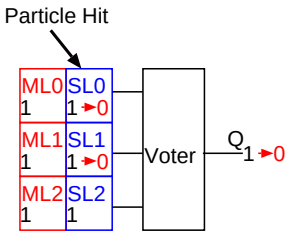



Fig. 8. General TMR FF structure.

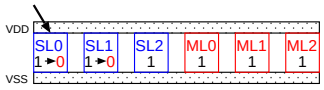



Fig. 9. Floorplans of TMR w/o considering MCUs.

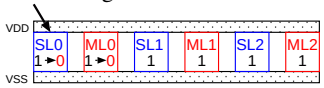



Fig. 10. Floorplans of TMR to avoid MCUs by interleaving

TABLE III
MCU/SEU Ratio in n/Mbit/h of Master and Slave Latches in the D-FFs

| Latch | Min. Dis. | # SEUs | # MCUs | #M/#S |
|---|---|---|---|---|
| Master | 0.73 $\mu$m | 541 | 88 | 16% |
| Slave | 1.03 $\mu$m | 493 | 19 | 3.8% |

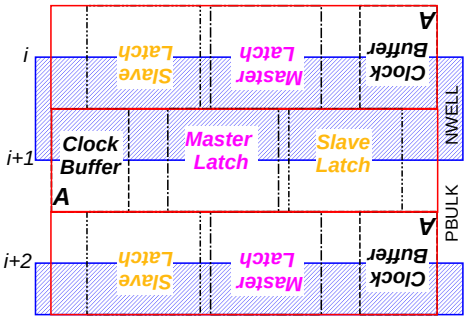



Fig. 11. Floorplan of the non-redundant D-FF array to measure MCU/SEU rates.

Fig. 11. Master latches are placed perpendicularly with the distance of 0.73 $\mu$m, while slave latches are placed diagonally with the distance of 1.03 $\mu$m. Note that these distances are between NMOS transistors on the P-bulk. Although the difference of distance is 0.3 $\mu$m, the MCU rates are 16% and 3.8% respectively. These measurement results reveal that the MCU rate heavily depends on the distance between components. It is better to place critical components as far apart as possible to avoid MCUs. Uemura et. al. reported that the canceling area to separate critical components enhances SER immunity in the DICE latch [11].

### B. Layout Structure to Avoid All Possible MCUs

If two redundant latches are flipped in the BCDMR FF, its output Q is flipped and becomes wrong. If one of latches and the keeper

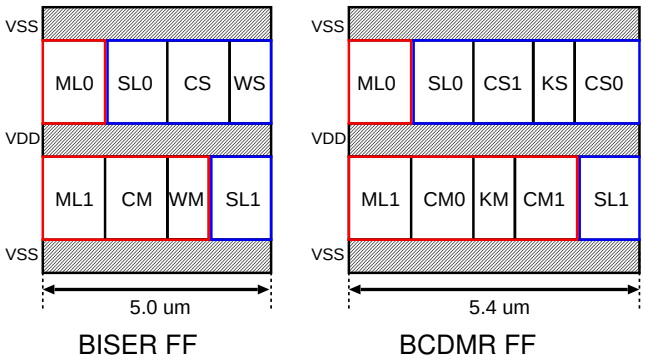



Fig. 12. Floorplan of the BISER and BCDMR FFs considering only MCUs between two latches in the master or slave part.

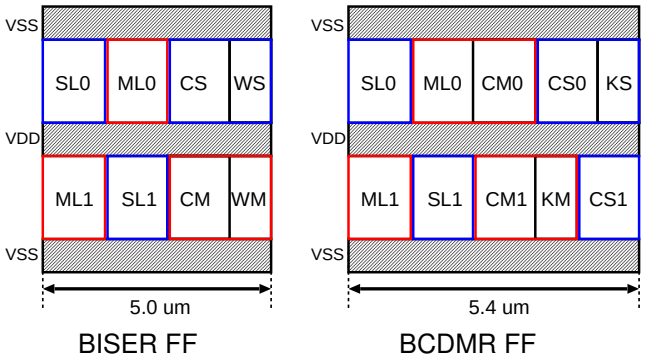



Fig. 13. Revised floorplans of the BISER and BCDMR FFs to Avoid MCUs between All Possible Critical Components.

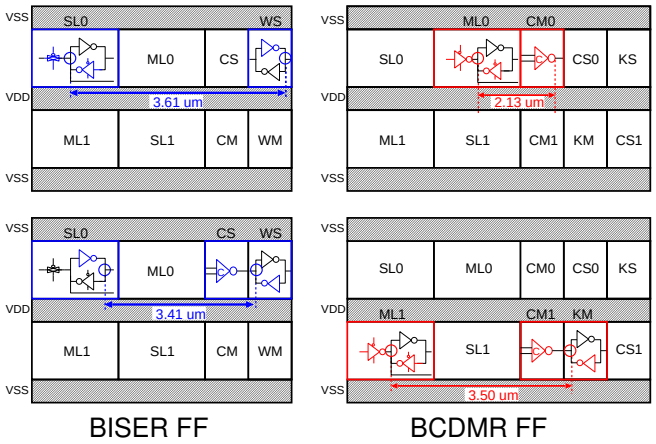



Fig. 14. Distances of critical components when Q=0 (Upper) Q=1 (Lower).

(e.g. ML0+KM or SL0+KS in Fig. 4) are flipped simultaneously by an MCU, Q is also flipped. In order to avoid an MCU, these critical components must be place as far apart as possible.

As for two latches in the master or slave part, the double-height cell structure[11] is very effective. Fig. 12 shows the floorplan of the BISER and BCDMR FFs considering only MCUs between two latches in the master or slave part. All components are placed in two rows to share N-well (PMOS transistors) regions. Since the sensitive area of PMOS transistors is much smaller than that of NMOS transistors[1], [12], the double-height cell sharing N-well regions is much stronger against soft errors than that sharing P-well (NMOS transistor) regions. The experimental results already shown in Fig. 7 are obtained from the floorplans in Fig. 12. As already mentioned in the previous section, SERs of redundant FFs (BISER and BCDMR) are 1/10 of the non-redundant FFs. It is mainly because we just take care of MCUs among two latches in the same part. If one of two master or slave latches is flipped, the C-element and the keeper become very vulnerable. If charge is simultaneously collected in the C-element or the keeper while one of latches is flipped, the keeper is also flipped. Then the FF is upset. In the floorplan of Fig. 12, master or slave latches, the C-elements and the keepers are placed very closely by the distances between NMOS transistors of 0.77 $\mu$m in the BCDMR and 1.54 $\mu$m in the BISER. The distance of 0.77 $\mu$m of the BCDMR is almost same as the master latches in Fig. 11. Thus the floorplan in Fig. 12 causes such a simultaneous flip (an MCU) as in the same manner in the D-FF array.

TABLE IV
MINIMUM DISTANCES BETWEEN CRITICAL COMPONENTS. (Q=0)

| Floorplan | Fig. 12 | Fig. 13 | Ratio |
|---|---|---|---|
| BISER | 1.54 $\mu$m | 3.61 $\mu$m | 2.34 |
| BCDMR | 0.77 $\mu$m | 2.13 $\mu$m | 2.76 |

Fig. 13 shows the revised floorplan of the BISER and BCDMR FFs in which latches, C-elements and keepers are placed separately as far apart as possible. The combinations of critical components are different depending on the value stored in the FF. If the BISER and BCDMR FFs store zero (Q=0), the shortest distances between critical components in NMOS transistor regions are 3.61 $\mu$m and 2.13 $\mu$m respectively as shown in Fig. 14 (Upper). They become 3.41 $\mu$m and 3.50 $\mu$m as in Fig. 14 (Lower) if they store one (Q=1). These distances are much longer when compared with the old floorplan. Table IV compares minimum distances between critical components for the old and revised floorplans when Q=0. The minimum distances of the revised floorplans are over 2x wider than those of the old ones. By placing critical components as far apart as possible, the possibility of MCUs can be reduced.

| | |
|---|---|
| Process | 65 nm bulk CMOS |
| Chip Size | 4 mm×4 mm |
| Package | QFP208 |

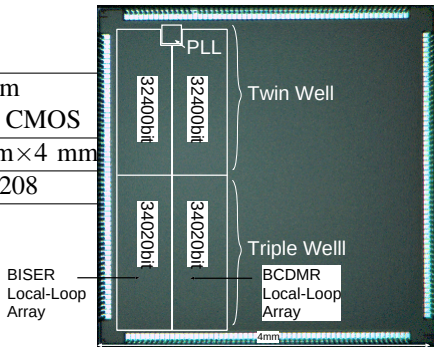



Fig. 15. Chip micrograph fabricated in a 65 nm process.

Experimental results are shown in the next section by neutron irradiations.

Seifert proposes hardened sequential elements based on DICE latches by inserting dummy gates between vulnerable transistors[13]. By paying 10% area overhead, the SER is reduced by 3.8x. Compared with two floorplans in Fig. 12 and 13, there is no area overhead since we interchange components to maximize the distance between critical components.

We ignore contributions of PMOS transistors for the critical components. The minimum distances of critical components in PMOS transistor regions are almost equivalent in the old and revised floorplans. For example, they are 0.72 $\mu$m and 0.66 $\mu$m in the old and revised ones. Even if the distance of critical components in PMOS transistor regions are almost equivalent, SERs of the revised floorplan are considerably decreased as shown in the next section. It reveals that the contribution of PMOS transistors for SERs is much smaller than that of NMOS transistors.

## V. Experimental Results

We have fabricated a 65 nm chip including BISER and BCDMR FFs arrays on twin-well and triple-well structures. Fig. 15 shows a chip micrograph which contains four arrays and a PLL (Phase Locked Loop) in the left half. There are two arrays of BISER and BCDMR FFs with 32,400 bit in the upper half (twin-well), while other two arrays with 34,020 bit are placed in the bottom half (triple-well).

In order to measure error rates while applying clock signals, 9 FFs forms a loop structure to keep flipped values[3]. The high-energy broad spectrum neutron-beam irradiations were carried out at RCNP of Osaka University. Experimental setups are same as those in Section. III-B except for the average acceleration factor, $3.67\times10^8$.

TABLE V
Number of measured upsets from the layout in Fig. 13 by 50 min. neutron irradiation (Q=0).

| | well | Clock Freq.[MHz] 1 | 10 | 100 | 300 |
|---|---|---|---|---|---|
| BISER | twin | 2 | 3 | 5 | 24 |
| | triple | 1 | 3 | 6 | 11 |
| BCDMR | twin | 0 | | | - |
| | triple | 3 | 2 | 2 | - |

TABLE VI
SERs in FIT/Mbit by the neutron irradiation computed from TableV (Q=0).

| | well | Clock Freq.[MHz] 1 | 10 | 100 | 300 |
|---|---|---|---|---|---|
| BISER | twin | 18 | 26 | 44 | 212 |
| | triple | 10 | 28 | 56 | 104 |
| BCDMR | twin | $< 9$ (No error) | | | - |
| | triple | 29 | 19 | 19 | - |

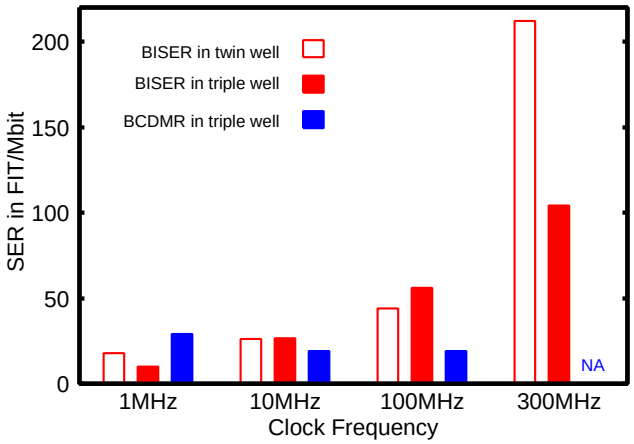



Fig. 16. SERs in FIT/Mbit by the neutron irradiation results of the DMR FFs of the layout in Fig. 13 (Q=0).

To increase the number of observed errors, 12 DUTs were measured at the same time. All FFs are initialized to be 0 before neutron irradiation. The irradiation time of each frequency is 50 minutes. Table V and VI show the actual number of observed errors in 50 minutes and SERs in FIT/Mbit respectively. Fig. 16 shows the soft error rates in FIT/Mbit. Note that the BCDMR FFs cannot work correctly at 300 MHz due to some clock signal wiring issue.

In the BISER FF, the SER is increasing according to the clock frequency since a SET pulse on the C-

element is easily captured by both of the redundant latches. It reveals that MCUs are dominant in the conventional floorplan in Fig. 12, which shows no frequency dependence. The SER on the twin well is twice larger than that on the triple well. We assume that the number of SET pulses becomes smaller in the triple well because of the shallow p-well depth.

We observed no upset on the BCDMR FFs in the twin-well structure. The SER is computed to be below 9 FIT/Mbit, which is over 100x stronger than the non-redundant D-FF with 1,031 FIT/Mbit as in Table 7. On the other hand, several upsets were observed in the triple-well structure. Unlike BISER, BCDMR is insensitive to the SET pulse on the C-element if there is no upset in the redundant latches. We assume that the parasitic bipolar effect[14] in p-well is dominant in the triple-well structure since deep n-well isolates p-well. The bipolar effect flips critical components simultaneously in the triple well structure.

## VI. Conclusion

We propose a layout structure to avoid MCUs on the redundant flip-flops. The redundant FFs such as the BISER FF or the DICE latches are very sensitive to MCUs. If two sequential elements are flipped simultaneously, FFs or latches are upset. A layout structure of the rad-hard BCDMR FF is proposed by placing critical components separately as far apart as possible. The critical components are placed separately to avoid MCUs. We have fabricated a 65 nm chip including over 30 kbit redundant FFs in the twin- and triple-well structures. The revised floorplan to prevent MCUs in the twin well has no error during the high-energy broad-spectrum neutron irradiations in 50 minutes. It means that the SER is lower than 9 FIT/Mbit. But some errors were observed in the triple well, which is mainly caused by the parasitic bipolar effect.

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