Intrinsic Vulnerability to Soft Errors and a Mitigation Technique by Layout Optimization on DICE Flip Flops in a 65 nm Bulk Process

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***Abstract*—We found that specific pairs of PMOS and NMOS transistors in DICEFF become sensitive to soft errors by device simulations. We propose several layout structures that can improve soft error tolerance with additional 39-46% area overhead. We evaluated soft error tolerance of a DFF and DICEFFs in a 65 nm bulk process by heavy ions. Our experimental results showed that the DICEFF has more than 300x better soft error tolerance than the DFF by Kr (LET 40.3 MeV·cm^2/mg) irradiation when supply voltage is 1.2 V, and the DICEFF has only 7x better soft error tolerance than the DFF when suplly voltage is 0.6 V. However, the proposed DICEFF has 58x better soft error tolerance than the DFF when suplly voltage is 0.6 V. DICEFF has so many sensitive pairs and lower soft error tolerance as supply voltage decreases that cannot be applied to highly-scaled process technologies.**

***Index Terms*—single event effect, soft error, heavy ion, bulk process, flip-flop, device simulation.**

I. Introduction

Reliability issues such as radiation-induced soft errors become more serious with technology downscaling [1] [2] [3] [4]. Soft errors are one of temporal failures that upset stored values in storage elements such as flip flops (FFs) or SRAMs caused by neutrons and alpha particles in the terrestrial region and by heavy ions in outer space. To improve the reliability, FFs or latches must be protected from soft errors [5] [6]. When a radiated particle hits close to a logic gate, its output node is perturbed, which is called a single event transient (SET) pulse. A single event upset (SEU) occurs when an SET pulse flips a storage element. In the circuit level, several redundant FFs such as Triple Modular Redundancy (TMR) [7], Dual Interlocked Storage Cell (DICE) [8] [9] and a Cascode Voltage Switch Logic (CVSL) based radiation hardness by design (RHBD) cell named Quatro [10] [11] have been proposed for effective countermeasures. DICE is strong against an upset on a single node, but weak to simultaneous upsets on two or more nodes. Soft error resilience highly depends on layout structures [12] [13]. Effective countermeasures called LEAP are proposed for the single height cell structure, in which NMOS and PMOS are each arranged in a single column [14]. However, LEAP design needs more metal layer and pitch for the cell routing [15]. It was shown that DICE designed double height cell structure has low radiation tolerance at a specific stored value and a clock state from the measurement results [16].

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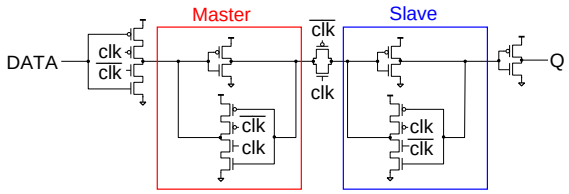

Fig. 1. Standard flip flop.

In this paper, we identify the root cause of vulnerability in DICEFFs to a particle hit with high energy by device simulations and propose several new layout structures according to the template of a 9-pitch standard cell library on the 65 nm process. We also investigated soft error tolerance of those layouts depending on supply voltage by heavy ions. Previous measurement results of DICEFFs in a 65nm bulk process by heavy ions irradiation are shown in Section II. Section III explains analysis of an upset mechanism by device simulations. Section IV proposes new layout structures by separating critical pairs of PMOS and NMOS transistors. Section V explains experimental results by heavy-ion irradiation and discussion. We conclude this paper in Section VI.

II. Previous Experimental Results [16]

Figure 1 shows a standard FF called the D-type FF (DFF). It has no tolerance against soft errors. Figures 2 and 3 show a schematic and a layout pattern of the DICEFF for measurement. The DICE structure mitigates soft errors by duplicating latches. The input and output signals of these half C-elements (HCE) have cross-coupled connections to be automatically recovered from a flip on a single node. A test chip was fabricated in a 65 nm bulk process in order to evaluate soft error tolerance. We evaluated soft error tolerance by heavy ion irradiation. Heavy ion irradiation tests were conducted by Ar and Kr ions at Takasaki Ion accelerators for Advanced Radiation Application (TIARA) in order to investigate soft error tolerance. In outer space, most of heavy ions have Linear Energy Transfer (LET) less than 60 MeV·cm^2/mg [17]. Thus, we chose Ar (LET : 15.4 MeV·cm^2/mg) and Kr (LET : 40.1 MeV·cm^2/mg) for measurement. Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1) and supply voltage (V_{dd}) was 1.2 V. Heavy ions were irradiated perpendicular to the test chip under the four DATA and CLK states. Cross Section (CS) is used in order to evaluate soft error tolerance, which means an area

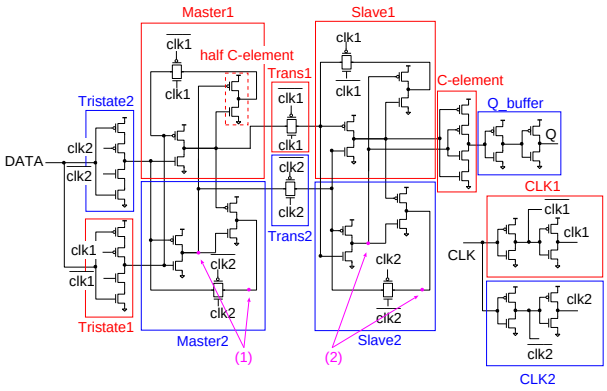

Fig. 2. Dual interlocked storage cell flip flop (DICEFF) for measurement in 2019 [16].

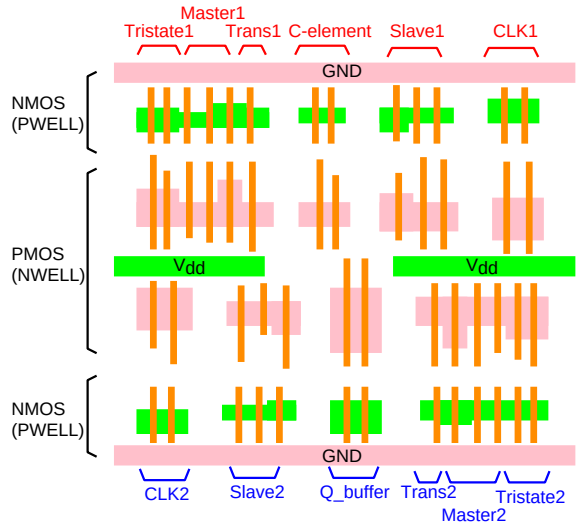

Fig. 3. Simplified layout structure of DICEFF for measurement in 2019 [16].

of upsets when a particle passes through a circuit block. Soft error tolerance becomes stronger if CS becomes smaller [18].

Figure 4 shows the experimental results of the CSs by Kr irradiation with error bars of 95% confidence. Note that there was no error in DICEFF by Ar irradiation. The average CS of DICEFF is 1/167 as big as that of DFF. At (DATA, CLK) = (0, 0), CS of DICEFF is only 1/7 as big as that of DFF. The DICEFF has errors only at (DATA, CLK) = (0, 0). On the other conditions, the DICEFF has no error. The DFF has almost equivalent error rates at all four static conditions. The layout structure of the DICEFF is optimized in order to place critical transistors as far apart as possible. Therefore, in contrast to the DICEFF, which we used in the experiment has a fatal unknown factor of the weakness to soft errors at (DATA, CLK) = (0, 0).

In addition, we examined soft-error tolerance depending on V_{dd} when (DATA, CLK) = (0, 1). We chose this state because the number of errors at the condition is the largest of all. Experiments were carried out at V_{dd} = 0.6 V, 0.8 V and 1.0 V by Kr irradiation. Figure 5 shows the experimental CSs depending on V_{dd} by Kr with error bars of 95% confidence.

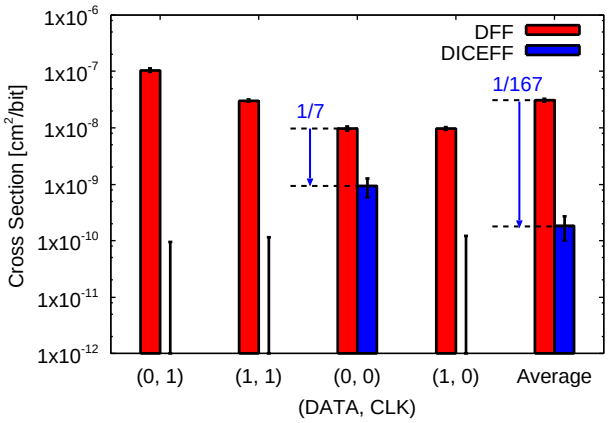

Fig. 4. Experimental results of the CSs by Kr irradiation (There is no error in DICEFF by Ar irradiation).

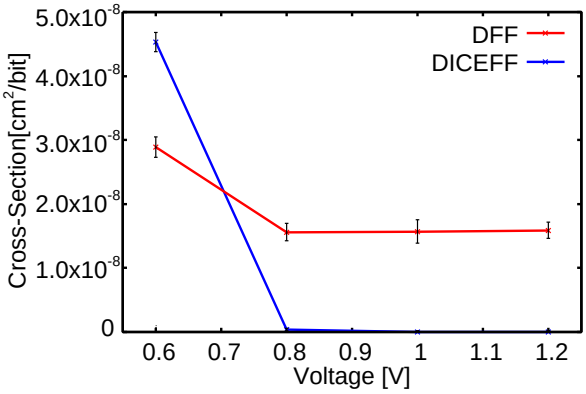

Fig. 5. Experimental results of the CSs by volt.

Both of the DFF and the DICEFF become weaker against soft errors as V_{dd} is lowered. We revealed that the DICEFF becomes weak to soft error when $V_{dd} < 0.8$ V. The DICEFF is less resistant to soft errors than the DFF when the V_{dd} = 0.6 V.

III. Analysis of Upset Mechanism by Device Simulation

We constructed a 3D transistor model to match static characteristics of a SPICE simulation distributed from a fabrication company. Device simulations were conducted under the condition at (DATA, CLK)=(0, 0) when soft errors were observed by the heavy ion irradiation. At CLK = 0, the transmission gates (Trans1 and 2) in Fig. 2 are off. An SEU only happens in the slave latch. We found that the following two pairs of transistors are critical to cause an SEU by device simulations.
1. NMOS and PMOS transistors in different HCEs.
2. PMOS transistors in the transmission gate and the slave latch.
We discuss how these transistors flip DICEFF by device simulations.

A. NMOS and PMOS transistors in different HCEs in the slave latch

Figure 6 shows the device model and circuit structure used in the simulation. Ix stands for a name of inverter, Tx stands

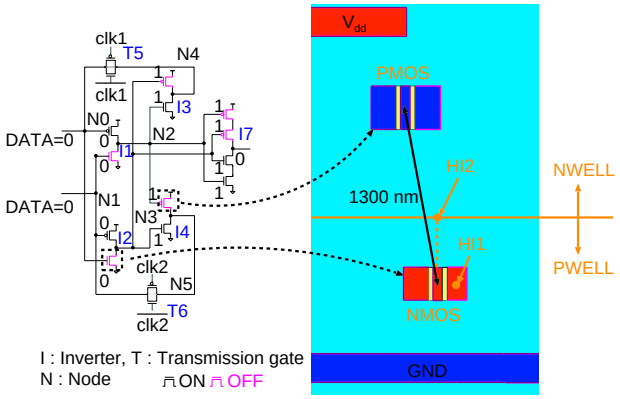

Fig. 6. Circuit diagram of the slave latch and top view of the device model (NMOS and PMOS in the slave latch).

for a name of transmission gate and Nx stands for a name of node. In the fabricated layout structure, all pairs of NMOS transistors in the four HCEs are placed as far apart as possible. But the pair of NMOS and PMOS transistors are closely placed. To reduce simulation time with keeping accuracy, the transistors inside the dotted rectangles are modeled at the device level, the other transistors are modeled at the SPICE level. The layout of the device model is consistent with the layout of the circuit used for the measurement. LET of the irradiated heavy ion is 40.1 MeV·cm^2/mg, assuming Kr and its track radius (r) is computed by Eq. (1) from [19].

$$r\ [\mathrm{nm}] = 7.16765 \times 10^{-3} \times \sqrt{\mathrm{LET}\ [\mathrm{MeV \cdot cm^2/mg}]} \quad (1)$$

Figure 7 shows the voltage waveforms when a heavy ion hits HI1 in Fig. 6. The irradiation point, HI1 is the center of the NMOS drain diffusion region. In this case, the stored value does not upset as shown in Fig 8 showing how DICEFF is recovered by a single node upset. The high impedance node (N3) stores the upset node (N1) as described below. V_{inter} denotes an intermediate voltage between Vdd and ground levels.

1) Heavy ion hits NMOS I2, and then N3 = 1 → 0.
2) When N3 upsets to 0, N0 and N4 = 0 → V_{inter}.
   N1 and N5 become a high impedance but the stored value still sticks to 0.
3) The input of I1 and I2 become 0 and V_{inter} respectively.
   N3 goes back to 1 and N2 remains 1.
4) Both of I3 and I4 inputs are 1.
   N0 and N4 go back to 0.

Figure 9 shows the voltage waveforms when a heavy ion hits HI2 in Fig 6. The irradiation point, HI2 is the intersection on the boundary between PWELL and NWELL and above the center of the NMOS gate terminal to generate electric charge in both PWELL and NWELL. In this case, the stored value upsets according to the state transition as shown in Fig 10. The same state transition occurs not only in the combination of I2 NMOS and I4 PMOS, but also in the combination of I1 NMOS and I3 PMOS.

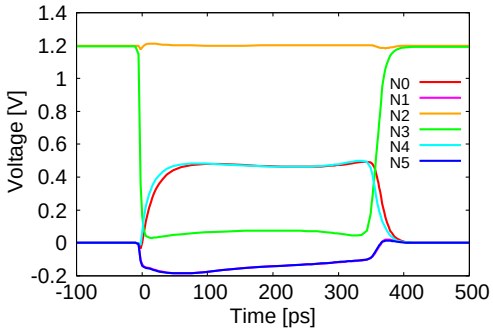

Fig. 7. Voltage waveforms when a heavy ion is irradiated to HI1.

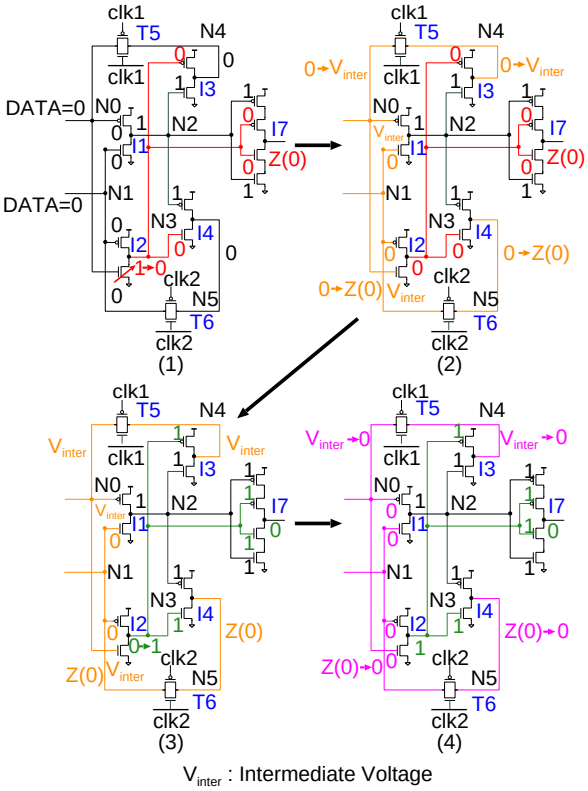

Fig. 8. State transitions when DICEFF recovers.

1) When a heavy ion hits at HI2, charge injected to I2 NMOS upsets N3 (N3 = 1 → 0).
1') The heavy ion hit also upsets N1 and N5 by charge injected at I4 PMOS. N0 and N4 = 0 → V_{inter}.
2) The inputs of I1 and I2 become 1 and V_{inter} respectively.
   N2 upsets to 0 but N3 remains 0.
3) Both of I2 and I3 inputs upsets. Then N0 and N4 upset to 1.

We investigated the critical charge of the master latch and slave latch by circuit simulation. Figure 11 shows simplified block of DICEFF layout structure for measurement in 2019. Master1 and Master2 are separated. Slave 1 and Slave 2 are similarly separated. When CLK = 1, charge is injected into the two places (1). When CLK = 0, charge is injected into the two

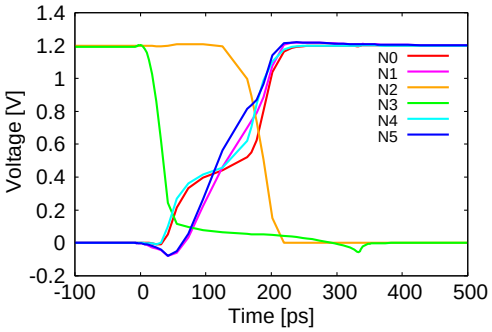

Fig. 9. Voltage waveforms when a heavy ion is irradiated to HI2.

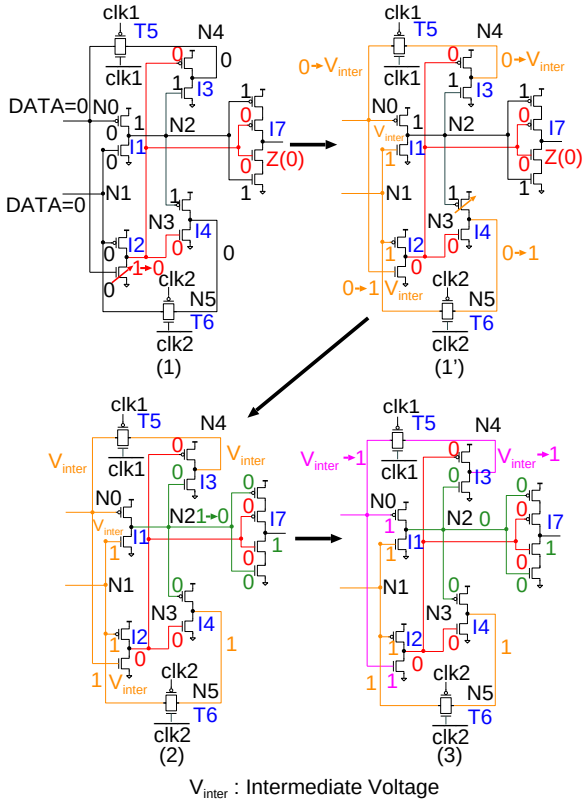

Fig. 10. State transitions when DICEFF upsets due to simultaneous charge injections at NMOS I2 and PMOS I4.

places (2). Table I shows the critical charge for each (DATA, CLK). When (DATA, CLK) = (0, 1), (1, 0), the combination of transistors that are off does not occur SEU, so the critical charge is 100 fC or more. The master latch ((DATA, CLK) = (1, 1)) has the critical charge 1.4 times larger than that of the slave latch ((DATA, CLK) = (0, 0)). When the master latch stores the value (CLK = 1), the transmission gates (Trans1 and 2) are on. Since many elements are connected, the master latch has the larger parasitic capacitance than that of the slave latch.

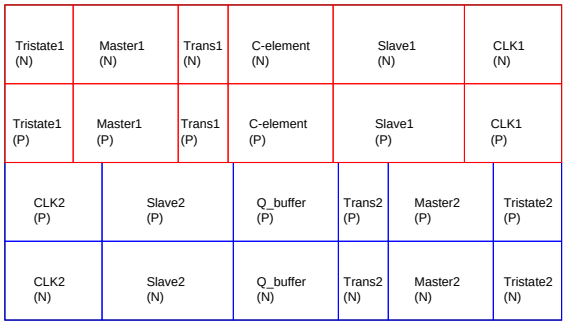

Fig. 11. Simplified block of DICEFF layout structure for measurement in 2019.

TABLE I
CRITICAL CHARGE OF DICEFF MEASURED IN 2019 FOR EACH (DATA, CLK).

(DATA, CLK)	Critical charge [fC]
(0, 1)	>100
(1, 1)	3.4
(0, 0)	2.4
(1, 0)	>100

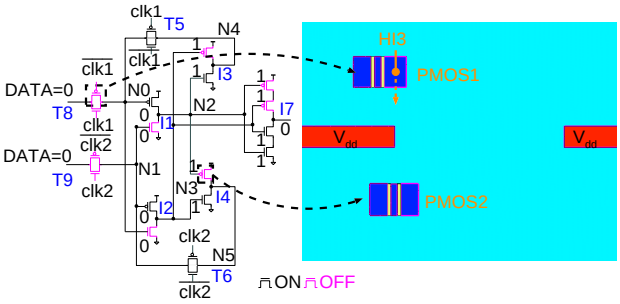

Fig. 12. Circuit diagram of the slave latch and top view of the device model (PMOS in the transmission gate and slave latch).

B. PMOS transistors in the transmission gate and the slave latch

Figure 12 shows a device model and the circuit structure for device simulations. LET of an irradiated heavy ion is 40.1 MeV·cm^2/mg, assuming Kr and its track radius is calculated by Eq. (1). Since drain and source terminals of the transmission gates are not directly connected to GND nor V_{dd}, an SET pulse is generated only by charge collection. On the other hand, in logic gates such as an inverter, body potential can be elevated by a particle hit and then the parasitic bipolar transistor composed of drain, source and body terminals turns on to generate an SET pulse. The irradiation point, HI3 is the center of PMOS1 (transmission gate) drain region. Figure 13 shows the definition of irradiation angles. No upset occurs at ϕ = 0°, but an upset occurs at ϕ = 45°. Figure 14 shows the voltage waveforms when a heavy ion is irradiated at ϕ = 45°. In outer space, heavy ions come from any angle. Those combinations of PMOS and NMOS transistors become a critical pair to cause soft errors.

When two transistors simultaneously collect carriers by a heavy ion hit and all high impedance nodes are wiped out, an SEU easily occurs at DICEFF. The high impedance nodes

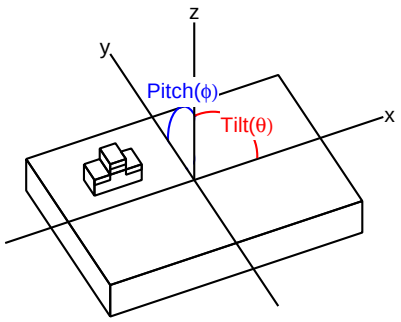

Fig. 13. Definition of irradiation angle.

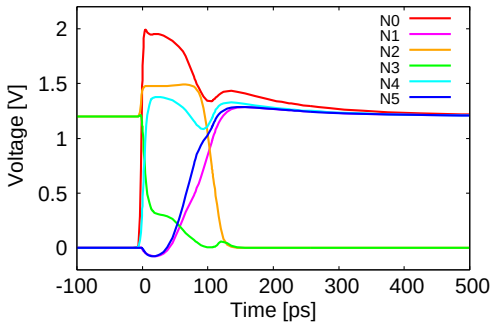

Fig. 14. Voltage waveforms when a heavy ion irradiated to HI3 at ϕ = 45°.

play the important roles to soft error tolerance in DICEFF. The device simulations clearly proves that the DICEFF we measured becomes vulnerable to soft errors due to the simultaneous upsets on the four nodes connected to different HCEs in the slave latch or the four nodes connected to the PMOS transistors in transmission gates and the slave latch. There are 50 pairs of transistors that cause soft errors in DICEFF when they simultaneously turn on.

C. Root cause of increased CS of DICEFF at lower supply voltage

Device simulations were conducted under the condition at (DATA, CLK)=(0, 1) and V_{dd} = 0.6 V when a lot of soft errors were observed by heavy ion irradiation. We focused on PMOS transistors in the master and slave latches. Figure 15 shows the device model and circuit structure for device simulations. LET of the irradiated heavy ion is 40.1 MeV·cm^2/mg, assuming Kr and its track radius is calculated by Eq. (1). The irradiation point, HI4 is the center of the ST2 PMOS (transmission gate) drain region. The irradiation angle is ϕ = 0°. At V_{dd} = 1.2 V, the stored value does not upset as shown in Fig. 16. While at V_{dd} = 0.6 V, the stored value upsets as shown in Fig. 17. At V_{dd} = 0.6V, the amount of increase in the potential of the node connected ST2 is smaller than at V_{dd} = 1.2V. As the amount of charge collected in ST2 decreased, the charge was also collected in MI1. Table II shows threshold LET values of several supply voltages when a heavy ion is irradiated to HI4. Threshold LET decreases as V_{dd} becomes lower. Even in the same circuit, by decreasing V_{dd}, the number of transistor pairs that cause SEU increases.

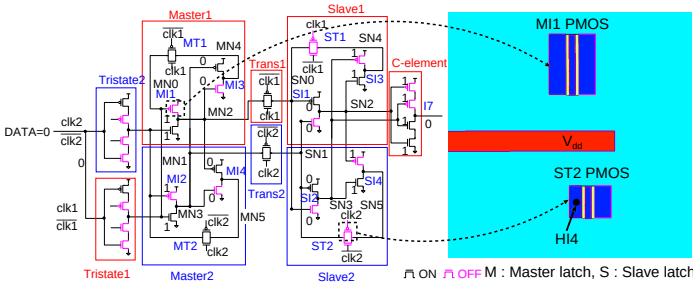

Fig. 15. Circuit diagram of the slave latch and top view of the device model (PMOS in the master and slave latches).

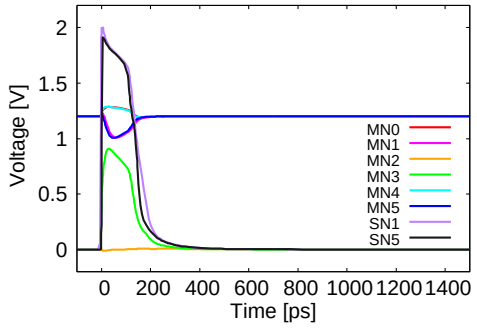

Fig. 16. Voltage waveforms when a heavy ion is irradiated to HI4 at V_{dd} = 1.2 V.

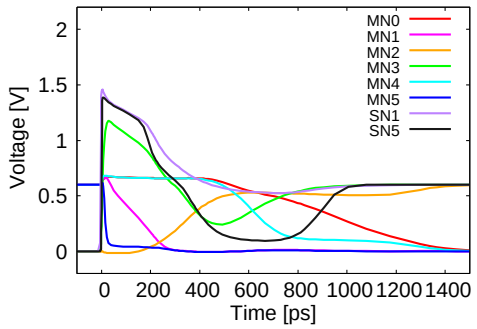

Fig. 17. Voltage waveforms when a heavy ion is irradiated to HI4 at V_{dd} = 0.6 V.

TABLE II
THRESHOLD LET OF EACH V_{dd} WHEN A HEAVY ION IS IRRADIATED TO HI4.

V_{dd} [V]	Threshold LET [MeV·cm^2/mg]
0.6	25
0.8	56
1.0	136
1.2	>200

IV. Examination of Countermeasures by Device Simulation

The discussion so far has been about our DICEFF in Fig. 2, which we measured in 2019, and now we discuss a newly-designed DICEFF in Fig. 18, which will measure in 2020. Compared with Fig. 2, one inverter before the output stage is removed to reduce area and delay time. Due to the circuit change, the condition with the lowest soft error tolerance

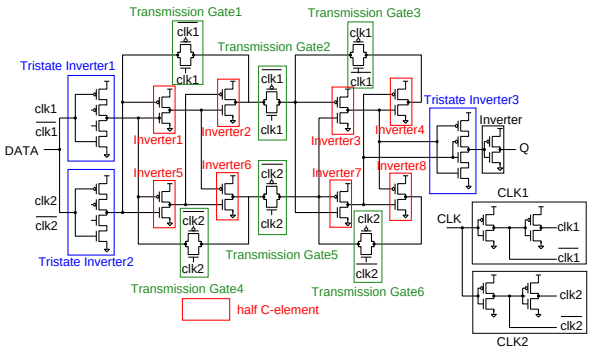

Fig. 18. DICEFF measured in 2020.

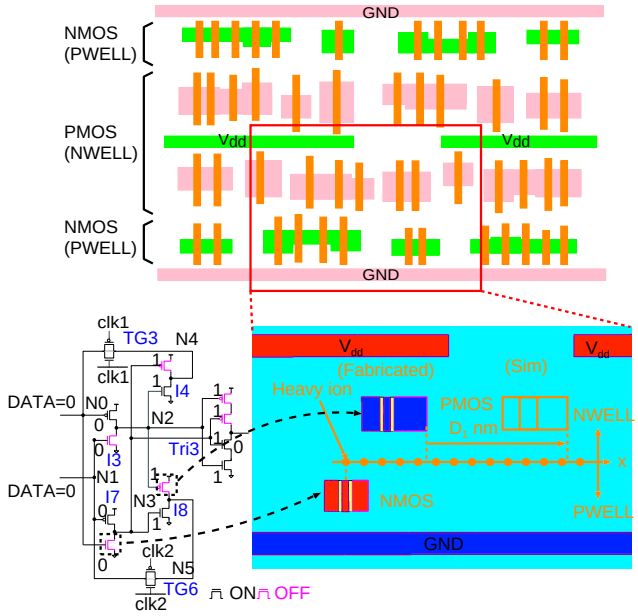

Fig. 19. Simplified layout structure, circuit diagram of the slave latch and top view of the device model used horizontally separation at NMOS and PMOS transistors in different HCEs in the slave latch.

changed from (DATA, CLK) = (0, 0) to (1, 0) .

We performed device simulations to examine radiation tolerance of different layout structures. Since the DICEFF must be embedded to a standard cell library, its cell height is fixed. Transistors in a critical pair can only be moved horizontally to keep the cell height.

A. NMOS and PMOS transistors in different HCEs in the slave latch (I7 NMOS and I8 PMOS)

Device simulations are performed by horizontally shifting PMOS (I8) locations. Irradiation points are moved along the boundary between PWELL and NWELL, to find out the minimum distance D_1 not to occur an upset at any irradiation point. Figure 19 shows the top view of the 3D device model. Soft error occurs in the range of -2250 nm $< D_1 <$ 1250 nm at vertical hit, -2600 nm $< D_1 <$ 2000 nm at θ = 45° hit.

B. PMOS transistors in the transmission gate and the slave latch (TG2 PMOS and I8 PMOS)

Device simulations are performed by horizontally shifting the transmission gate PMOS (TG2) D_2. The irradiation points are always at the center of the PMOS (TG2) drain region. Soft error does not occur at vertical hit and occurs in the range of -1750 nm $< D_2 < 0$ nm at ϕ = 45° hit.

C. PMOS transistors in different HCEs in the slave latch (I4 PMOS and I8 PMOS)

Device simulations are performed by horizontally shifting the transmission gate PMOS (I4) D_3. The irradiation points are always at the center of the PMOS1 drain region. Soft error occurs in the range of -2200 nm $< D_3 < -750$ nm at ϕ = 45° hit.

Figure 20 (a) shows a simplified layout diagram of a standard DICEFF as a reference. Figure 20 (b) shows a layout structure that improves soft error tolerance by separating inverters in the slave latch. Figure 20 (c) shows another layout structure that improves soft error tolerance by separating PMOS and NMOS transistors in I3, I4, I7 and I8. The dotted sky blue arrows indicate a pair of transistors that is tolerant to soft errors up to Kr irradiation by device similations. We designed 6 different layout structures : 3 different well tap shapes of the two proposed layouts (DICEFF2 and DICEFF3). Their layouts were designed according to the template of a 9-pitch standard cell library on the 65 nm process. The cell height of them is doubled in order to decrease the number of metal layers for the cell routing. All designed DICEFFs use only three metal layers for the cell routing. The conventional single-height cell increase the number of routing layers and prolong the total routing length, which have negative impacts on routability and cell performance. NG means 'no guard ring'. The guard ring is an n+ or p+ diffusion layer path to absorb charge generated in the wells pulled down to GND or up to $V_{\rm dd}$. It is effective to suppress fluctuations of the substrate potential close to vulnerable transistors. It is effective to suppress latch-up, but it can also suppress the parasitic bipolar effect. PG (Partial Guard ring) has a separate guard ring only in the vertical direction. PG+ fills a well tap to the empty space in addition to PG. Figure 21 shows the layout structure of DICEFF3PG+. Table III shows the results of delay time, power consumption by circuit simulations at $V_{\rm dd}$= 1.2 V and area of the proposed DICEFFs considering parasitic components extracted from layout patterns. D-Q delay is the minimum delay time from D to Q including setup time before a clock edge. All values are normalized to those of DICEFFNG1. The values in parentheses are normalized to those of DICEFF2NG. The power consumption of the proposed FFs are 12-14% larger than that of DICEFFNG1. The delay times of the proposed FFs are 15-16% longer than that of DICEFFNG1. The areas of the proposed FFs are 39-46% larger than that of DICEFFNG1. The overheads of the proposed FFs are less than 5%.

V. Experimental Results

A test chip was fabricated in a 65 nm bulk process in order to evaluate soft-error tolerance. Four chips are mounted in

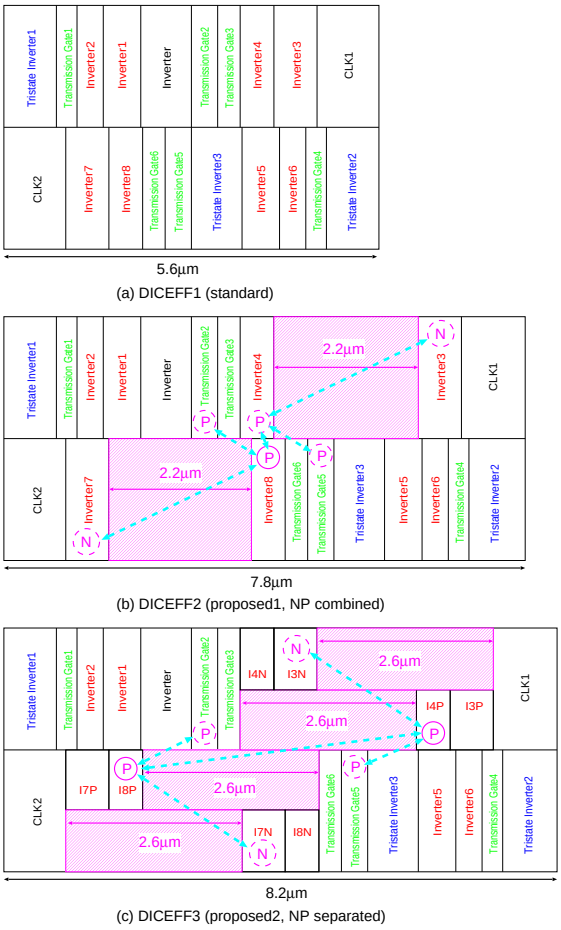

Fig. 20. Simplified block of conventional and proposed layout structures.

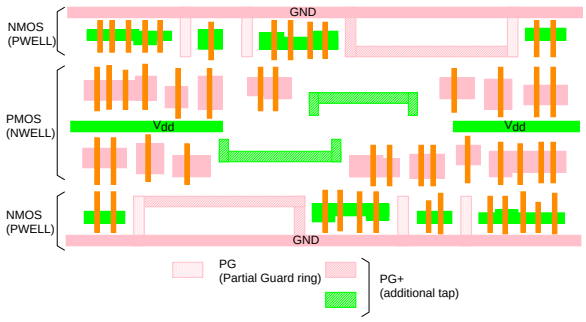

Fig. 21. Simplified layout structure of DICEFF3PG+ (Partial Guard ring + well tap in empty space).

a package. The test chip contains 12,064-bit DFFs, 14,416-bit each DICEFFs. All FFs are connected in series to form a shift register. We evaluated soft error tolerance by heavy ion irradiation. Heavy ion irradiation tests were conducted by Ar and Kr ions at Takasaki Ion accelerators for Advanced Radiation Application (TIARA). We used Ar (LET : 15.8 MeV·cm^2/mg) and Kr (LET : 40.3 MeV·cm^2/mg) for measurement. Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1) and V_{dd} = 0.6 V, 0.8 V, 1.0 V and 1.2 V. Each irradiation time was 30 sec, and irradiation was repeated for 5 times per conditions.

TABLE III
SIMULATION RESULTS OF AREA, D-Q DELAY, POWER AND NUMBER OF TRANSISTOR OF EACH FF AT V_{dd}= 1.2 V. ALL VALUES ARE NORMALIZED TO THOSE OF DICEFFNG1. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF DICEFF2NG.

FF	Power	D-Q delay	Area
DICEFFNG1	1.00	1.00	1.00
DICEFFPG1	1.00	1.00	1.00
DICEFF2NG	1.12 (1.00)	1.15 (1.00)	1.39 (1.00)
DICEFF2PG	1.12 (1.00)	1.15 (1.00)	1.39 (1.00)
DICEFF2PG+	1.12 (1.00)	1.15 (1.00)	1.39 (1.00)
DICEFF3NG	1.14 (1.02)	1.15 (1.00)	1.46 (1.05)
DICEFF3PG	1.14 (1.02)	1.15 (1.00)	1.46 (1.05)
DICEFF3PG+	1.14 (1.02)	1.16 (1.01)	1.46 (1.05)

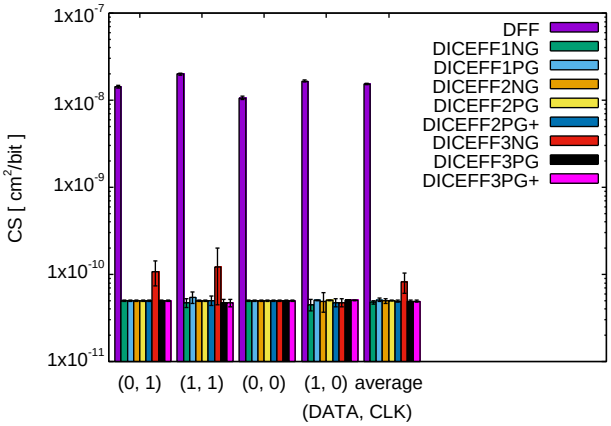

Fig. 22. Experimental results of CSs by Kr irradiation at V_{dd} = 1.2 V.

The irradiation procedure was as follows. The measurements for V_{dd} = 1.2 V were skipped 3) and 5).

1) Initialize serially-connected FFs by all 0 or all 1 (V_{dd} = 1.2 V).
2) Stabilize CLK to 0 or 1 (V_{dd} = 1.2 V).
3) Decrease V_{dd} to 0.6 V, 0.8 V or 1.0 V.
4) Expose heavy ions.
5) Increase V_{dd} to 1.2 V.
6) Read out stored data of FFs (V_{dd} = 1.2 V).
7) Count the number of upsets.
8) Repeat 1) - 7) for four (DATA, CLK) conditions and four supply voltages.

The CS of all DICEFF by Ar irradiation were the error bar range and the CSs were less 1×10^{-10} cm^2/bit. The CS of the DFF was about 1×10^{-8} cm^2/bit. The DICEFF has more than 140x better soft error tolerance than the DFF by Ar irradiation. Figure 22, 23, 24 and 25 show the experimental results of the CSs by Kr irradiation with error bars of 95% confidence. Table IV shows the value of the average CS normalized by DFF. The average CS of all DICEFF without DICEFF3NG is 1/300 as big as that of DFF at V_{dd} = 1.0 V and 1.2V. The average CS of DICEFF1 and DICEFF2 is 1/7 or 1/8 as big as that of DFF, but the average CS of DICEFF3PG+ is 1/58 as big as

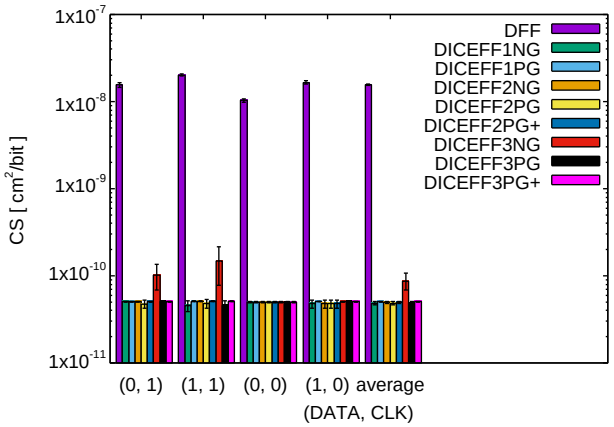

Fig. 23. Experimental results of CSs by Kr irradiation at V_{dd} = 1.0 V.

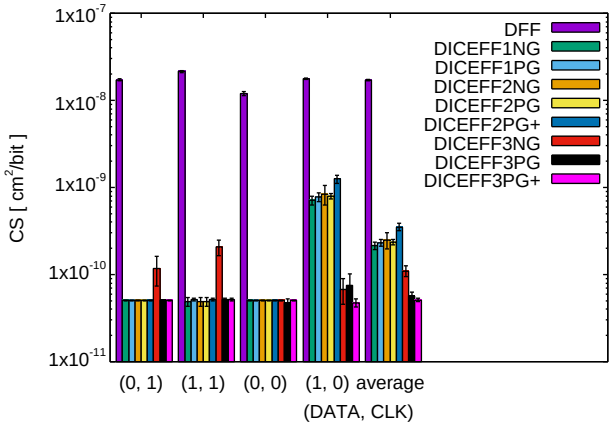

Fig. 24. Experimental results of CSs by Kr irradiation at V_{dd} = 0.8 V.

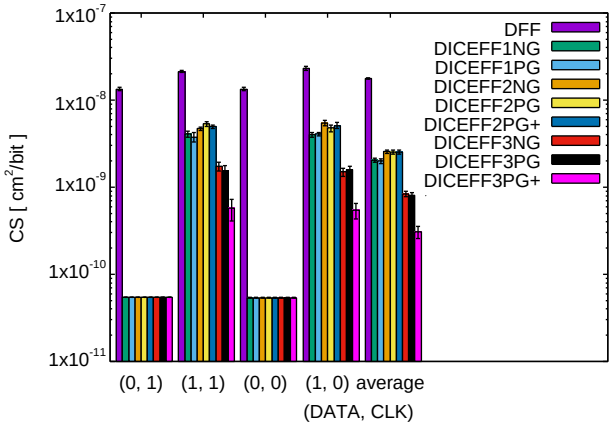

Fig. 25. Experimental results of CSs by Kr irradiation at V_{dd} = 0.6 V.

that of DFF at V_{dd} = 0.6 V. The average CS of DICEFF3PG+ is 1/7 as big as that of the regular DICEFF (DICEFF1NG) at V_{dd} = 0.6 V. The DICEFF has errors at V_{dd} = 0.8 V when (DATA, CLK) = (1, 0). The DICEFF has errors at V_{dd} = 0.6 V when (DATA, CLK) = (1, 0) and (1, 1). The DICEFF has the lowest soft error tolerance at (DATA, CLK) = (1, 0). This result agrees with the result in Table I.

TABLE IV
EXPERIMENTAL RESULTS OF THE AVERAGE CSS BY KR IRRADIATION. THE CSS ARE NORMALIZED TO THAT OF DFF.

FF	CS			
	V_{dd} = 1.2 V	1.0 V	0.8 V	0.6 V
DFF	1/1.00	1/1.00	1/1.00	1/1.00
DICEFF1NG	1/321.50	1/325.05	1/79.17	1/8.68
DICEFF1PG	1/301.37	1/310.89	1/73.39	1/8.90
DICEFF2NG	1/309.86	1/315.26	1/68.95	1/6.95
DICEFF2PG	1/308.00	1/325.05	1/72.46	1/6.98
DICEFF2PG+	1/312.37	1/315.26	1/48.72	1/7.01
DICEFF3NG	1/188.26	1/179.63	1/155.45	1/21.22
DICEFF3PG	1/312.37	1/320.41	1/304.27	1/21.95
DICEFF3PG+	1/312.37	1/310.89	1/334.64	1/58.17

VI. Conclusion

In the previous experimental results measuring radiation tolerance of the DFF and DICEFF in the 65nm bulk process by heavy ions, the DICEFF has no error by Ar irradiation. The DICEFF has 167x better soft error tolerance than the DFF by Kr irradiation, but the DICEFF has only 7x better soft error tolerance than the DFF at (DATA, CLK) = (0, 0) while the DICEFF has no error at the other three (DATA, CLK) states. The DICEFF also becomes less resistant to soft errors than the DFF at (DATA, CLK) = (0, 1) when the V_{dd} = 0.6 V. We investigated the root cause of the low soft error tolerance by device simulations. At NMOS and PMOS transistors in different HCEs in the slave latch, two nodes are upset simultaneously by a single heavy ion hit and then SEU occurs. At PMOS transistors in the transmission gate and the slave latch, no upset occurs at $\phi = 0°$, but an upset occurs at $\phi = 45°$. At (DATA, CLK) = (0, 1), threshold LET is over 200 MeV·cm^2/mg when V_{dd} = 1.2 V, but is decreased to 28 MeV·cm^2/mg when V_{dd} = 0.6 V. We also investigated the minimum distance that does not upset by Kr 45° hits by horizontally shifting critical transistors. No upset occurs by shifting critical transistors over 2μm but the area penalties are 39-46%. We measured radiation tolerance of the DFF and DICEFF in the 65nm bulk process by heavy ions. In the experimental results, the DICEFF has more than 140x better soft error tolerance than the DFF by Ar irradiation. The DICEFF has 300x better soft error tolerance than the DFF by Kr irradiation when V_{dd} = 1.0 V and 1.2 V, but the DICEFF without DICEFF3 has only 7x or 8x better soft error tolerance than the DFF when V_{dd} = 0.6 V. The DICEFF3PG+ has 58x better soft error tolerance than the DFF and 58x better soft error tolerance than the regular DICEFF when V_{dd} = 0.6 V. The DICEFF has errors at V_{dd} = 0.6 V when (DATA, CLK) = (1, 0) and (1, 1). The DICEFF has the lowest soft error tolerance at (DATA, CLK) = (1, 0). This result agrees with the result that the master latch has the critical charge larger than that of the slave latch by curcuit simulations. The distance is not scaled by technology downscaling, which means area overhead becomes larger in more scaled process technologies. There are lots of pairs of transistors in DICEFF that must not upset at the same time. As technology downscaling, it becomes more difficult to keep all the distances between these transistors enough not to upset simultaneously. Therefore, a mitigation technique other than DICEFF is better in advanced scaled bulk processes.

ACKNOWLEDGMENT

The authors would like to thank to QST (National Institutes for Quantum and Radiological Science and Technology). The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC) in collaboration with, Cadence Corporation, Synopsys Corporation and Mentor Graphics Corporation. This work is supported by the Program on Open Innovation Platform with Enterprises, Research Institute and Academia (OPERA) from Japan Science and Technology Agency (JST).

REFERENCES

[1] R. Baumann. The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction. In Digest. International Electron Devices Meeting,, pages 329–332, Dec. 2002.

[2] V. Chandra and R. Aitken. Impact of technology and voltage scaling on the soft error susceptibility in nanoscale cmos. In 2008 IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems, pages 114–122, 2008.

[3] V. Ferlet-Cavrois, L. W. Massengill, and P. Gouker. Single event transients in digital cmos—a review. IEEE Transactions on Nuclear Science, 60(3):1767–1790, 2013.

[4] I. Chatterjee, B. Narasimham, N. N. Mahatme, B. L. Bhuva, R. A. Reed, R. D. Schrimpf, J. K. Wang, N. Vedula, B. Bartz, and C. Monzel. Impact of technology scaling on sram soft error rates. IEEE Transactions on Nuclear Science, 61(6):3512–3518, 2014.

[5] D. Krueger, E. Francom, and J. Langsdorf. Circuit design for voltage scaling and ser immunity on a quad-core itanium processor. In 2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pages 94–95, 2008.

[6] N. Seifert, B. Gill, K. Foley, and P. Relangi. Multi-cell upset probabilities of 45nm high-k + metal gate sram devices in terrestrial and space environments. In 2008 IEEE International Reliability Physics Symposium, pages 181–186, 2008.

[7] D. G. Mavis and P. H. Eaton. Soft error rate mitigation techniques for modern microcircuits. In 2002 IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No.02CH37320), pages 216–225, April 2002.

[16] Y. Tsukita, M. Ebara, J. Furuta, and K. Kobayashi. Soft-error tolerance depending on supply voltage by heavy ions on radiation-hardened flip flops in a 65 nm bulk process. In ASICON, pages A1–4, Oct. 2019.

[8] T. Calin, M. Nicolaidis, and R. Velazco. Upset hardened memory design for submicron cmos technology. IEEE Transactions on Nuclear Science, (6):2874–2878, Dec 1996.

[9] K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera. A low-power and area-efficient radiation-hard redundant flip-flop, DICE ACFF, in a 65 nm Thin-BOX FD-SOI. IEEE Transactions on Nuclear Science, 61(4):1881–1888, Aug 2014.

[10] S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev. A soft error tolerant 10t sram bit-cell with differential read capability. IEEE Transactions on Nuclear Science, 56(6):3768–3773, 2009.

[11] Y. . Li, H. . Wang, R. Liu, L. Chen, I. Nofal, S. . Shi, A. . He, G. Guo, S. H. Baeg, S. . Wen, R. Wong, M. Chen, and Q. Wu. A quatro-based 65-nm flip-flop circuit for soft-error resilience. IEEE Transactions on Nuclear Science, 64(6):1554–1561, 2017.

[12] M. P. Baze, B. Hughlock, J. Wert, J. Tostenrude, L. Massengill, O. Amusan, R. Lacoe, K. Lilja, and M. Johnson. Angular dependence of single event sensitivity in hardened flip/flop designs. IEEE Transactions on Nuclear Science, 55(6):3295–3301, 2008.

[13] O. A. Amusan, L. W. Massengill, M. P. Baze, A. L. Sternberg, A. F. Witulski, B. L. Bhuva, and J. D. Black. Single event upsets in deep-submicrometer technologies due to charge sharing. IEEE Transactions on Device and Materials Reliability, 8(3):582–589, 2008.

[14] L. Hsiao-Heng Kelin, L. Klas, B. Mounaim, R. Prasanthi, I. R. Linscott, U. S. Inan, and M. Subhasish. Leap: Layout design through error-aware transistor positioning for soft-error resilient sequential cell design. In 2010 IEEE International Reliability Physics Symposium, pages 203–212, 2010.

[15] K. Lilja, M. Bounasser, S. . Wen, R. Wong, J. Holst, N. Gaspard, S. Jagannathan, D. Loveless, and B. Bhuva. Single-event performance and layout optimization of flip-flops in a 28-nm bulk technology. IEEE Transactions on Nuclear Science, 60(4):2782–2788, 2013.

[17] Christian Poivey Jenet L. Barth, John C. Isaacs. In The Radiation Environment for the Next Generation Space Telescope, pages A8–A12, Sep. 2000.

[18] J. S. Kauppila, T. D. Loveless, R. C. Quinn, J. A. Maharrey, M. L. Alles, M. W. McCurdy, R. A. Reed, B. L. Bhuva, L. W. Massengill, and K. Lilja. Utilizing device stacking for area efficient hardened SOI flip-flop designs. In IEEE International Reliability Physics Symposium, pages SE.4.1–SE.4.7, June 2014.

[19] K. Warren, L. Massengill, R. Schrimpf, and H. Barnaby. Analysis of the influence of mos device geometry on predicted seu cross sections. IEEE Transactions on Nuclear Science, 46(6):1363–1369, Dec 1999.