Radiation-Hardened Structure to Reduce Sensitive Range of a Stacked Structure for FDSOI

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***Abstract*—Flip-flops (FFs) with stacked transistors have high radiation tolerance in a fully-depleted silicon on insulator (FDSOI) process. However, the flip-flops are weak against a radioactive particle hit with high linear energy transfer (LET) and from high incident angles. In this study we used heavy-ion irradiation tests to evaluate the soft-error tolerance of a stacked structure and a radiation-hardened structure in an attempt to reduce sensitive range (RSR). We propose a novel flip-flop (FF) with the RSR structure. We fabricate a chip in a 65 nm FDSOI process with three latches, each with a different distances between stacked transistors. Experimental results reveal that the stacked structures are weak against a heavy-ion hit that exceeds a LET of 60 MeV-cm^2/mg even though the distance between stacked transistors was increased from 250 nm to 350 nm. We evaluated the RSR structure by TCAD simulations and measured the radiation-hardness of the proposed FF by heavy-ion irradiation on the fabricated chips. Measurement by heavy ions with LET of 67.2 MeV-cm^2/mg at all angles show no detectable errors in the proposed FF.**

***Index Terms*—soft error, heavy ion, FDSOI, flip-flop, low delay overhead, stacked transistor.**

I. Introduction

The emphasis on technology downscaling has led to the demand for semiconductor chips that are more reliable against soft errors. Soft error is a phenomenon where radiation upsets the stored values in flip-flops (FFs) or SRAMs and causes malfunction in digital circuits. Most soft errors are instigated by heavy ions in outer space and in terrestrial regions by neutrons or alpha particles.

Devices with advanced technologies for outer space require highly reliable radiation-hard designs. The triple modular redundancy (TMR) [1] and the dual interlocked storage cell (DICE) [2][3] are widely used to increase reliability in these devices. However, TMR and DICE have larger delay, area and power overheads than conventional FFs. Thus, radiation-hardened FFs with smaller overheads are indispensable. A stacked structure on fully-depleted silicon on insulator (FD-SOI) has been found to mitigate soft errors with small area and power penalty [4][5][6].

Prior reports have shown that neutron-induced soft error rates (SERs) on 90 nm DICE latches are more than 10x higher than that on a non-redundant latch [7]. In contrast, the neutron-induced SER of a DICE FF is almost half of that of a DFF (Delayed FF) in a 40 nm technology [8]. The weak mitigation effect in the 40 nm technology, is because the narrow spacing between transistors that promotes charge collection on multiple nodes when they are hit by an ion. Similarly, stacked structures on FDSOI are influenced by charge sharing when a heavy ion has high linear energy transfer (LET) [9]. The cross section (CS) of the stacked structure in a 65 nm FDSOI process is shown in Fig. 1. CS of the stacked latch is 1/11 the value of a conventional unstacked latch even when the latches are hit by heavy ions with LET of 40.9 MeV-cm^2/mg. But CS of the stacked latch gradually approaches to the value of an unstacked latch as LET increases.

Similar to the stacked inverter, the reduce sensitive range (RSR) inverter has also been proposed to mitigate soft errors [4]. The metal wire connects the two nodes between the stacked PMOS and NMOS transistors in the RSR inverter. Reference [4] states that the soft-error tolerance against heavy ions in latches using stacked inverters and the RSR inverters are almost equal in a 0.15 μm FDSOI. The stacked latch in a 65 nm FDSOI is susceptible to high-energy heavy ions due to the narrow distance between the stacked transistors. However, in a 0.15 μm FDSOI, CSs of the stacked and RSR latches when the latches were hit by heavy ion with 15 MeV-cm^2/mg were not dramatically different with the CSs when heavy ion has 64 MeV-cm^2/mg. Even when a heavy ion generates carriers between the stacked transistors in the off-state in a 65 nm FDSOI, carriers can go to a power or ground node through the stacked transistor in an on-state in the RSR inverter. In a stacked inverter, carries generated between the pair of stacked PMOS or NMOS transistors in an off-state, cannot easily go to power or ground node. The metal wire makes a difference in the soft-error tolerance of the RSR and stacked inverters in the 65 nm FDSOI.

In this paper, we propose a radiation-hardened FF named reduction sensitive range with low delay (RSRLD) that reduce soft errors for FDSOI even against heavy ions exceeding 40.9 MeV-cm^2/mg. We evaluated the radiation-hardness of the FFs by TCAD simulations and heavy-ion irradiation on a test chip fabricated in a 65 nm FDSOI process. Section II explains the radiation-hardened structures and TCAD simulations results. Section III explains the proposed FFs using the RSR structures. Section IV shows the test chip structure and experimental heavy-ion irradiation results. Section V concludes this paper.

II. Radiation-Hardened Structure

FDSOI processes suppress radiation effects by preventing charge collection under the buried oxide (BOX) layer. The parasitic bipolar effect (PBE) however, is the dominant cause

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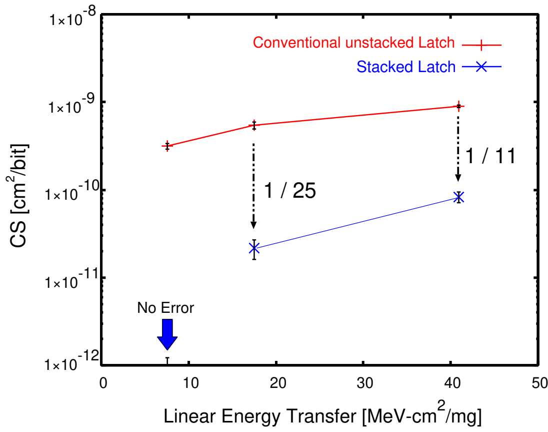


Fig. 1. Measurement results of heavy-ions-induced CS on latches in a 65 nm FDSOI process [9].

soft errors in FDSOI devices [10]. The holes generated in a channel increases the body potential of the layer. Then, a parasitic bipolar transistor composed of drain, body and source terminals is turned on. The stacked structure has been shown to suppress PBE in FDSOI [4]. Figure 2 shows a stacked inverter composed of two series-connected NMOS and PMOS transistors. Each diffusion between the two series-connected transistors is shared to minimize area overhead. When a radioactive particle hits close to NMOS transistors in the stacked inverter, its output node is not disturbed unless both of stacked NMOS transistors are turned on by PBE simultaneously. However, the radiation-hardness of the stacked structure decreases as the LET of heavy ions increases. Heavy ions with high LET may influence both of stacked transistors when they pass close by.

Figure 3 shows a stacked inverter [4] that we have named it the reduction sensitive range (RSR) inverter. The diffusion layers between two series-connected NMOS and PMOS transistors in the RSR inverter are shorted by a metal wire to eliminate holes generated by a particle hit.

We evaluate radiation-hardness of the RSR inverter and compare the results with that of the stacked inverter.

A. TCAD Simulation Analyses

Radiation-hardness of the RSR inverter is evaluated by three-dimensional TCAD simulations using Synopsys Sentaurus at supply voltage (V_{DD}) = 0.8 V in the 65 nm FDSOI. Figure 4 depicts the schematic and the cross-section of the RSR latch composed of the RSR inverter and a conventional inverter. We use the 3D transistor with a raised diffusion layer. The raised diffusion layer constructed on source and drain terminals consists of 20 nm silicon without nickel silicide. The drain, gate and source terminals of the 3D transistor are fully covered by contancts. Distance between the stacked transistors in the RSR inverter is 260 nm. The spatial distribution of charge cloud is defined as a Gaussian function with the standard deviation of 30 nm [11]. A particle hit on an NMOS transistor was used in this study because NMOS transistors are more vulnerable to particle hits than PMOS transistors [9].

1) Radiation-hardness of RSR Inverter: We evaluated soft-error tolerance of the RSR inverter when a heavy ion injects at T1, T2 or the midpoint between T1 and T2. Heavy ions up to 60 MeV-cm^2/mg LET are injected in the RSR inverter to simulate conditions in outer space [12].

a) Particle hits at T1: The stored value of the RSR latch is not upset even when a particle has a LET of 60 MeV-cm^2/mg. Voltage waveforms of N2 and N3 are shown in Fig. 5 (a). The SET pulse is attenuated by 44% after passing through the PMOS transistor (T3). The SET pulse is suppressed because signals below the threshold voltage cannot pass through the PMOS transistor. The SET pulse attenuation depends on threshold voltage of a PMOS transistor. In prior study, we reported that SET pulse by a particle with LET of 60 MeV-cm^2/mg can attenuate after passing through the PMOS transistor and soft errors are suppressed in the low-threshold transistors in Ref. [6]. In this paper, simulations were conducted using high-threshold low-power transistors because our test chips were fabricated by low-power transistors.

b) Particle hits at T2: The stored value of the RSR latch is not upset even when a particle has LET of 60 MeV-cm^2/mg as shown in Fig. 5 (b). A parasitic bipolar transistor in T2 is activated. Although PBE induces current flow, soft error rates do not increase because the voltage of the drain and source terminals on T2 must be equal due to the short-circuited wire.

c) Particle hits at the midpoint between T1 and T2: The stored value of the RSR latch is not upset for a particle with LET of 60 MeV-cm^2/mg as shown in Fig. 5 (c). It is 7x larger than the threshold LET (the minimum LET value at which the latch upsets: LET_{th}) of the latch composed of the stacked inverter instead of the RSR inverter.

We found that the stacked inverters were more sensitive to soft errors at higher tilt angles than the conventional inverter in Ref. [5] because it is more possible for heavy ions to pass through the sensitive volume. The tilt angle (θ) of the stacked transistors is defined as shown in Fig. 6 (a). Radiation-hardness of the stacked structure depending on tilt angles are evaluated using the LET_{th} when a heavy ion injects at the midpoint between T1 and T2. Figure 6 (b) shows that the LET_{th} strongly correlates with the tilt angles. The LET_{th} of the RSR latch at the tilt angles of 30° and 60° are more than 3.5x bigger than that of the stacked latch. However, the LET_{th} of the RSR latch gradually approaches to that of the stacked latch as the tilt angle increases. These results show that the RSR inverter is more sensitive to soft errors at higher tilt angles than the stacked latch. Furthermore, the RSR inverter is more resistant to soft error than the stacked inverter up to a tilt angle of 60°.

2) Comparison of Stacked and RSR inverters: In order to explain the difference of the radiation-hardness between the stacked and the RSR inverters, hole density induced by a heavy-ion strike is calculated using TCAD simulations. Holes forcibly activate the parasitic bipolar transistor. Figure 7 shows transient hole densities in the body layer of the stacked transistors after a heavy-ion strike. In the stacked inverter in Fig. 7 (a), generated holes remain in both channel regions even after 100 ps at a density of 2×10^{19} cm^{-3}. As a result, a stored value flips when a heavy-ion hits the stacked inverter. However, in the RSR inverter in Fig. 7 (b), generated holes decrease below 0.8×10^{19} cm^{-3} after 20 ps. The sharp decline

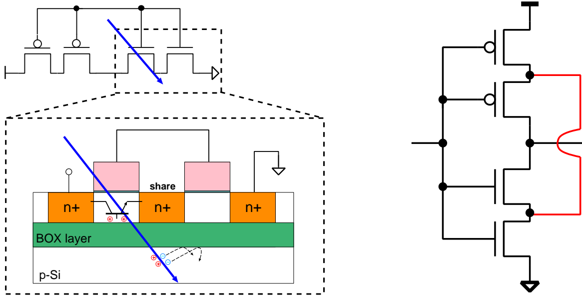


Fig. 2. Stacked inverter in FD-SOI [4].

Fig. 3. Reduction sensitive range inverter [4].

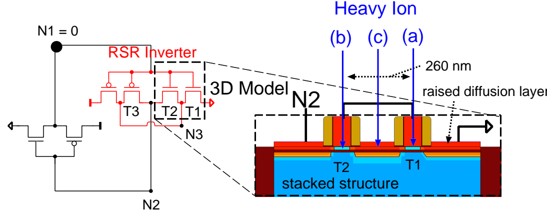


Fig. 4. Schematic diagram and cross-section of 3D models of RSR latch used for TCAD simulations. By setting the initial value of N0 to 0 V, a heavy-ion hits on NMOS transistors at V_{DD} = 0.8 V.

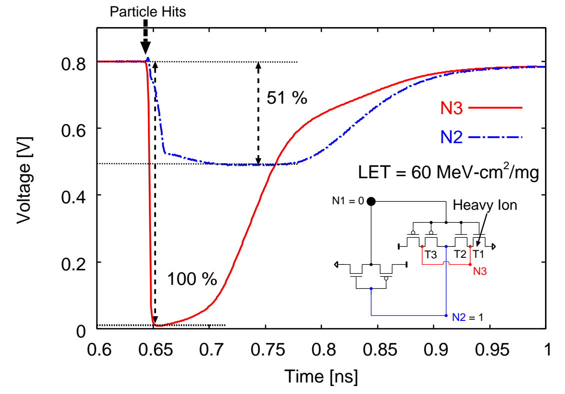
in generated holes is because generated holes are recombined with electrons flowing through the short-circuited wire in the RSR inverter. Thus, it is stronger against a heavy-ion strike than the stacked inverter in the 65 nm FDSOI.

III. Radiation-Hardened Structure in Flip-Flop

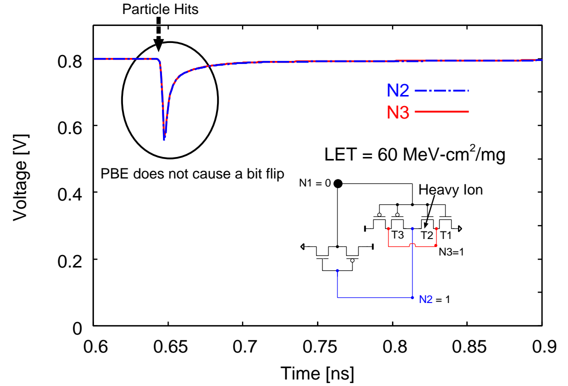
Figure 8 shows a conventional DFF called Transmission Gate FF (TGFF). It has the master and slave latches composed of a tristate inverter and an inverter. It is not tolerant to soft errors. The stacked FF has a master and slave latch composed of a stacked tristate inverter and a stacked inverter (Fig. 9). Although the overheads of delay time and area of the stacked FF are bigger than TGFF, the stacked FF is resistant to soft errors as already shown in Fig. 1.

The reduction sensitive range FF (RSRFF) has a master and slave latch composed of the RSR tristate inverter and the RSR inverter (Fig. 10). RSRFF has long delay similar to the stacked FF due to the stacked structure. We propose a radiation-hardened FF using the RSR structure with shorten delay time (Fig. 11) named the RSR with low delay overhead FF (RSRLDFF). The transmission gate in RSRFF was replaced by the tristate inverter (TI), which is directly connected to the output inverter. Thus, the RSR structure in the slave latch has a small impact on delay time. In addition, the RSR inverter in the master latch and TI is connected to N3 instead of N2 as shown in Fig. 11. Through this connection, the tristate inverter between the master and slave latches is driven by T1 and T4 transistors directly connected to power or ground rails while maintaining the RSR structure. Therefore, RSRLDFF achieves a shorter D-Q delay time than the stacked FF.

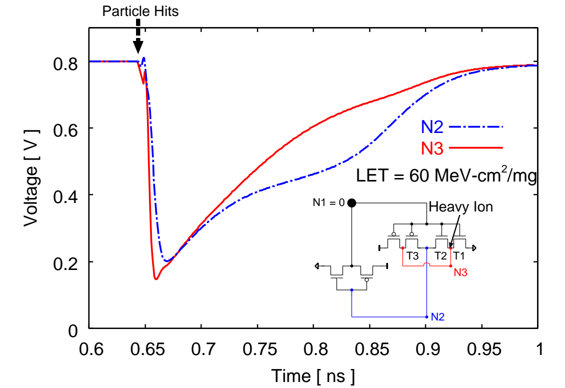
We measure D-Q delay, setup time and power consumption in FFs using SPICE simulation in a 65 nm FDSOI process. Table I indicates the simulation results of D-Q delay, setup



(a) The particle hits at T1 transistor. N2 and N3 are perturbed.



(b) The particle hits at T2 transistor. PBE is not significant.



(c) The particle hits at the midpoint between T1 and T2.

Fig. 5. Simulation results of voltage waveforms caused by a heavy-ion strike. Latch in Fig. 4 does not upset up to LET = 60 MeV-cm^2/mg.

time, power at 10% data activity and V_{DD} = 0.8 V and area normalized to those of TGFF. The values in parentheses are normalized to those of the stacked FF. The delay time of the stacked FF is 1.8x longer than that of TGFF because the stacked inverters increases delay time. The delay time of RSRFF is 2.2x longer than that of TGFF. However, the proposed RSRLDFF is 30% faster than the stacked FF because the stacked structure with the short-circuited wire in RSRLDFF has little influence on its delay time. The setup time of the stacked FF, RSRFF and RSRLDFF are more than 2x longer than that of TGFF. Thus, they are some penalties for the increase in operating speed. The longer setup time is because

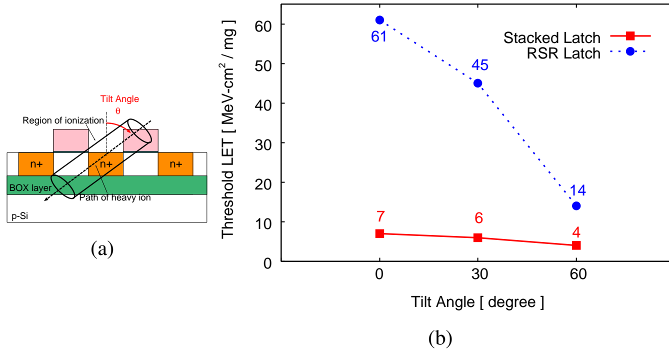


Fig. 6. (a) shows tilt angles of stacked transistors for TCAD simulations [5]. Cylinder shows the region of ionization. (b) shows simulation results depending on tilt angles.

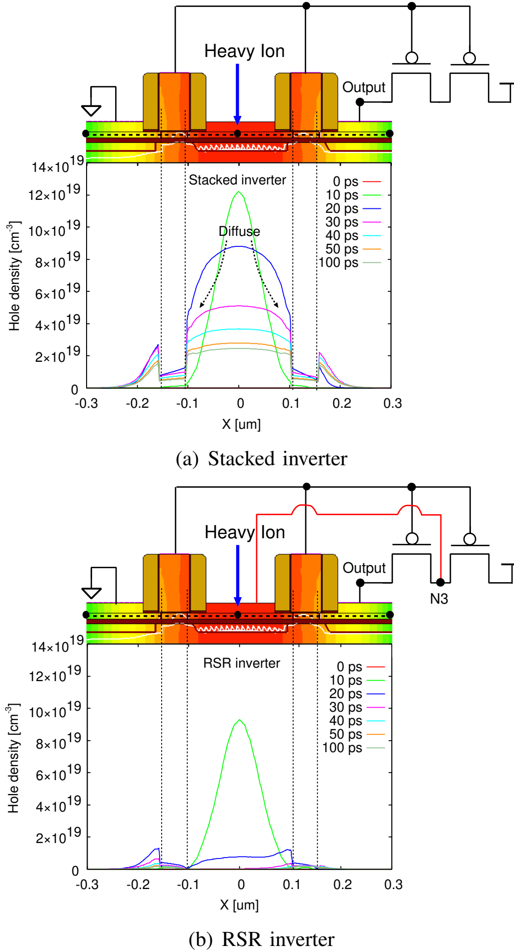


Fig. 7. Simulated transition of hole density in body layer when a heavy ion with LET of 60 MeV-cm^2/mg passes through midpoint between two series-connected NMOS transistors at 0 ps.

the stacked inverter and the RSR inverter are slower than the conventional inverter. The power consumption is almost the same as that of the stacked FF and TGFF. The RSR structure needs additional 20 nm of space between the stacked transistors because the diffusion layer has a contact for the short-circuited wire as shown in Fig. 12. However, the areas of the stacked FF and RSRFF are equivalent. This is because the contact can be put without increasing the area of a standard

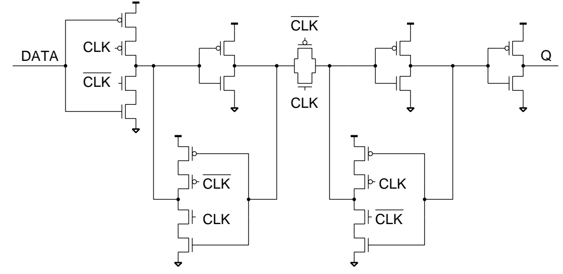


Fig. 8. Transmission-gate FF (TGFF).

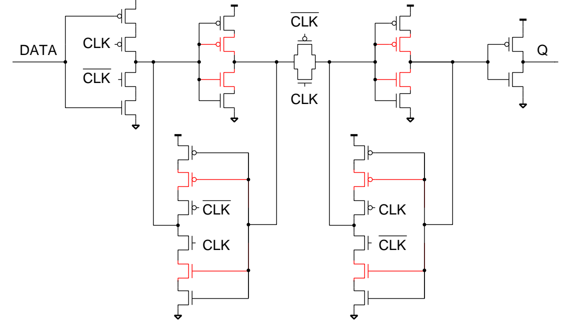


Fig. 9. Stacked FF.

TABLE I
SIMULATION RESULTS OF D-Q DELAY, SETUP TIME, POWER, AREA OF EACH FF WHEN V_{DD} = 0.8 V. ALL VALUES ARE NORMALIZED TO THOSE OF TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF STACKED FF USING SPICE SIMULATION.

FF	D-Q delay	Setup time	Power	Area
TGFF	1	1	1	1
Stacked FF	1.76 (1)	2.69 (1)	1.05 (1)	1.24 (1)
RSRFF	2.16 (1.23)	4.27 (1.58)	1.07 (1.04)	1.24 (1.00)
RSRLDFF	1.25 (0.71)	3.07 (1.14)	1.08 (1.05)	1.35 (1.08)

cell of RSRFF. The area of RSRLDFF is bigger than that of the stacked FF because of the two additional transistors.

IV. Experimental Results of Heavy-Ion Irradiation

Heavy-ion irradiation test was carried out at the Takasaki ion accelerators for advanced radiation application (TIARA), Japan. We fabricated two test chips in a 65 nm FDSOI process with a thin BOX layer [13]. Note that their manufacturing processes are different from that in Fig. 1. We measured the number of upsets caused by heavy ions at V_{DD} = 0.8 V. Test chip were exposed to heavy ions at static conditions for 30 s.

CS was used to evaluate soft-error tolerances using Eq. 1 [14]. The error bars are within 95.4% (2σ) confidence.

$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{ion}} \cos\,\theta\ N_{\mathrm{FF}}} \qquad (1)$$

CS is calculated from the number of errors (N_{error}), the effective heavy ion fluence at θ ($N_{\mathrm{ion}} \cos\,\theta$), and the number of FFs (N_{FF}). The tilt angle (θ) of the chip is defined as shown in Fig. 13 (a).

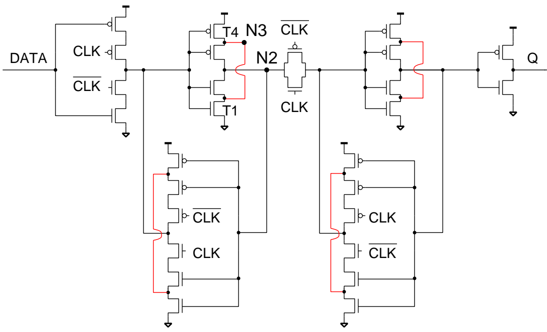


Fig. 10. Reduction Sensitive Range FF (RSRFF).

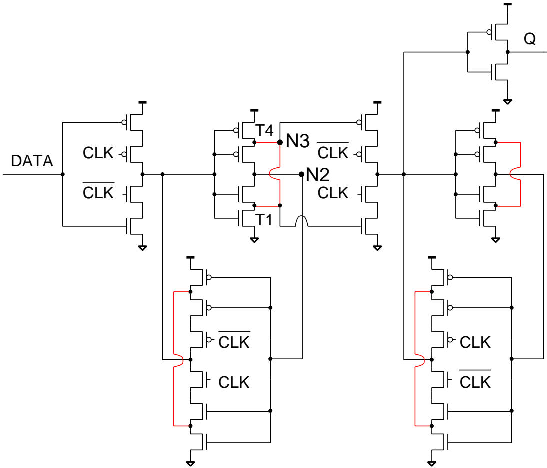


Fig. 11. RSR with low delay overhead FF (RSRLDFF).

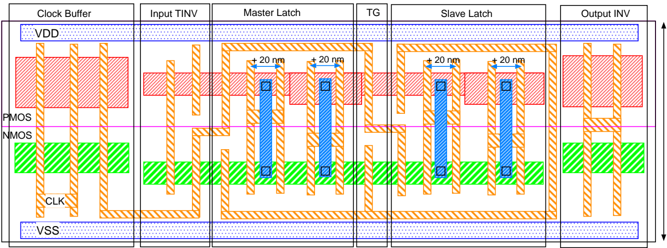


Fig. 12. Simplified layout of RSRFF.

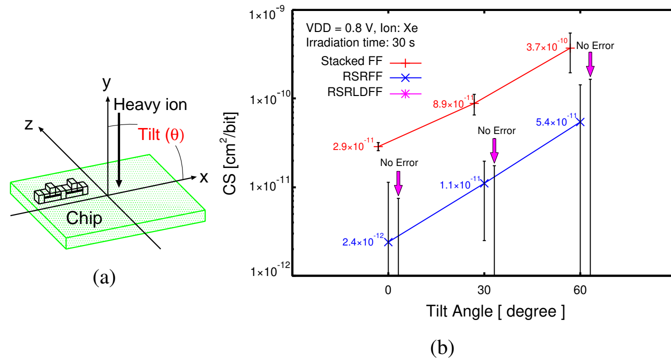


Fig. 13. (a) shows tilt angles of chip. (b) shows experimental results in relation to tilt angles when (DATA, CLK) = (0, 1). Error bars are within 95.4 % confidence intervals.

A. Vulnerability of Stacked Structure

The effect that the distance between stacked transistors has on radiation resilience was investigated. We assumed that

TABLE II
ENERGY AND LET OF HEAVY IONS.

Heavy-ion	LET [MeV-cm^2/mg]	Energy [MeV]
Ar	17.5	107
Kr	40.9	230
Xe	67.2	350

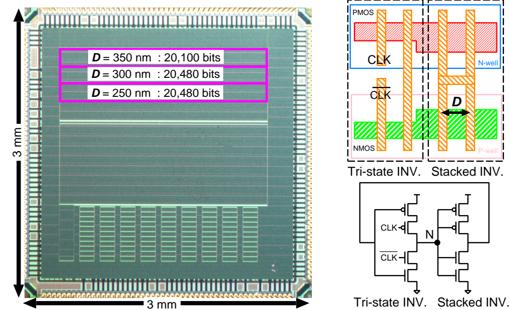


Fig. 14. Chip micrograph fabricated including stacked structures with three different distances between stacked transistors in a 65 nm FDSOI process. Distance between stacked transistors is defined as D.

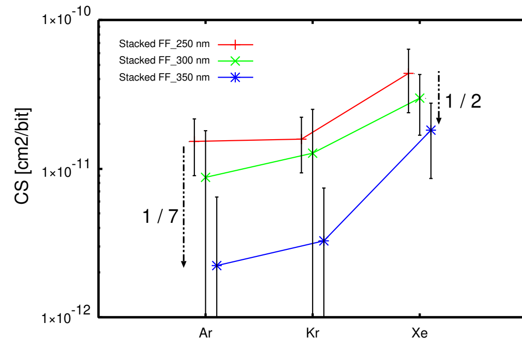


Fig. 15. Heavy-ion-induced cross sections at N = 0 in Fig. 14. Error bars are within 95.4% confidence. Down arrows mean no error.

stacked structures have high soft error tolerance when there is enough distance between stacked transistors (D). This is because two stacked transistors are not influenced by a heavy ion at the same time when D is longer enough than the spatial distribution of a charge cloud generated by a particle strike.

Three latches composing of a tristate inverter and a stacked inverter with different distances between stacked transistors were fabricated as shown in Fig. 14. Measurements were repeated five times under each condition from the normal angle when the node N = 0 in Fig. 14. The radiation hardness was investigated by three ion species as described in Table II.

Figure 15 shows the heavy-ion-induced CSs in relation to the distance between stacked transistors. The Ar-induced CS of the latch with D = 350 nm is 1/7 smaller than that of the latch with D = 250 nm. However, the Xe-induced CS of the latch with D = 350 nm is only 1/2 smaller than that of the latch with D = 250 nm. The experimental results revealed that widening D from 250 nm to 350 nm decreases CS of the stacked structure after a radioactive particle hit with less than LET of 41 MeV-cm^2/mg. The stacked structures are not effective against a radioactive particle hit with more than LET of 60 MeV-cm^2/mg even though D = 350 nm.

TABLE III
NUMBER OF EMBEDDED FFS IN THE CHIP.

FF	# of FF
TGFF	22,680
Stacked FF	22,950
RSRFF	22,950
RSRLDFF	22,680

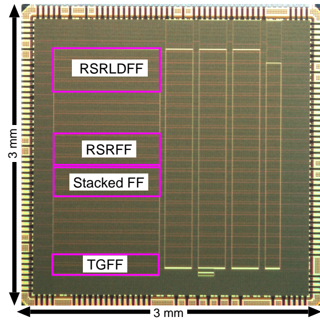


Fig. 16. Chip micrograph fabricated including proposed FFs in a 65 nm FDSOI process.

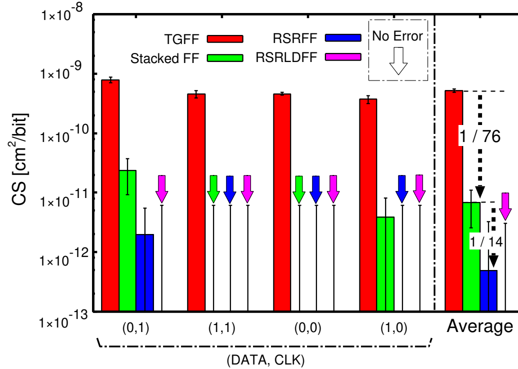


Fig. 17. Experimental results of heavy-ion-induced cross sections from the normal angle under four DATA and CLK states and averaged CSs. Error bars are within 95.4% confidence. Down arrows mean no error.

B. Radiation Hardness of Proposed Flip Flop

1) Experimental Results: We evaluate the radiation hardness of the proposed RSRLDFF. TGFF, the stacked FF, RSRFF and RSRLDFF were fabricated as shown in Fig. 16. Table III indicates the number of embedded FFs in the chip. The distance between stacked transistors in the stacked FF and RSRFF were equivalent.

Measurements were repeated five times per condition with Xe ions (LET of 67.2 MeV-cm^2/mg) from a normal angle under four DATA and CLK states for two chips. In addition, we examined Xe-induced CSs at incident angles at $V_{\rm DD}$ = 0.8 V when (DATA, CLK) = (0, 1). Experiments were carried out at 30° and 60° tilt angles. Note that measurements were repeated five times at 60° tilt angle and three times at 30° tilt angle.

Figure 17 shows heavy-ion-induced CSs under four static conditions and the averaged CSs when $V_{\rm DD}$ = 0.8 V. CS of the stacked FF in Fig. 17 was smaller than that in Fig. 1 mainly due to differences of the manufacturing process. The averaged CS of the stacked FF is 1/76 smaller than that of TGFF. The stacked structure suppressed soft error but 14 errors occurred in the stacked FF, while there was only total 1 error in RSRFF. The RSR structure reduced soft errors in the stacked structure via the short-circuited wire. RSRLDFF was the most resistant and had no soft errors.

Figure 13 (b) shows the heavy-ion-induced CSs in relation to tilt angles. CSs of RSRFF at an angle of 30° and 60° were 1/7 smaller than that of the stacked FF. There were 16 errors in the stacked FF tilted at a 60° angle, while there were two errors in RSRFF at an angle of 60°. There were no errors in RSRLDFF at all angles. The proposed RSRLDFF was the most resilient to soft errors even when tilted at higher angles than the stacked FF.

2) Comparison between Simulation and Experimental Results: Experimental results showed RSRFF is 7x stronger against soft errors than the stacked FF at angles of 0°, 30° and 60°. Simulation results also showed that the RSR inverter had higher soft-error tolerance than the stacked inverter when tilted at angles up to 60°. The CS of RSRFF at an angle of 60° is close to the CS of the stacked FF at an angle of 0° in the experimental results in Fig. 13 (b). The $LET_{\rm th}$ at an angle of 60° is also close to the $LET_{\rm th}$ of the stacked FF at an angle of 0° in the simulation results in Fig. 13 (b). We concluded the RSR inverter is more resilient against soft error than the stacked inverter in the 65 nm FDSOI process even at higher incident angles and particle energy.

3) Proposed Flip Flop for higher data activity: If an input data is different from a stored data, the input tristate inverters, the tristate inverter or the transmission gates in between master and slave latches in Fig. 9, 10, and 11 are all sensitive to soft errors. Figure 18 shows the soft error sensitive parts in RSRLDFF when an input data is different from a stored data. These states do not become dominant at low data activity in flip-flops. But it is mandatory to replace the tristate inverters and the transmission gates with radiation-hard ones for higher data activity (HDA) such as an asynchronous counter.

All measurements were done to initialize all flip flops to 0 or 1. The soft error tolerance of the radiation-hardened FFs was not measured when input data is different from storage data. Further measurements using the CHB (checkerboard) allows us to evaluate the sensitivity in Fig. 18. However, it takes long to initialize all FFs in the implemented shift registers since the clock signal is given from the last FF, while input data is given from the first FF to prevent timing violation [15].

Figure 19 depicts radiation-hardened FFs for HDA to mitigate soft errors when input data is different from stored data. The stacked FF, RSRFF and RSRLDFF have the input tristate inverters composed of series-connected three NMOS and PMOS transistors. Two transistors of them are controlled by the CLK signal. In RSRFF and RSRLDFF, the input tristate inverters take the RSR structure. The transmission gate in between master and slave latches in the stacked FF and RSRFF are duplicated as shown in Figs. 19 (a), (b). While, RSRLDFF has the tristate inverter with the RSR structure in between master and slave latches composed of series-connected three NMOS and PMOS transistors in Fig. 19 (c).

Table IV indicates the simulation results of D-Q delay, setup time, power dissipation at 10% data activity at $V_{\rm DD}$ = 0.8 V and area of FFs in Fig. 19. All values are normalized to those of TGFF. The values in parentheses are normalized to those of the stacked FF for HDA. All radiation-hardened FFs for HDA have bigger overheads than the FFs not for HDA in Figs. 9 - 11. The circuit performance and area ratios of the proposed RSRLDFF for HDA to the stacked FF for HDA are almost same as the ratios of the standard RSRLDFF to the standard

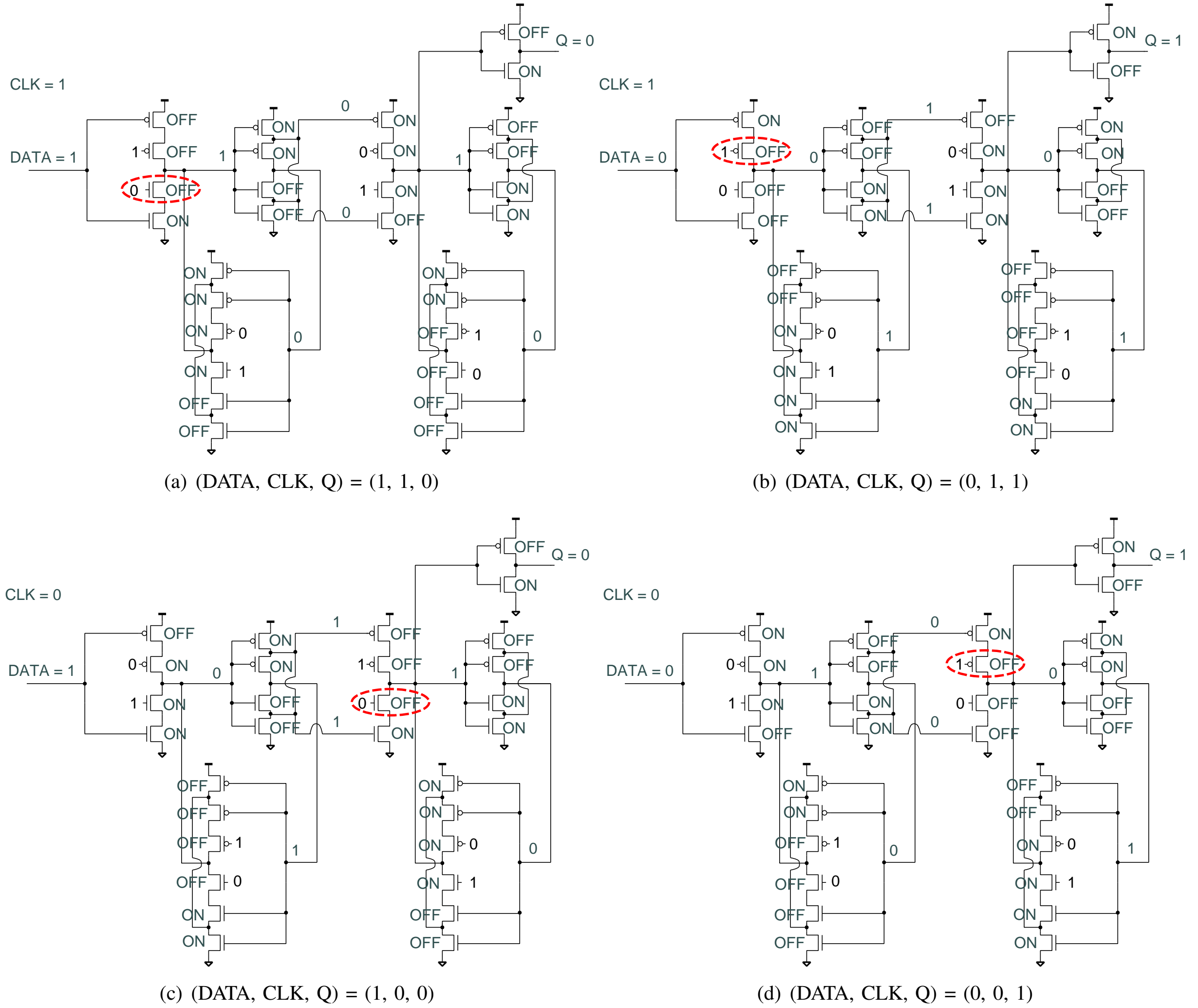


Fig. 18. Soft error sensitive part in RSRLDFF when input data is different from storage data. Transistor enclosed in red dotted circle is sensitive part.

TABLE IV
SIMULATION RESULTS OF D-Q DELAY, SETUP TIME, POWER, AREA OF EACH FF FOR HIGHER DATA ACTIVITY WHEN V_{DD} = 0.8 V. ALL VALUES ARE NORMALIZED TO THOSE OF TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF STACKED FF FOR HDA USING SPICE SIMULATION.

FF	D-Q delay	Setup time	Power	Area
TGFF	1	1	1	1
Stacked FF for HDA	2.24 (1)	4.72 (1)	1.14 (1)	1.35 (1)
RSRFF for HDA	2.78 (1.24)	6.94 (1.47)	1.16 (1.02)	1.35 (1.00)
RSRLDFF for HDA	1.75 (0.78)	5.11 (1.08)	1.19 (1.04)	1.47 (1.09)

stacked FF.

V. Conclusion

We evaluated radiation resilience in relation to the distance between stacked structures in a 65 nm FDSOI. Increasing the distance from 250 nm to 350 nm decreases CSs of the stacked structures when hit by a radioactive particle with less than LET of 41 MeV-cm^2/mg. The stacked structures were vulnerable against a radioactive particle hit with LET exceeding 60 MeV-cm^2/mg even at a distance of 350 nm.

We measured the soft-error tolerance of the radiation-hardened structure for FDSOI that has a short-circuited wire between series-connected PMOS and NMOS transistors to reduce sensitive range of the stacked structure. In addition, we propose a radiation-hardened FF with a RSR structure that has small delay overhead. The proposed RSRLDFF has 30% shorter delay and only 10% additional area overheads than the stacked FF. We investigated their radiation-hardness by TCAD simulations and heavy-ion irradiation. We observed no errors in the proposed RSRLDFF at incident angles of 0°, 30° and 60° even at LET of 67.2 MeV-cm^2/mg. We there fore conclude that RSRLDFF is more resilient against soft errors than the stacked FF even at higher incident angles and particle energy.

Further studies are needed in order to measure SERs in the CHB pattern.

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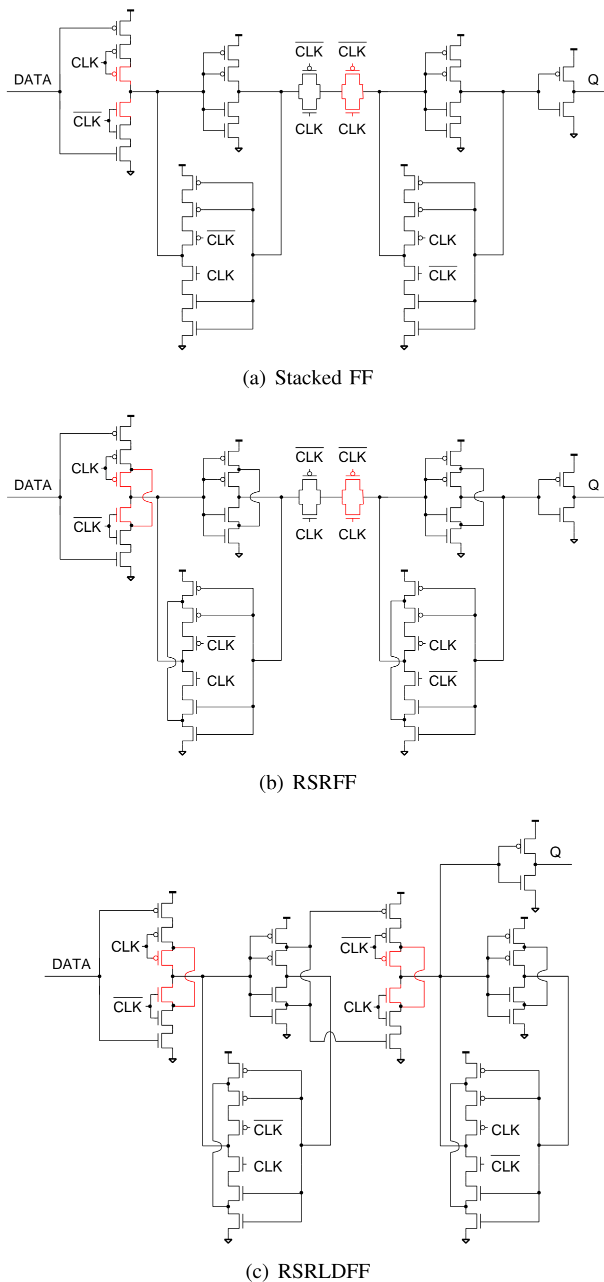

(a) Stacked FF

(b) RSRFF

(c) RSRLDFF

Fig. 19. Radiation-hardened FFs for higher data activity (HDA).

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