Total Ionizing Dose Effect by Gamma-ray Irradiation and Recovery Phenomenon by Applying High Gate Bias to Commercial SiC Power MOSFETs

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***Abstract*—This paper reports the recovery effect of V_{GS} application on *I-V* characteristics of Si and SiC power MOSFETs degraded by the Total Ionizing Dose (TID) Effect using Co-60 γ-ray source. An SiC planar MOSFET showed the lowest degradation by γ-ray irradiation of 118 krad, with a decrease in V_{th} of about 0.4 V. The two types of SiC trench MOSFETs showed different TID responses and recoveries by V_{GS} application, which is assumed to be by the difference in oxide thickness.**

I. Introduction

SiC MOSFETs are next-generation power semiconductors that enable compact, high-performance power systems. They are expected to the miniaturize and enhance power systems for spacecraft. For outer space use, it is essential to evaluate the total ionizing dose (TID) effect as a degradation phenomenon of semiconductors because of large amounts of radiation. Fig. 1 shows the principle of TID [1]. When semiconductors are irradiated, electron-hole pairs are generated by the ionizing action of radiation. Some of the holes of the generated electron-hole pairs are trapped in the oxide layer and accumulate, resulting in the degradation of device characteristics. It is necessary to measure the effect of low quality oxide layers and structural differences on TID in SiC MOSFETs, and TID effects on commercial SiC MOSFETs are also being investigated [2], [3]. Recovery phenomenon exists in TID. It was reported that TID is recoverd by thermal annealing and applying a high gate electric field [3]-[7]. Applying a high gate electric field is more effective than thermal annealing [3]. In this paper, we measured the degradation of commercial Si and SiC planar and SiC trench MOSFETs by γ-ray irradiation and their recovery phenomena.

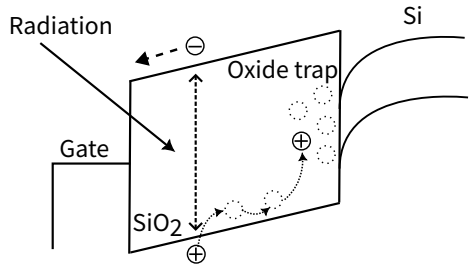

Fig. 1. Schematic diagram of TID degradation of MOS devices by radiation [1].

TABLE I
Electrical characteristics of target MOSFETs.

MOSFET	Si planar	SiC planar	SiC trench vendor A	SiC trench vendor B
Maximum V_{DS} [V]	600	650	650	650
Maximum I_D [A]	21	22	20	21
Maximum V_{GS} [V]	25	19	23	22
Recommended driving V_{GS} [V]	10	15	18	18
R_{on} [mΩ]	130	120	107	120

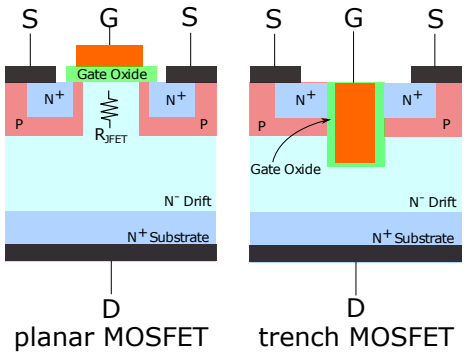

Fig. 2. Cross-sectional views of planar MOSFET and trench MOSFET.

II. Experimental methods

Irradiation tests are performed by using a Co-60 source. We used an Agilent N6700C power supply to measure the *I-V* characteristic and V_{DS} = 0.1 V for the I_{DS} - V_{GS} characteristic.

A. γ-ray irradiation

To compare the TID effect of power MOSFETs, commercial power MOSFETs shown in Table I were γ-ray irradiated. All of these MOSFETs were manufactured by different companies. In this paper, we define the SiC trench MOSFET of the vendor A and the vendor B as the SiC_A and the SiC_B, respectively. Fig. 2 shows the cross sections of the planar and trench structures, and the SiC trench MOSFETs have embedded gate oxide layers. The Co-60 source were irradiated up to 118 krad. Recommended driving voltages of V_{GS} = 10 V and 18 V were applied to the Si and SiC MOSFETs, respectively, during irradiation.

B. Applying High Gate Bias

After γ-ray irradiation, high V_{GS} was applied to two types of SiC trench MOSFETs from V_{GS} = 18 V to 38 V. The SiC planar MOSFET was not measured because it showed much smaller degradation by TID. V_{GS} was applied from V_{GS} = 18 V to 50 V on the Si MOSFET, because it was not recovered at V_{GS} = 38 V. V_{GS} was applied in steps of 2 V every 5 min. And then V_{GS} was set to 0 V for 10 min.

C. Additional High Gate Bias Application

The second high V_{GS} application was measured to the SiC_A, which had a smaller recovery than the SiC_B. Two months was passed at the second V_{GS} application after the first one. The V_{GS} was applied from V_{GS} = 40 V to 50 V, and then V_{GS} = 0 V for 10 minutes.

III. Results and Discussion

Figs. 3 and 4 show the results of I-V characteristics before and after γ-ray irradiation and before and after the first gate bias application, respectively. The SiC planar MOSFET showed the lowest degradation, with the threshold voltage decrease by about 18%. The SiC_B after irradiation suffered from I_{DS} increase of 1 mA at V_{GS} = 0 V. The Si MOSFET was irrecoverably damaged by TID, with I_{DS} of 40 mA at V_{GS} = 0 V after V_{GS} = 50 V was applied. In Fig. 5 and Table II, the SiC_B recovered to 98% of the pre-irradiation V_{th} after the first application of gate bias. V_{th} was restored by neutralization of oxide trap charge by FN tunnel electrons from the application of high gate bias [3]. After the application of V_{GS}, the SiC_B rapidly recovered to the initial V_{th} level, while the SiC_A monotonically recovered. This is presumably due to the difference in the actual gate electric field by the difference in oxide layer thicknesses. The SiC_A have a lower electric field than the SiC_B. When additional V_{GS} was applied to the SiC_A, V_{th} recovered significantly, similar to the SiC_B, and recovered to the initial V_{th}. In the 2 months between the first application of V_{GS} and the additional application of V_{GS}, there was only a decrease in V_{th} of about 0.2 V, and there is be no damage caused by the high gate bias. However, gate reliability must be evaluated because a much higher voltage was applied to V_{GS} than the recommended drive voltage. The decrease in V_{th} after 2 months at room temperature is presumably due to the recovery from the bias temperature instability (BTI) effect and the FN tunneling electrons.

TABLE II
V_{th} change in SiC trench MOSFETs.

SiC trench MOSFET	V_{th} [V]	
	SiC_A	SiC_B
fresh device	4.22	3.64
before gate bias	2.65	0.13
after gate bias (V_{GS} = 38V)	3.06	3.58
after gate bias (V_{GS} = 50V)	4.22	N/A

IV. Conclusion

The recovery characteristics of commercial Si and SiC power MOSFETs were measured by γ-ray irradiation and high gate bias application. The SiC planar MOSFET had the highest TID resistance by γ-ray irradiation. The Si planar MOSFET was damaged permanently. The SiC_B was more heavily degraded by γ-ray irradiation than the SiC_A. It recovered to the original V_{th} level by applying V_{GS} = 38 V. Contrary to the small degradation caused by TID, the SiC_A showed less recovery by application of V_{GS} = 38V than the SiC_B, but recovered to the original V_{th} by applying additional high gate bias. This suggests that the oxide layer of the SiC_A was thicker than that of the SiC_B. The possibility of reusing MOSFETs by recovering device degradation due to TID was indicated, but how to apply such a high V_{GS} in outer space and gate oxide layer reliability must be considered. To improve the lifetime of satellites, it is necessary to select MOSFETs with high tolerance to TID, such as the SiC planar MOSFET used in this study.

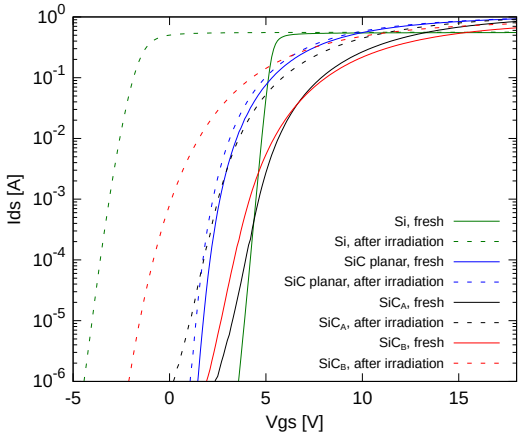

Fig. 3. I-V characteristics by γ-ray irradiation.

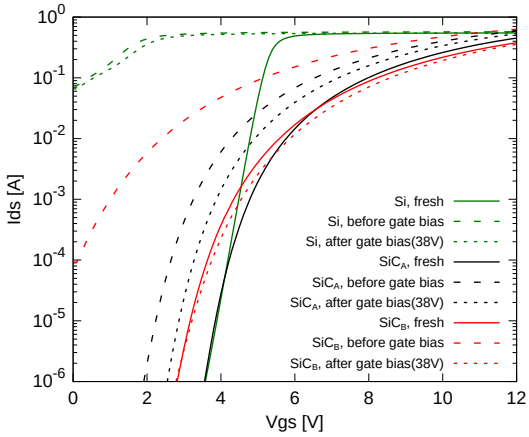

Fig. 4. I-V characteristics by high gate bias.

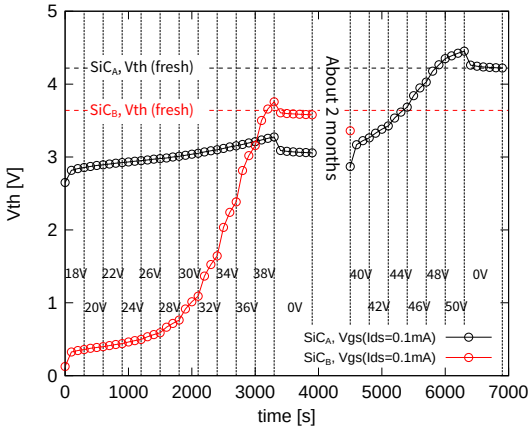

Fig. 5. Recovery of V_{th} of SiC trench MOSFETs by Applying high V_{GS}.

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