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Plasma Induced Damage Depending on Antenna Layers in Ring Oscillators

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Abstract

Plasma Induced Damage (PID) is an inevitable reliability issue in VLSI. In this paper, PID depending on different antenna layers is evaluated. Ring Oscillators (ROs) are fabricated in a 65 nm process and oscillation frequencies are measured. The frequencies of ROs are controlled by MOSFET switches between power (ground) rails and virtual power (ground) nodes. Initial frequencies of ROs with PMOS switches are slower in upper layers. However, those with NMOS switches are faster than those without PID because high-k dielectrics are damaged by positive charge. $V_{\rm th}$ is shifted by more than 7.7% and 11% due to PID in PMOS and NMOS respectively.

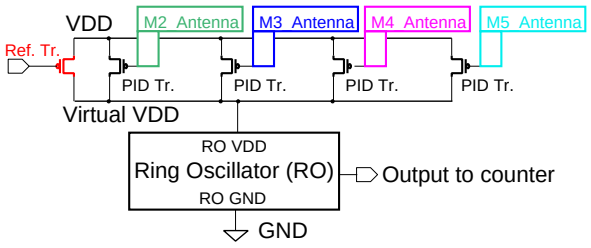
1. Introduction

Plasma induced damage (PID) is caused by charge during metallization process [1]. It shifts threshold voltage ($V_{\rm th}$) and oscillation frequency. Previous researches evaluated difference between SiO_2 and high-k (HK) dielectrics [2], square and comb antenna shape [3], thickness of dielectrics [4] and so on. This paper focuses on PID depending on antenna layers. Ring Oscillators (ROs) are fabricated in a 65 nm Fully-Depleted Silicon-On-Insulator (FDSOI) process and frequencies are measured. Frequency fluctuation is converted to $V_{\rm th}$ by circuit simulations.

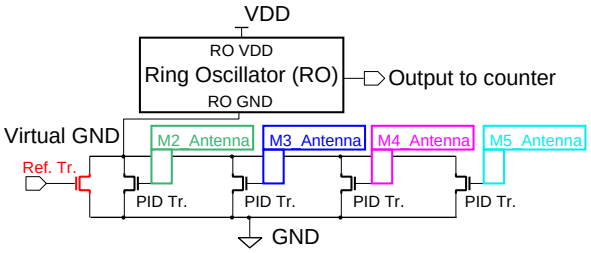
2. Measurement Circuits

We fabricated a chip including 11-stage ROs in a 65 nm process. In previous measurement circuits, antennas are connected directly on wires inside ROs [1, 5]. However, it cannot separate PID effects between PMOS and NMOS. Fig. 1 shows the proposed measurement circuit to evaluate PID. PMOS transistors are inserted between VDD and RO VDD (virtual VDD) as shown in Fig. 1(a). A PMOS transistor without an antenna (Ref. Tr.) is inserted as a reference. PMOS transistors with the antenna (PID Tr.) are also inserted. These PID Tr. are influenced by PID. Each PID Tr. has a different antenna layer from the second (M2) to the fifth (M5) metal layers. These layers have same metal thickness and width. When a PID Tr. is ON, virtual VDD voltage and oscillation frequency decrease if $V_{\rm th}$ of the PID Tr. increases. PID depending on antenna layers can be evaluated by comparing frequencies of ROs with Ref. and PID Tr. NMOS transistors are inserted between GND and RO GND (virtual GND) to evaluate PID on NMOS as shown in Fig. 1(b). Fig. 2 shows a cross section of Ref. and PID Trs. in these measurement circuits. Gate metal area of Ref. Tr. is as smallest as possible to avoid PID. M5 PID Tr. has large M5 area for the antenna. Areas of other metal layers on M5 PID Tr. are minimized. From M2 to M4 PID Trs. have similar structures.

Fig. 3 shows the test chip fabricated in a 65 nm FDSOI process. The chip size is 2 mm x 1.5 mm. It has 70 ROs in each structure. The antenna ratio is 2k in all ROs.



(a) PMOS type.



(b) NMOS type.

Fig. 1. Measurement circuit to evaluate PID with different antenna layers.

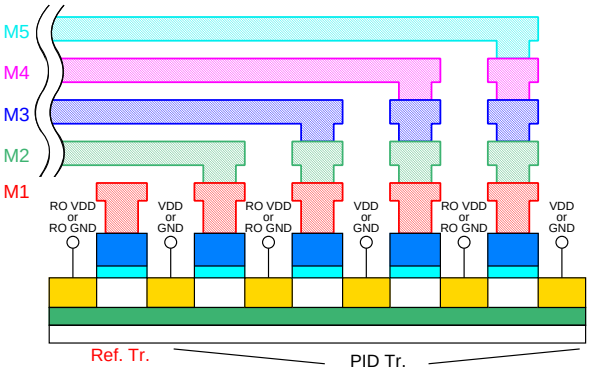


Fig. 2. Cross section of Ref. and PID Trs.

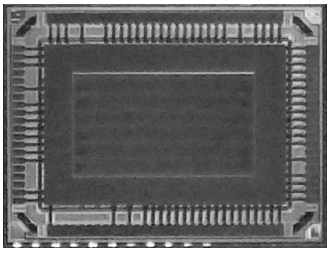
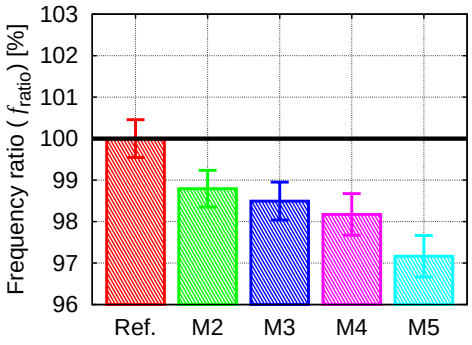


Fig. 3. Chip micrograph.

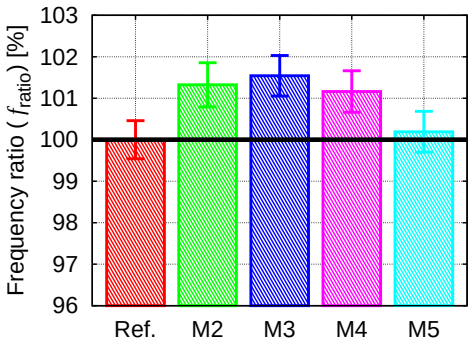
3. Measurement Results

Initial frequencies are measured to evaluate PID. Measurement conditions are at room temperature, 1.0 V supply voltage and 28 μs oscillation time. Frequency ratio ($f_{\rm ratio}$) are calculated by Eq. (1).

$$f_{\rm ratio} = f_{\rm PID}/f_{\rm Ref} \quad (1)$$



(a) Initial frequencies of PMOS type.



(b) Initial frequencies of NMOS type.

Fig. 4. Measurement results of initial frequencies.

f_{PID} and f_{Ref} are frequencies of PID and Ref. Tr. respectively. f_{ratio} indicates how the initial frequency differs from that of Ref. Tr.

Fig. 4 shows the measurement results. Initial frequencies of PMOS types with the antenna are slower than those of Ref. Tr. as shown in Fig. 4(a). The ROs with M5 Tr. are the lowest f_{ratio}. V_{th} degrades by PID in PMOS with antennas in upper metal layers. The initial frequency of M5 Tr. decreases by 2.8% from Ref. Tr. However, initial frequencies of NMOS types are faster than those of Ref. Tr. as shown in Fig. 4(b). V_{th} is decreased by PID in NMOS. It is explained by positive charging damage in HK dielectrics [6]. The fabricated FDSOI process uses SiON and HK to control V_{th} by gate work functions. V_{th} decreases due to positive charging damage in HK. However, if SiON suffers from PID, V_{th} increases regardless of positive or negative charge as shown in Fig. 5 [6]. V_{th} decreases in any metal layer by positive charging damage to HK. However, SiON is damaged and V_{th} increases in upper metal layers.

4. Threshold Voltage Conversion

We convert frequency fluctuation to V_{th} shift using circuit simulations. Simulated circuits are with parasitic capacitance and resistance from designed layout patterns. Frequency oscillations are simulated with changing V_{th} of PID Tr. Fig. 6 shows the simulation results. X-axis is V_{th} shift (ΔV_{th}). V_{th} decrease in both PMOS and NMOS to fit for measurement data as shown in Fig. 4. Y-axis is frequency ratio based on the frequency without ΔV_{th}. Frequency ratio of PMOS and NMOS are in proportion to ΔV_{th}. Table I shows results of V_{th} conversion. ΔV_{th} of NMOS M5 Tr. is only 1.1%. However, there are also over 7.7% and 11% ΔV_{th} in PMOS and NMOS respectively. Designers should consider V_{th} shifts caused by PID, particularly depending on metal layers.

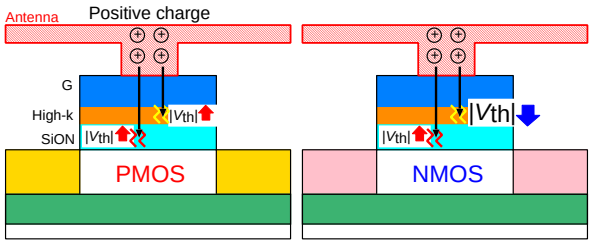


Fig. 5. V_{th} fluctuation due to positive charge.

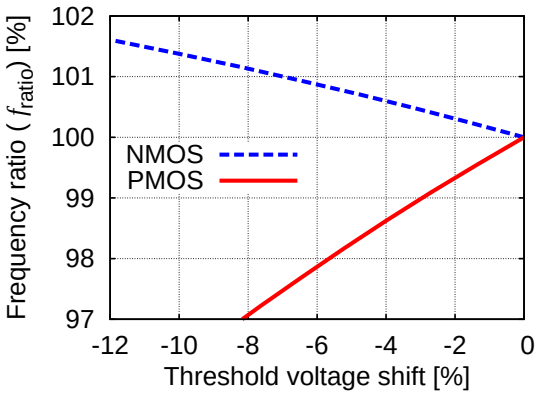


Fig. 6. Simulation results of V_{th} shift.

Table I. V_{th} conversion results.

$-\Delta V_{\mathrm{th}}$[%]	M2	M3	M4	M5
PMOS	3.4	4.2	5.1	7.7
NMOS	9.6	11	8.4	1.1

5. Conclusion

We fabricated ROs in 65 nm FDSOI process to evaluate PID depending on antenna layers. PMOS and NMOS switches are inserted between power or ground rails and virtual power or ground nodes. Oscillation frequencies of transistors with antenna is compared with those without antenna. Initial frequencies of PMOS switches decrease by incrementing antenna layers. However, ROs of NMOS switches with antenna become faster than ROs without antenna because HK is damaged by positive charge. V_{th} on both PMOS and NMOS transistors shift by 7.7% and 11% respectively in the worst case. V_{th} shift caused by PID should be considered during chip design.

Acknowledgment

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