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# Radiation Hardness Evaluations of 65 nm FD-SOI and Bulk processes by Measuring SET Pulse Widths and SEU Rates

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**Abstract**

**We measure SET (Single Event Transient) pulse widths on inverter chains and SEU (Single Event Upset) rates on flip-flops (FFs) fabricated in 65-nm FD-SOI (Fully Depleted Silicon On Insulator) and bulk processes. The layout designs of test chips are strictly identical between their processes besides BOX (Buried OXide) layers. Experimental results show that neutron-induced SEU and SET rates in the FD-SOI process are 230x and 450x lower than those in the bulk process, respectively.**

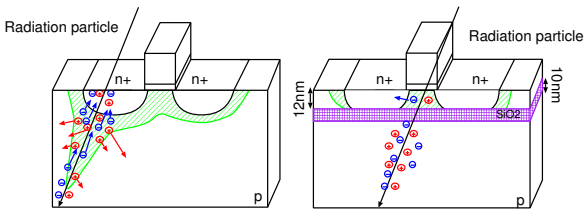
## 1. Introduction

According to the process scaling down to nanometers, LSI is less reliable to radiation-induced soft errors such as SEU and SET [1]. SEU is a flip of the state of memory elements by radiation-induced charge collection at a sensitive node such as the drain [2]. SET pulse is also caused by radiation strikes in combination circuit [3]. For soft error resilience, there are radiation-hardened FFs and FD-SOI technology. Radiation-hardened FFs have area, delay and power consumption penalties than D-FF, while FD-SOI transistors have high soft error resilience without any overhead [4]. It is because that FD-SOI transistors can suppress the effects of charge collection [5]. Fig. 1 shows how charged particles act to produce a single event both in bulk and FD-SOI processes.

In this paper, we measure neutron-induced soft error rates on logic circuits fabricated in a 65-nm FD-SOI technology and a 65-nm bulk technology. The layout designs of test chips are strictly identical between FD-SOI and bulk processes except for thin BOX layers.

## 2. Test Circuit Structure

Inverter chains and TDCs (time-to-digital converters) are embedded to measure SET pulse width distribution. Fig. 2 shows the schematic circuit diagram of embedded inverter chains and a TDC. It is connected to a 16 inverter chains through the logic tree of NAND and NOR gates. Each inverter chain consists of 50 inverters. This structure suppresses propagation-induced effect and measures SET pulse widths accurately [6]. Fig. 3 shows a circuit structure to measure SET pulse widths. The implemented TDC is based on ring-oscillator and counter. It measures SET pulse width by the resolution of delay time of the inverter in ring-oscillator. In 65-nm FD-SOI and bulk processes, the resolutions of TDC are 19.6 ps and 37.1 ps respectively when supply voltage is 1.2 V. These resolutions are obtained from calibration results as shown in Fig. 4. To measure SEU rates on FFs, we prepare a shift-register based FF array, which is constructed by FFs and a clock buffer chain [8].




(a) bulk (b) FD-SOI

Fig. 1. Collection of charge at drain region

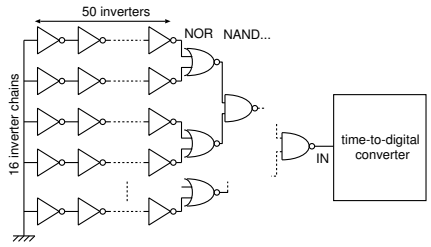



Fig. 2. Schematic circuit diagram of embedded inverter chain and TDC.

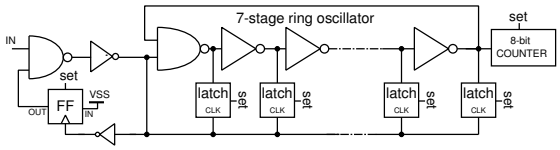



Fig. 3. Time-to-digital converters to measure SET pulse width.

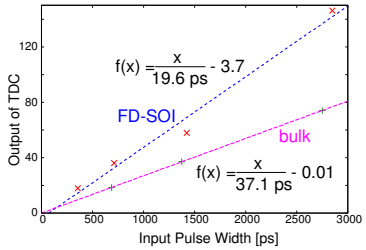



Fig. 4. Calibration results of TDC fabricated in 65nm FD-SOI and bulk processes.

Fig. 5 shows the fabricated test chip micrograph with floorplan and layout pattern. The layout designs of test chips are strictly identical between FD-SOI and bulk processes to compare soft error rates. However, the channel impurity concentrations and the threshold voltage of FD-SOI transistors are lower than those of bulk transistors [9]. The body thickness is 12 nm and the thickness of buried-oxide layers is 10 nm in the FD-SOI process. The test chip includes 829 units of SET pulse measurement circuits and a 140,000 bit FF array. To measure dependencies of SETs, we implemented 6 different types of inverter chains. The parameters of implemented inverter chains are summarized in Table I.

## 3. Experimental Results

Accelerated tests were performed by the spallation neutron beam at RCNP (Research Center for Nuclear Physics, Osaka University). The average accelerated factor is $4.8 \times 10^8$. We measured 12 FD-SOI test chips and 12 bulk test chips simulta-

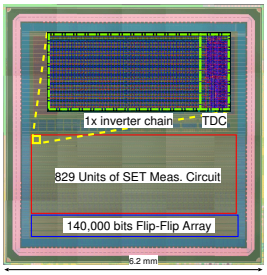



Fig. 5. Fabricated test chips micrograph with foorplan and layout pattern.

Table I. The parameters of implemented inverter chains.

| inverter chains | drive strength | fanout | well-contact interval [$\mu$m] | drain area [a.u.] |
|---|---|---|---|---|
| 1x | 1 | 1 | 50 | 1 |
| 1xWC | 1 | 1 | 2 | 1 |
| 1xFO2 | 1 | 2 | 50 | 1 |
| 1xFO4 | 1 | 4 | 50 | 1 |
| 2x | 2 | 1 | 50 | 1 |
| 4x | 4 | 1 | 50 | 2 |

Table II. SEU rates on FD-SOI and bulk FFs.

| stored values | FD-SOI | bulk |
|---|---|---|
| | SEU rate [n/Mbit/h] | SEU rate [n/Mbit/h] |
| ALL1 | 1.1 | 185 |
| ALL0 | 0.5 | 188 |

neously and their supply voltages were fixed to 1.2 V. During irradiation, all stored values of the FF array are initialized to "0" or "1". Stored values are retrieved and initialized every 7 minutes.

Table II shows SEU rates on the FD-SOI and bulk FFs. Average SEU rate on the FD-SOI FFs is 230 times lower than that on the bulk FFs. The enhancement of soft error resilience by the FD-SOI technology is bigger than that by radiation-hardened design such as dual interlocked storage cell (DICE) latch [10, 11].

Table III shows SET rates on the FD-SOI and bulk inverter chains. Only one SET pulse was injected in the FD-SOI inverter chains in the 485 times measurement (approximately 5 hours neutron irradiation) . In average, the FD-SOI inverters are 450x less susceptible than the bulk inverters. In the bulk process, SETs are observed in all inverter chains. The 1x inverter has highest SET rate and other inverters have only 1.5x – 3.5x higher error resilience than the 1x inverter. Therefore, it is difficult to completely eliminate soft errors by resizing gate widths of transistors and by connecting extra load capacitance in the bulk process.

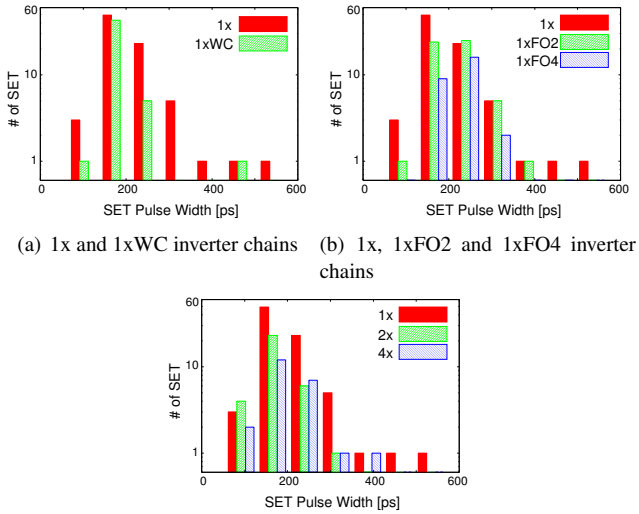
Fig. 6(a) shows SET pulse width distributions on 1x and 1xWC inverter chains. SET pulse widths are roughly exponentially-distributed and average SET pulse width on 1xWC inverters is shorter than that on 1x inverters. It is because 1xWC inverter chains have high density well-contact as shown in Table I. These results correspond to our previous results [12]. Fig. 6(b) shows SET pulse width distributions on 1x, 1xFO2, and 1xFO4 inverter chains and Fig. 6(c) shows SET pulse width distributions on 1x, 2x, and 4x inverter chains. Although the number of SETs is reduced according to fanout or drive strength, these inverter have almost similar distributions and average SET pulse widths.

## 4. Conclusion

We fabricated a test circuit with strictly identical layout designs in FD-SOI and Bulk processes and measure SEU rates and SET pulse width distributions. Experimental results show that neutron-induced SEU and SET rates in the FD-SOI process are 230x and 450x lower than that in the bulk process respectively. As for SET pulse width in bulk process, the number of SETs is reduced according to fanout, drive strength or high density well-contact. However, it is difficult to completely eliminate SET by their method. FD-SOI technology can effectively enhance soft error resilience without area, delay and power consumption penalties.

Table III. SET rates on FD-SOI and bulk inverter chains.

| inverter | FD-SOI | | bulk | |
|---|---|---|---|---|
| | SET rates [n/Minv./h] | average SET pulse width[ps] | SET rates [n/Minv./h] | average SET pulse width[ps] |
| 1x | 0.0 | N/A | 26 | 185 |
| 1xWC | 0.0 | N/A | 17 | 159 |
| 1xFO2 | 0.0 | N/A | 14 | 195 |
| 1xFO4 | 0.0 | N/A | 7.4 | 202 |
| 2x | 0.0 | N/A | 12 | 156 |
| 4x | 0.2 | 78 | 7.6 | 180 |




(a) 1x and 1xWC inverter chains (b) 1x, 1xFO2 and 1xFO4 inverter chains

(c) 1x, 2x and 4x inverter chains

Fig. 6. SET pulse width distributions in 65nm bulk process.

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## References

[1] S. Borker et. al., *IEEE Micro*, vol. 25, No. 6, pp. 10-16 2005.
[2] T. May et. al., *IEEE Trans. Electron Devices*, vol. ED-26, pp. 2-9. 1979.
[3] P. Shivakumar et. al., *DSN*, pp. 389-398. 2002.
[4] J. Baggio et. al., *IRPS*, pp. 677-678, 2004.
[5] V. Ferlet-Cavrois et. al., *IEEE, Trans. Nucl. Sci.*, vol. 49, No. 6, pp. 2948-2956, 2002.
[6] M. J .Gadlage et. al., *TDMR*, vol. 10, no. 1, pp.157-163, 2010.
[7] J. Furuta et. al., *IRPS*, pp. SE.5.1-SE.5.5. 2012.
[8] J. Furuta et. al., *ASP-DAC*, pp. 83-84. 2011.
[9] N. Sugii et. al., *IEEE Trans. Elec. Dev.*, vol. 57, no. 4, pp. 835-845. 2010.
[10] D. Krueger et. al., *ISSCC*, pp. 94-95. 2008.
[11] P. Hazucha et. al., *JSSC*, vol. 39, no. 9, pp 1536-1543, 2004.
[12] J. Furuta et. al., *IRPS*, pp. 5B.2.1-5B.2.5 2011.