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# Impact on delay due to random telegraph noise under low voltage operation in logic circuits

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## 1. Introduction

Recently, reliability of an advanced LSI becomes a serious issue because of the variability associated with the technology scaling. In particular, Random Telegraph Noise (RTN) has attracted much attention as a temporal variation that has been enlarged with the scaling. Recently, Intel demonstrated a micro processor that can operate over a wide voltage range from 0.28 V to 1.2 V, targeting near-threshold computing that brings the promise of an order of magnitude improvement in energy efficiency [1]. However, such an aggressive voltage scaling may not result in a stable operation of conventional logic circuits. In near-threshold operation, a slight fluctuation in the threshold voltage ($\Delta$Vth) such as induced by RTN, may lead to a serious delay increase that will cause malfuction of the circuit operation. The purpose of this paper is to evaluate and issue an alert the impact of RTN on circuit delay fluctuation under low voltage operation.

## 2. Test structure for RTN-induced Delay fluctuation Measurement

We use a circuit matrix array for the evaluation of RTN-induced delay fluctuation. Fig. 1 shows the test structure fabricated in a 65nm process. The circuit matrix array contains 18 $\times$ 14 7-stage ring oscillators(ROs). We therefore have 252 identical 7-stage ROs, which we consider as representatives of combinational circuits. The output of each RO is connected to a divider so that we can measure the oscillation frequency of the RO, as shown in the bottom part of Fig. 1. The RO and the divider have separate power supplies, $V_{\mathrm{DD\_D-FF}}$ and $V_{\mathrm{DD\_RO}}$, such that we can measure oscillation frequency under low voltage operation of the RO while we can expect stable operation of the divider with a higher supply voltage than the RO. The RO has a homogeneous structure. That is, except for a NAND Gate for controlling oscillation, all the inverter gates have the identical circuit structure with the same device sizes. Each transistor has within-die (WID) variability, but the variation is averaged out in the RO. In the homogeneous RO, RTN is expected to have a little effect on oscillation frequency at a normal operating voltage. However, as we lower the supply voltage, the delay fluctuation due to the threshold voltage variation becomes large. RTN-induced delay fluctuation may becomes visible, and in some cases becomes fatal, which is the target of our investigation.

## 3. Experimental Results and Discussion

A. Impact of RTN on delay in combinational circuits

We assume that the maximum frequency shift for each RO is caused by RTN. Fig.2 shows the cumulative distribution of the frequency fluctuation by RTN measured at $V_{\mathrm{DD\_RO}} = 0.6$ V and $V_{\mathrm{DD\_D-FF}} = 0.9$ V. Many ROs exhibit small amount of fluctuation. However, we have observed a large amount of fluctuations up to 6.2 % in several ROs.

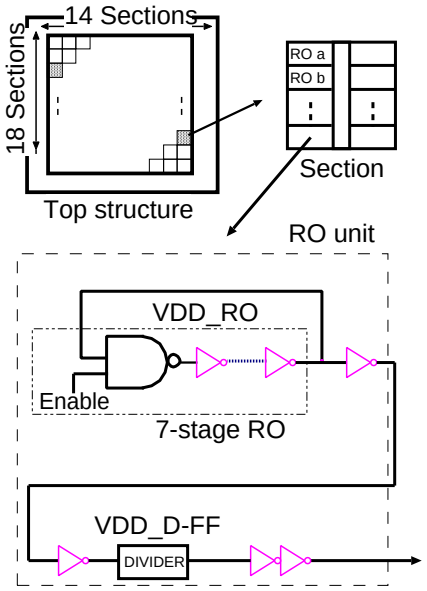


Figure 1: A test structure for process variation and RTN-induced delay fluctuation measurement in 65nm process.

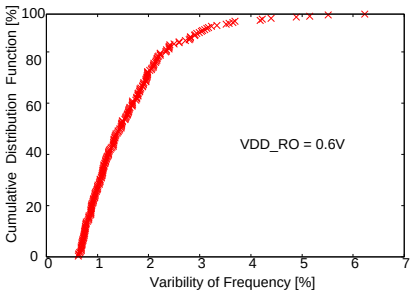


Figure 2: Distribution of RTN-induced frequency fluctuations at $V_{\mathrm{DD\_RO}} = 0.6$ V.

B. The dependence of RTN-induced delay fluctuation on supply voltage

It has been reported that the ratio of RTN-induced frequency fluctuation increases as $V_{\mathrm{DD\_RO}}$ decreases [3]. So, it is concerned that the frequency fluctuation becomes very serious at a low supply voltage in a logic circuit. To evaluate the frequency fluctuation at a low supply voltage, we set up the RO supply $V_{\mathrm{DD\_RO}}$ from 0.4 V to 0.6 V at 50 mV intervals.

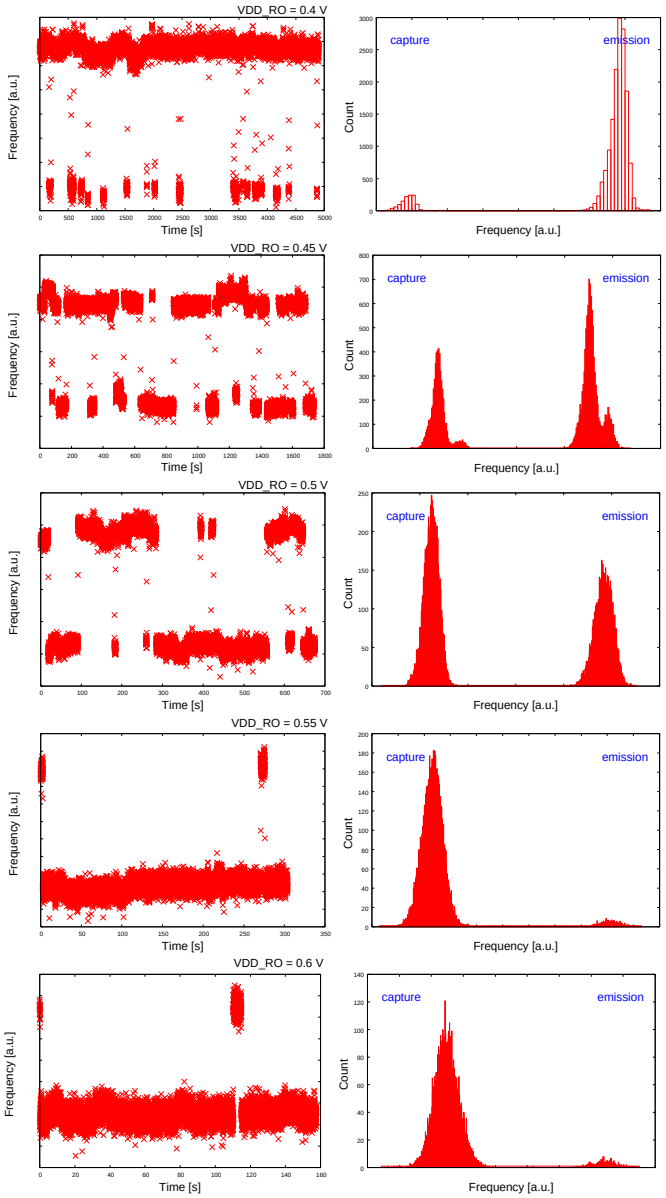


Figure 3: The dependence of supply voltage on RTN-induced delay fluctuation (sample 3 in Fig.5).

Fig.3 shows frequency fluctuation at a certain sample on various supply voltages. When a charge carrier is captured by a defect inside the dielectric of a MOSFET, RO flequency becomes low. As for the average values of time to capture ($\tau_c$) and time to emission ($\tau_e$), the former decreases and the latter increases with the decreased amount of supply voltage (Fig.4). The same property of $\tau_c$ and $\tau_e$ can be observed in a transistor-level RTN measurement where drain current fluctuation is measured under a DC bias condition. In our experiment, we can evaluate RTN by observing frequency fluctuation under operationg condition using the test structure.

We have selected 3 samples from 252 ROs that show distinctive binary fluctuations for each supply voltage. In those ROs, the histgram of oscillation frequencies exhibits a mixture of two gaussian distribution as shown in Fig.3. We evaluate the amount of frequency fluctuation from those distributions. Fig.5 shows the frequency fluctuation as a function of supply voltage. Fig.5 shows a linear relationship between the fluctuation and supply voltage of 0.5 V and above, and the saturation near threshold voltage. At a low supply voltage around 0.4 V, the variability of the frequency becomes very severe and may cause a failure in circuit operation.

## 4. Conclusion

We have measured RTN-induced delay fluctuation in CMOS logic circuits using a circuit matrix array test structure. At a normal operating voltage, the impact of RTN on frequency fluctuation is small in a homogeneous combinational circuit. However, near threshold voltage, it become so serious that RTN-induced frequency degradation may cause a failure in circuit operation. So, it is essential that a circuit designer should consider the impact of RTN on delay fluctuation under low voltage operation.


## Acknowledgement

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## References


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[2]K. Ito, et al., IRPS2011, p.710.


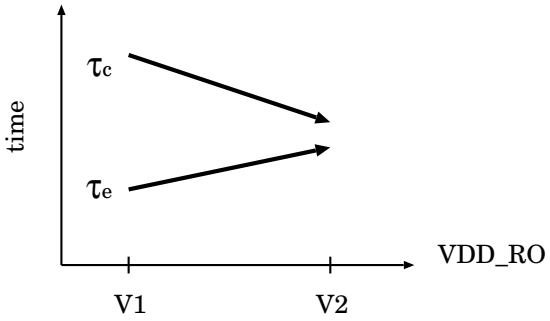


Figure 4: The concept of the dependence of $\tau_c$ and $\tau_e$ on supply voltage. It is similar to the dependence of those on DC bias.

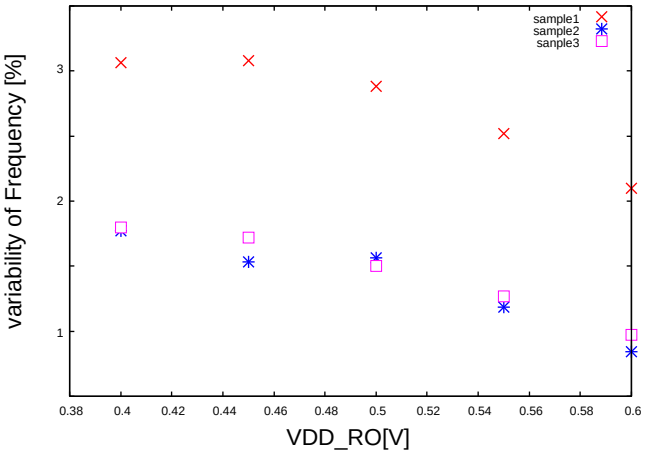


Figure 5: Impact on delay due to RTN induced by one trap for each supply voltage.