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Impact of Body-Biasing Technique on RTN-induced Delay Fluctuation

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1. Introduction

Designing reliable systems has become more difficult in recent years[1]. In addition to conventional problems such as transistor leakage, the degradation and variation of transistor performance have a severe impact on the dependability of VLSI systems. Random Telegraph Noise (RTN) has attracted much attention as a temporal transistor performance fluctuation. RTN already has a severe impact on CMOS image sensors[2], Flash memories[3], and SRAMs[4]. Recently we have shown that RTN also induces performance fluctuation to logic circuits[5]. On the other hand, adaptive body-biasing technique has been widely used to compensate for die-to-die parameter variations[6]. However, the impact of the body-biasing technique on RTN at the circuit level has not been well understood. In this paper, we investigated the impact of body-biasing technique on RTN-induced circuit delay fluctuation.

2. Simplest Test Structure of Synchronous Circuit

Figure 1 shows the simplest test structure that can emulate the synchronous circuit operation. Combinational circuit delay is emulated by ring oscillator (RO) oscillation frequency. Sequential circuit operation is emulated by D-FF that is toggled by the RO output. The power supply for RO and D-FF can be independently controlled. The substrate bias for p-type substrate and n-type substrate can also be independently controlled. Figure 2 shows the whole test structure for RTN measurement. RTN-induced delay fluctuation is measured by the RO frequency fluctuation. There are 840 same samples of Fig. 1 on 2 mm^2 area and the statistical nature of RTN can be evaluated by the RO array. This chip is fabricated in a commercial 40 nm CMOS technology. All measurements are done at room temperature. Figure 3(a) shows the measurement results of the oscillation frequency for about 100 s

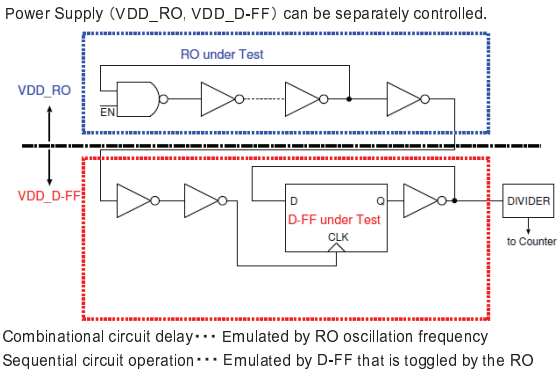

Figure 1: Simplest test structure that can emulate the synchronous circuit operation.

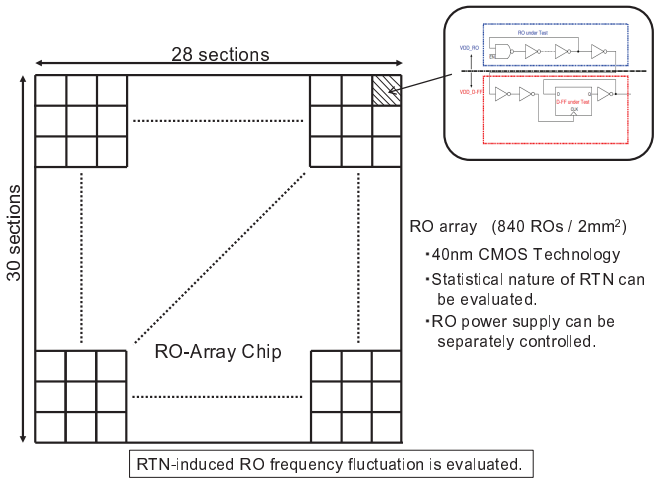

Figure 2: Whole test structure for RTN measurement.

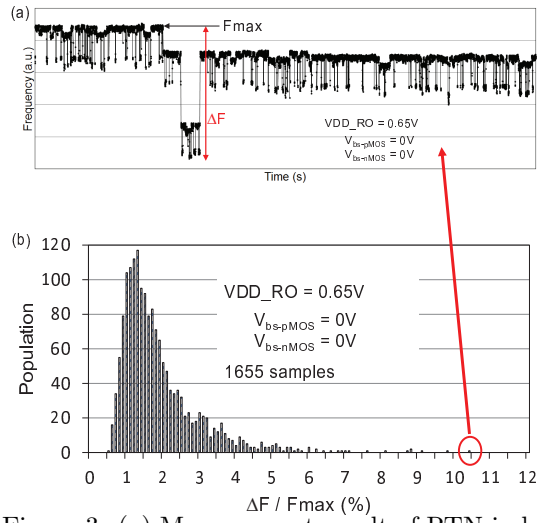

Figure 3: (a) Measurement result of RTN-induced RO frequency fluctuation. (b) Histogram of measured $\Delta F/F_{max}$.

at VDD_RO=0.65V. The body bias for pMOS ($V_{bs\text{-}pMOS}$) and nMOS ($V_{bs\text{-}nMOS}$) are set to 0 V. Measurement results show the large step-like frequency fluctuation. Here, F_{max} is defined as the maximum oscillation frequency and ΔF is defined as the maximum frequency fluctuation as shown in Fig. 3(a). $\Delta F/F_{max}$ is a good measure for the impact of RTN-induced frequency fluctuation and $\Delta F/F_{max}$ = 10.4 % for Fig. 3(a). Figure 3(b) shows the histogram of measured $\Delta F/F_{max}$ for the whole test structure of Fig. 2 over two chips (1655 ROs). It is found that small number of samples have a large RTN-induced fluctuation and a long tail exists for larger $\Delta F/F_{max}$.

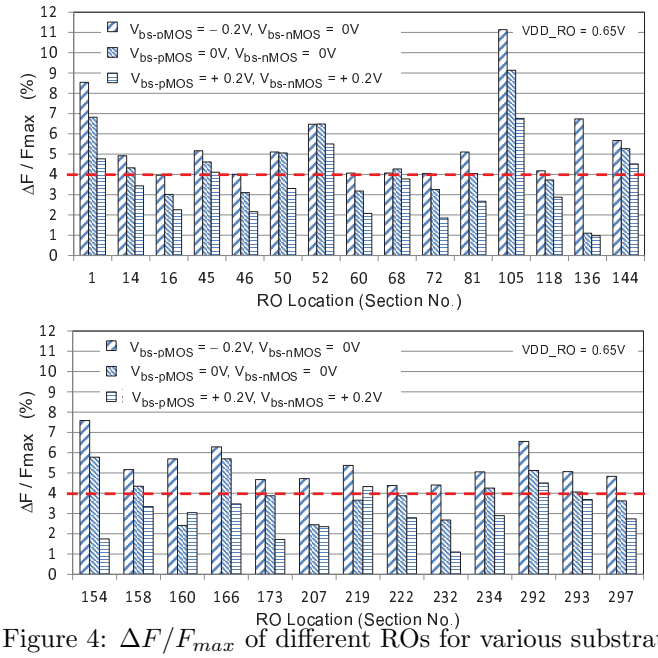

Figure 4: $\Delta F/F_{max}$ of different ROs for various substrate bias condition. ROs that have more than 4 % fluctuation at reverse substrate bias case are shown.

3. Impact of Body-Biasing Technique on RTN

Figure 4 shows the the measurement results of $\Delta F/F_{max}$ of different ROs for various substrate bias condition. Substrate bias conditions are categorized as reverse bias case ($V_{bs\text{-}pMOS} = -0.2V$, $V_{bs\text{-}nMOS} = 0V$), normal bias case ($V_{bs\text{-}pMOS} = 0V$, $V_{bs\text{-}nMOS} = 0V$), and forward bias case ($V_{bs\text{-}pMOS} = +0.2V$, $V_{bs\text{-}nMOS} = +0.2V$). 300 ROs in one test structure of Fig. 2 are investigated at VDD_RO=0.65V. Figure 4 shows ROs that have more than 4 % fluctuation at reverse bias case to evaluate the forward body-bias effect on large $\Delta F/F_{max}$ samples (24 ROs). When substrate bias is changed from the reverse bias case to the forward bias case, $\Delta F/F_{max}$ tends to decrease. However, for example, $\Delta F/F_{max}$ slightly increases in the case of the RO location "68" and "219" when forward substrate bias is applied. It is found that the impact of RTN-induced delay fluctuation tends to be reduced by forward body-biasing technique, but a few ROs do not follow this tendency. To further investigate the forward body-bias effect on RTN, $\Delta F/F_{max}$ is plotted with respect to oscillation frequency (Fig. 5). When pMOS substrate bias ($V_{bs\text{-}pMOS}$) is changed from −350 mV to −50 mV, it is found that $\Delta F/F_{max}$ reduces from 5.0 % to 2.8 % and the impact of RTN is suppressed by forward body-biasing. The oscillation frequency can also be changed by VDD_RO. When VDD_RO is changed by 20 mV (Fig. 5), the frequency of the RO is changed by the same amount as for the case of changing $V_{bs\text{-}pMOS}$ by 200 mV (Fig. 5). As shown in Fig. 5, $\Delta F/F_{max}$ remains almost constant value (3.5 %) when VDD_RO is changed by 20 mV. Although RTN is not suppressed by a small shift of supply voltage, RTN is suppressed by forward body-biasing.

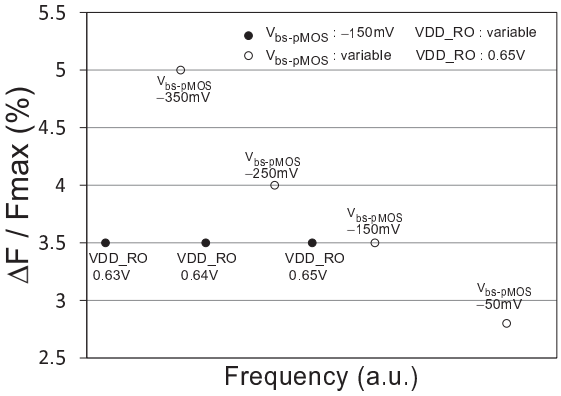

Figure 5: The impact of VDD_RO shift and body-bias shift on $\Delta F/F_{max}$.

4. Conclusions

By measuring 822 ROs fabricated in a commercial 40 nm CMOS technology, statistical nature of RTN-induced delay fluctuation is described. Small number of samples have a large RTN-induced delay fluctuation. It is found that the impact of RTN-induced delay fluctuation becomes as much as 10.4 % under low supply voltage (0.65V) operation. It is also found that the impact of RTN-induced delay fluctuation tends to be reduced by forward body-biasing technique, but a few ROs do not follow this tendency.

Acknowledgement

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