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Multi-core LSI Lifetime Extension by NBTI-Recovery-based Self-healing

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1. Introduction

Designing reliable systems has become more difficult in recent years. Besides conventional problems such as transistor leakage, the degradation and variation of transistor performance have a severe impact on the dependability of VLSI systems[1]-[3]. Negative-Bias-Temperature-Instability (NBTI) is one of the strongest reliability concerns for CMOS circuits[4][5]. Remarkable phenomena on NBTI is that degraded performance of a PMOS transistor recovers when the bias-temperature stress to the gate oxide is removed or relaxed. In this paper, we describe multi-core LSI lifetime extension method. In the following, it is shown that LSI lifetime is extended by combining NBTI recovery and circuit parallelization. It is a crucial step for this lifetime extension method to clarify the amount of NBTI recovery. So we characterize NBTI by a very short measurement delay (400 ns) NBTI sensor[6]. It is generally believed that the measurement delay is set to as short as 1 μs to avoid NBTI recovery for the correct NBTI characterization. It is also shown for the first time that transforming silicon area into LSI reliability is a promising and realistic concept for the ever-shrinking CMOS technology.

2. Lifetime Extension by NBTI Recovery

Fig. 1 shows that an LSI performance degrades with time and finally reaches to its lifetime, for example, 10 years that is defined by the lower limit of LSI performance. If LSI performance is recovered with NBTI recovery, its lifetime can be further extended as shown in Fig. 1. As a result, it is a crucial step for this lifetime extension method with NBTI recovery to clarify the amount of NBTI recoverable component. The nature of the recoverable component is clarified with measurement results in section 4.

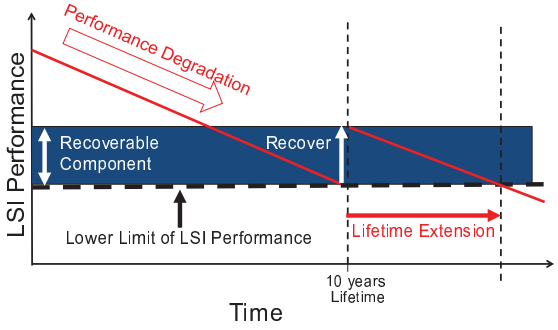

Figure 1: Degraded LSI performance can be recovered with NBTI recovery that leads to LSI lifetime extension.

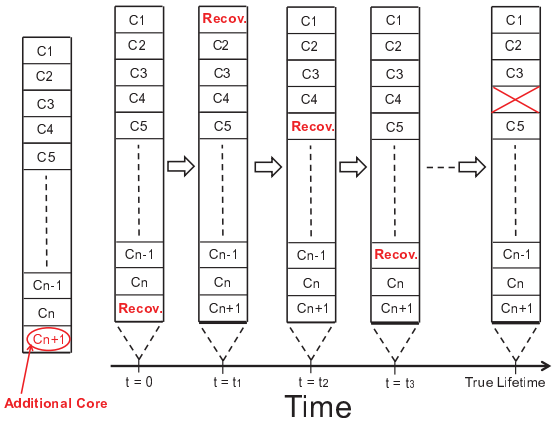

Figure 2: The example of an (n+1)-core LSI ($C_1 - C_{n+1}$) operation is shown. Shortly before C_1 reaches to its lifetime at $t = t_1$, C_1 changes to recovery mode, and C_{n+1} becomes active mode. By recovering one of $n + 1$ cores, n-core LSI system does not stop and the lifetime can be extended due to NBTI recovery.

3. Multi-core LSI Lifetime Extension

Recent scaling of CMOS device leads to circuit parallelization or multi-core architecture in many applications. Conventionally, yield is improved, power is decreased, and hot-spots on a die is decreased due to the circuit parallelization. This paper describes for the first time that transforming silicon area into LSI reliability is a promising and realistic concept for the ever-shrinking CMOS technology. Fig. 2 shows the (n+1)-core LSI ($C_1 - C_{n+1}$). For example, shortly before C_1 reaches to its lifetime at $t = t_1$, C_1 changes to recovery mode, and C_{n+1} becomes active mode. So this LSI keeps active n-core circuits. As a result, by recovering one of $n + 1$ cores, n-core LSI system does not stop and the lifetime can be extended due to NBTI recovery (Originally the lifetime is only t_1 for n-core ($C_1 - C_n$) LSI).

4. NBTI Characterization Results

To quantitatively clarify the amount of recoverable component shown in Fig. 1 is a crucial step for the lifetime extension. Recently we proposed an NBTI sensor that can characterize NBTI with a 400 ns measurement delay[6]. NBTI is characterized by the off-leak current of PMOS transistors. Because this circuit contains 2160 PMOS transistors under an NBTI stress, an averaged nature of NBTI is obtained. This circuit was fabricated in a commercial 65 nm CMOS technology. In this section, NBTI degradation and recovery measurement results with this circuit are described. Fig. 3 shows that the off-leak current decreases with stress time compared to its initial value that is also plotted in the same figure. The bias of 2160 PMOS transistors during the stress phase is $V_{gs} = -2.2$ V, $V_{ds} = 0$

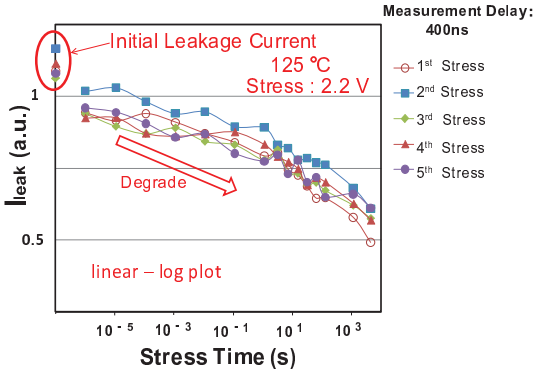

Figure 3: The off-leak current decreases with stress time compared to its initial value. The recoverable component shown in Fig. 1 measured by off-leak current remains almost constant after repeatedly added NBTI stress.

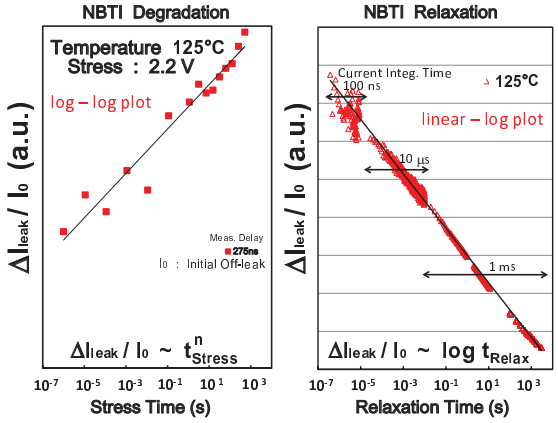

Figure 4: (left) The measurement result of NBTI degradation follows power law. (right) The measurement result of NBTI recovery follows log t. In the case of nominal operation, the relaxation speed is much faster than the degradation speed. Due to this asymmetrical nature of NBTI, lifetime extension by NBTI recovery is very effective method.

V, $V_{sub} = V_s$, and the bias during the measurement phase is $V_{gs} = 0$ V, $V_{ds} = -2.2$ V, $V_{sub} = V_s$. The stress temperature is 125°C. So stress time of 2000 s in Fig. 3 roughly corresponds to one year circuit operation at room temperature and nominal operating voltage. After this 2000 s NBTI stress is added to a DUT, the off-leak current decreases to about half of its fresh value. After enough recovery, off-leak current of the same DUT is again measured and it is found that off-leak current almost recovers to its fresh value as shown in Fig. 3. This DUT is further repeatedly stressed under the same stress condition and it is found that initial off-leak current always recovers to its fresh value as shown in Fig. 3. It means that the recoverable component shown in Fig. 1 measured by off-leak current remains almost constant after repeatedly added NBTI stress. In a real application, there may not be enough time to recover. Fig. 4 (right) shows the NBTI recovery clearly follows log t from 400 ns to 3000 s. Further details are described in [6]. By modeling the recovery behavior of Fig. 4 (right), the amount of NBTI recovery can be tuned by a relaxation time in a real application. Fig. 4

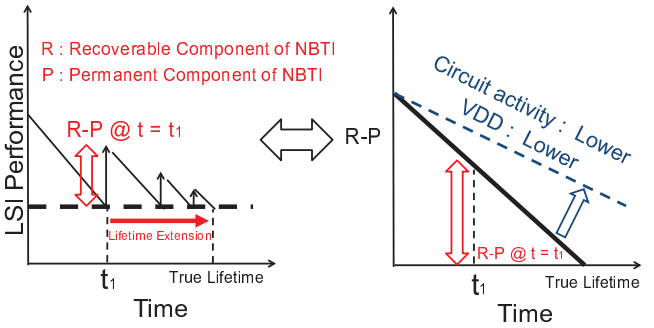

Figure 5: The concept of a circuit operation to extend its lifetime. LSI performance can be repeatedly recovered until $R - P$ reaches to zero.

(left) shows the NBTI degradation measurement result and we can predict the degradation by the power law behavior. Fig. 5 shows the concept of a circuit operation to extend its lifetime. Effective recoverable component, $R-P$, decreases with time because the permanent component of NBTI (P) gradually increases. True lifetime is defined as the time when $R - P = 0$. LSI performance can be repeatedly recovered until $R - P$ reaches to zero as shown in Fig. 5. Further lifetime extension can be achieved when the operating voltage, VDD, and/or the circuit activity become lower as indicated by the blue dashed line in Fig. 5. NBTI degradation under nominal operating voltage is a gradual process compared to the NBTI recovery that follows log t with very fast component as shown in Fig. 4 (right). Due to this asymmetrical nature of NBTI, lifetime extension by NBTI recovery is very effective method. In the case of multi-core LSI under a given workload, NBTI-recovery-based self-healing by the additional core works effectively when the degradation speed of slow process corner core is reduced.

5. Conclusions

It is shown that LSI lifetime can be extended by combining NBTI recovery and circuit parallelization. NBTI recovery is characterized by the recently proposed NBTI sensor with 400 ns measurement delay that is fabricated in a commercial 65 nm CMOS technology. Measurement results show that the recoverable component measured by off-leak current remains almost constant after repeatedly added NBTI stress. It is also shown that the amount of NBTI recovery can be tuned by a relaxation time in a real application and it follows log t from 400 ns to 3000 s. As a result, multi-core LSI lifetime extension can be achieved. For the first time, transforming silicon area into LSI reliability is shown to be a promising and realistic concept for the ever-shrinking CMOS technology.

Acknowledgement

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